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A futuristic digital interface with a glowing globe in the center. The interface features various data visualizations including bar charts, line graphs, and network diagrams. Text elements like 'BUSINESS', 'NETWORK SEARCH', and 'LADING 100%' are visible. The background is a dark blue with light blue highlights, suggesting a high-tech environment. A person's hand is visible at the bottom, interacting with the interface.

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# High Speed and Area Efficient FIR Filter using Distributive Arithmetic Technique and Compressor based Adder

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**ABSTRACT:** The execution of FIR channels on FPGA taking into account conventional technique costs significant equipment assets, which conflicts with the diminishing of circuit scale and increment of framework pace. FIR channels utilizing Arithmetic is utilized to build the asset use while pipeline structure is additionally used to expand the framework speed. Moreover, the isolated LUT strategy is additionally used to diminish the required memory units. Distributed Reconfigurable Partial Product Generation (DRPPG) based Reconfigurable FIR filter has been designed with the help of Distributed Arithmetic (DA) based multiplication techniques. DA multiplication technique performs the multiplication without help of any specialized multiplication architecture. Hence, this architecture called as "Multiplier-less Architecture". Bi-Recoder technique has been performed to provide the partial product generation. All the LUT's are provided with different inputs at the same time, implying parallel mechanism. This increases the speed of operation.

**KEYWORDS:** - Look Up Table (LUT), Read Only Memory (ROM), Distributive Arithmetic (DA), Xilinx Simulation

## I. INTRODUCTION

A Digital filter is a filter that performs mathematical operations on sampled and discrete time signals to reduce or enhance the certain aspect of the signals. It usually consists of an Analog-to-digital converter block to convert the analog form of signal to digital form signal (sampled data or discrete time signal). To perform the numerical operations on the sampled data or discrete time signal, digital signal processors are used. This processor may be a general purpose processor such as PC or a microprocessor or a DSP chip Ozalevli [1].

In some high-performance applications, FPGA or ASIC is used instead of general purpose processor or specialized DSP with particular parallel architecture for performing operations such as filtering. It carries the numerical calculations on sampled data. These calculations typically involve multiplying the input values by constants and adding the products together [2, 3].

In addition to, some peripheral components such as memories are used to store the data. Finally, a Digital-to-Analog converter block is used to convert the processed digital signal to corresponding analog signal. FPGA's are reprogrammable for various equipment capacities with no expansion in the execution cost as connected with custom ICs and ASIC's. Configurability and parallelism are the real points of interest of FPGA's. Size/adaptability of the rationale cell, speed and the directing engineering are central point for a FPGA based outline. The rationale cell executed on FPGA can be a basic transistor or an unpredictable structure like chip [4].

FPGA's have two execution approaches. One is through SRAM based LUT and the second using multiplexer based rationale components. Multiplexer based execution is by and large quicker than SRAM based outline, yet possess marginally more prominent region [5].

Commutation and other undesirable sign parts of a sign can be evacuated by computerized channels. They work on a limited accuracy computerized representation of a sign. Simple signs are changed over to advance by testing, quantizing and coding. A small special purpose digital computer then processes the obtained digital signal and converts the input sequence into a desired output sequence [5, 6].

Advanced preparing of simple signs has a few points of interest. The PC can be time shared for a few uses and the computerized usage expense is impressively lower than that of its simple partner. Advanced channel's exactness depends just on the word length, quantizing interim and the testing rate. Instead of RLC segments, the advanced

channels utilize basic components like adders, multipliers, shifters and postponement components. Subsequently they are not influenced by elements like temperature, warm float and others that influence the simple channel. Advanced channels can be altered by basically changing the PC calculation as opposed to simple framework which must be physically remade [6].

The execution of limited move band FIR channels requires impressively more number of juggling operations and equipment parts, for example, multipliers, adders and postponement components. To accomplish the same frequency detail, FIR channels require higher number of taps contrasted with IIR channels. This makes them unacceptable for FPGA usage [7].

To stay away from MAC operations, various multipliers less methods are being utilized. Among all the accessible strategies, Distributed Arithmetic (DA) is most appropriate for FPGA execution. DA utilizes Look-Up Tables, adders and movement registers to play out the separating operation. In this system LUT's are pre developed for all the conceivable blends of inputs and the channel coefficients. They are conjured while performing channel operation.

Parallel DA architecture was improvised with split LUT and slight modification in the structure. Instead of using ROM for each input data's, LUT is fed with a set of 4 data's. This again resulted in parallel operation. The structure provides flexibility to alter the contents of LUT as against ROM usage. The limitations of the structure were, as the number of inputs increased, required LUT structures proportionately increased thereby resulting in an increase in hardware utilization on FPGA, ensuing in reduction of speed of operation.

## II. DISTRIBUTIVE ARITHMETIC TECHNIQUE

DA is so named in light of the fact that the number juggling operations that show up in sign preparing (e.g., expansion, duplication) are not “lumped” as a solid useful element but rather are conveyed in a regularly unrecognizable manner. The frequently experienced type of calculation in advanced sign preparing is a total of items (or in vector investigation speech or internal item era). This is additionally the calculation that is executed most proficiently by DA. The inspiration for utilizing DA is its compelling computational productivity. The points of interest are best misused in circuit plan, however off-the-rack equipment frequently can be designed adequately to perform DA. Via cautious outline, one may decrease the aggregate door tally in a sign preparing number-crunching unit by a number sometimes littler than 50 percent and regularly as extensive as 80 percent.

DA is fundamentally (however not so much) somewhat serial computational operation that structures an inward (spot) result of a couple of vectors in a solitary direct stride. The benefit of DA is its productivity of motorization. Conveyed Arithmetic is regularly utilized, where figuring the internal result of two vectors involves the majority of the computational workload.

This kind of figuring profile depicts a huge segment of sign handling calculations; thus the potential utilization of Distributed Arithmetic is gigantic. The inward point is regularly registered utilizing multipliers and adders. At the point when registered successively, the duplication of two B-bit numbers requires B/2 to B increases, and is time concentrated. Then again, the augmentation can be registered in parallel utilizing B/2 to B adders, however is territory serious (K. Hwang 1979, D. L. Jones 1993: 1077–1086). Whether a K-tap channel is processed serially or in parallel, it requires in any event B/2 increases for every duplication in addition to K – 1 expansion for summing the items together. In the most ideal situation,  $K \cdot (B + 2) / (2 - 1)$  increases are required for a K-tap channel utilizing multipliers and adders. A aggressive contrasting option for utilizing a multiplier is Distributed Arithmetic. It packs the calculation of a K-tap channel from K augmentations and K - 1 expansion into a memory table and creates result in B-bit time, utilizing B - 1 expansion.

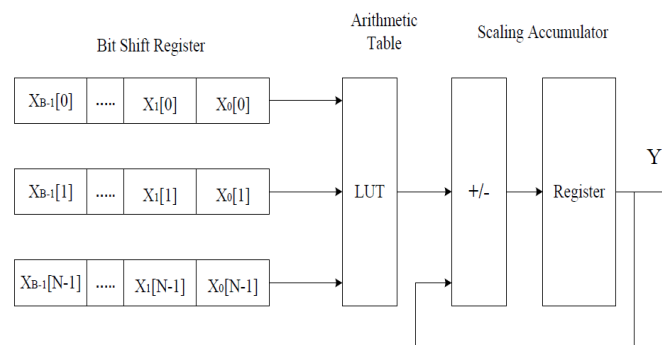


Figure 1: Distributed Arithmetic Block Diagram

### III. PROPOSED METHODOLOGY

On the off chance that the coefficients are little, it is exceptionally advantageous to acknowledge through the rich structure of FPGA LUT. While the coefficient is substantial, it will take parcel of capacity assets of FPGA and decrease the count speed.

The proposed structure of Reconfigurable DA based FIR filter is shown in Figure 2. It performs MAC function for the different filter coefficient values. Filter coefficient values are changed dynamically in the current proposed research work. The input samples are divided into some parallel instants, and each instant can execute concurrently with the help of Serial in Parallel out Shift Register (SIPOSR).

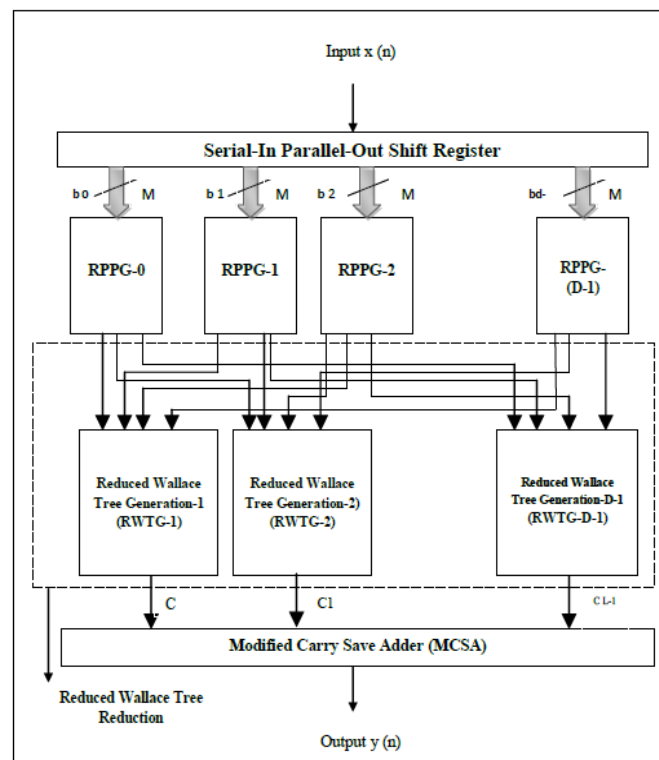


Figure 2: Proposed structure of Reconfigurable DA based FIR filter

In PPG unit, partial products of multiplication results are generated. Traditionally  $N^2$  AND gates are used to produce the partial product results. To provide the partial products, different architectures are developed which have been described in the literature part of this thesis. One of the important PPG generation multiplications is "Russian Peasant Multiplication (RPM)". In RPM based PPG unit, Multiplexors are used to generate the partial product results.

In PPR unit, the outputs coming from PPG units are reduced to two " $2*n$ " bit rows by using Wallace or Reduced Wallace Tree Reduction methodologies. Traditionally Full Adders (FAs) and Half Adders (HAs) are considered to reduce the results of PPG outputs.

In the final stage of PPA unit, there is one important addition structure will be required to add two " $2*n$ " bit data. Different types of addition structure have existed to perform binary multiplications like "Ripple Carry Adder", "Carry Select Adder" and "Carry Save Adder".

Example:-

Step 1:-  $x(n) = 0001$ , where  $x(n)$  is the input of the FIR Filter

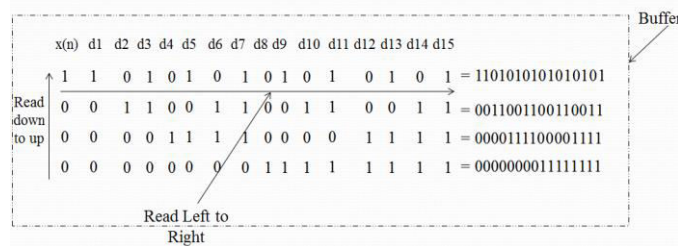
Step 2:-  $x(n)$  is passing through all delay flip flop (D-FF),

$d1=0001$ ,  $d2=0010$ ,  $d3=0011$ ,  $d4=0100$ ,  $d5=0101$ ,  $d6=0110$ ,  $d7=0111$ ,  $d8=1000$ ,  $d9=1001$ ,  $d10=1010$ ,  $d11=1011$ ,  $d12=1100$ ,  $d13=1101$ ,  $d14=1110$ ,  $d15=1111$





Step 3:- Input of the FIR filter and output of the D-FF passing through Buffer



Step 4:- All buffer passing through LUT then

h0	h1	h2	h3	h4	h5	h6	h7	h8	h9	h10	h11	h12	h13	h14	h15
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Output of the LUT

$$P1 = h0+h1+h3+h5+h7+h9+h11+h13+h15$$

$$P2 = h2+h3+h6+h7+h10+h11+h14+h15$$

$$P3 = h4+h5+h6+h7+h12+h13+h14+h15$$

$$P4 = h8+h9+h10+h11+h12+h13+h14+h15$$

Suppose

h0=0000, h1=0001, h2=0010, h3=0011, h4=0100, h5=0101, h6=0110, h7=0111, h8=1000, h9=1001, h10=1010, h11=1011, h12=1100, h13=1101, h14=1110, h15=1111

So,

$$P1 = 1000000$$

$$P2 = 1000100$$

$$P3 = 1001110$$

$$P4 = 1011100$$

Step 5:- Output of the FIR Filter

$$Y_n = P1 + P2'0 + P3'00 + p4'000$$

$$= 1000000 + 1000100'0 + 1001110'00 + 1011100'000$$

$$= 10011111000 (1240)$$

#### IV. RESULT AND SIMULATION

##### A. Simulation

The simulation was performed using XILINX and ModelSim simulator.

##### B. Hardware Utilization

The VHDL languages were used to design the VLSI architecture modules and are synthesized Virtex-2p, Vertex-E and Spartan-3 (XC2VP27FG, XCV50E8CS, and XC3s504PQ). Hardware description language (HDL) synthesis report for 16-tap, 32-tap and 64-tap FIR filter using multiplier-less DA technique are shown in table I, table II and table III respectively. It is observed from the table I, shows that the  $B(N-1) + B'(N-1)$  flip flop,  $L(N-1)$  adders,  $NL$  multiplier and  $T_M + T_A + 3T_{FA}$  cyclic period for previous design but  $(N-1)L + NL$  flip flop,  $L(N-1) + (L-1)(N+2)$  adder, 0 multiplier and  $T_A + (N-1)T_{FA}$  cyclic period for proposed multiplier-less FIR filter implemented. It is observed from the table II, the flip flop, adder, multiplier and cyclic period for the proposed FIR filter using DA technique and previous design. From the analysis of the result, it is found that the proposed FIR filter using DA technique gives a superior performance as compared with previous algorithm.

The proposed algorithm gives a flip flop 124 as compared with 312 flip flops for previous algorithm. Similarly, proposed design gives 114 adders and 0 multiplier as compared with 60 adders and 64 multipliers for previous 16-tap FIR filter algorithm

### C. Synthesis Utilization

Device utilization summary for FIR filter using DA technique are shown in table IV respectively. It is observed from the table that the processing unit for FIR filter using DA technique uses 5736 number of slice, 154 number of slice flip flop, 10566 number of LUTs, 2.187 ns minimum period and 457.247 MHz maximum frequency for Spartan-3 device family. It is similarly that the processing unit for FIR filter using DA technique uses 5736 number of slice, 154 number of slice flip flop, 10566 number of LUTs, 1.298 ns minimum period and 770.416 MHz maximum frequency for vertex-2p device family.

### D. Comparison Result

As shown in table V the maximum frequency and number of slice result are obtained for the proposed FIR filter using DA algorithm and previous algorithm. From the analysis of the results, it is found that the proposed FIR filter using DA algorithm gives a superior performance as compared with previous algorithm.

Figure 6 and figure 7 shows the graphical illustration of the performance of proposed method discussed in this research work in term of maximum frequency and number of slice. From the above graphical representation it can be inferred that the proposed algorithm gives the best performance as compared with previous algorithm.

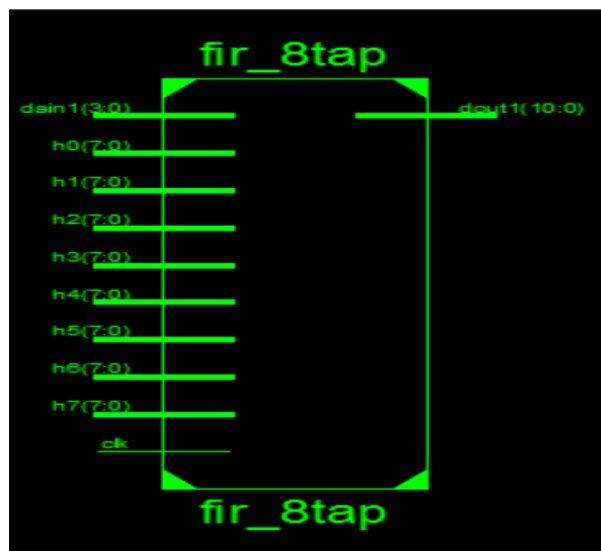


Figure 3: View Technology Schematic of 8-tap FIR Filter using DA Technique

Figure 3 shows the view technology schematic of 8-tap FIR filter using distributed arithmetic technique. In this figure, 'dain' is the input of the 8-tap FIR filter using distributed arithmetic technique, 'h0, h1, h2, h3, h4, h5, h6, h7' are the input of the 8-tap FIR filter using distributed arithmetic technique and 'dout' is the output of the 8-tap FIR filter using distributed arithmetic. Figure 4 shows the resistor transfer level of the 8-tap FIR filter using distributed arithmetic technique.

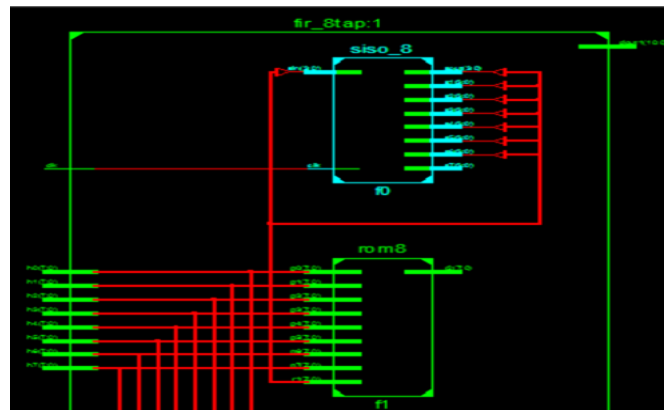


Figure 4: RTL View of 8-tap FIR Filter using DA Technique

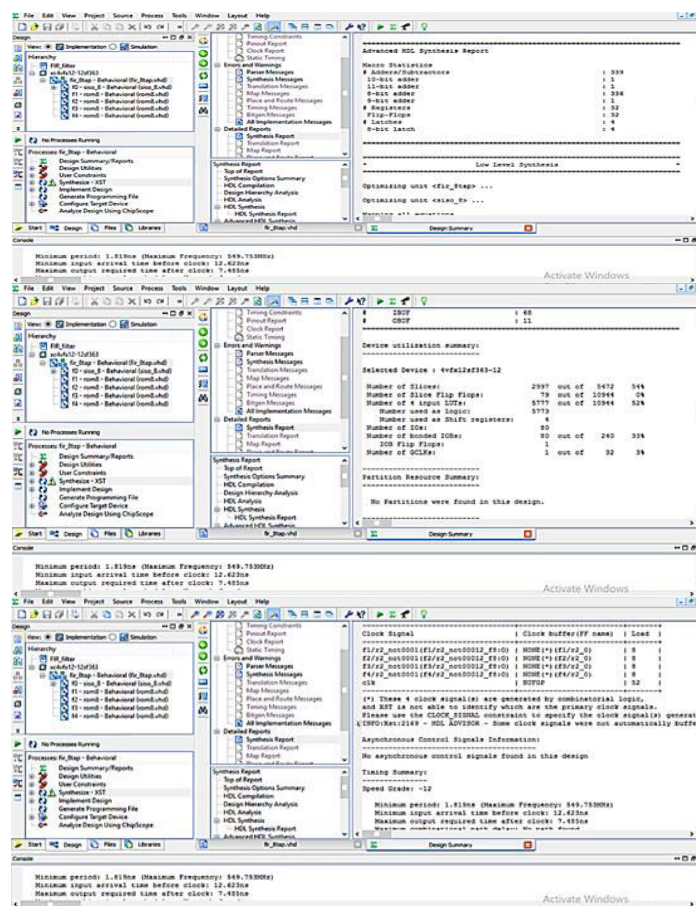


Figure 5: HDL Synthesis Report of 8-tap FIR Filter using DA Technique

## V. CONCLUSION

Distributed Arithmetic (DA) based Reconfigurable FIR filter has been introducing to provide more configuration and performance improvement. DA based architecture is called as "Multiplier-less" architecture in which LUT is used to store the filter coefficient values. Bi-Recorder based Reconfigurable Partial Product Generation (RPPG) unit is designed to change filter coefficients continuously. Reduced Wallace Tree Generation (RWTG) and Reduced Wallace Tree Reduction (RWTR) processes are used to performing partial product calculation. Further to add two binary results, modified carry save adder based partial product addition process is used in the current research work. FIR filter designed using high level system tools, shows that Verilog based filter design is better for low cost FPGA applications. System generator based FIR filter design works for high speed FPGA applications. Hence for low area designs, VHDL

based design is better than System generator design. From the analysis of the results, it is found that the proposed FIR filter using DA algorithm gives a superior performance as compared with previous algorithm.

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