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DEBAM: Decoder-Based Approximate Multiplier for Low Power Application

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A B S T R A C T: Approximate computing is a promising method for designing power-efficient computing systems. Many image and compression algorithms are inherently error-tolerant and can allow errors up to a specific limit. In such algorithms, savings in power can be achieved by approximating the data path units, such as a Multiplier. a novel decoder logic-based Multiplier design with the intent to reduce the partial products generated. Thus, leading to a reduction in the hardware complexity and power consumption while maintaining a low error rate. Our proposed design

KEYWORDS: ASIC Application Specific Integrated Circuit ISE Integrated Synthesis Environment

I. LITERATURE REVIEW

1) **“A low-power, high-performance approximate Multiplier with configurable partial error recovery”**, Title: C. Liu, J. Han, and F. Lombardi, in Proc. Conf. Design, Autom. Test Eur., Mar. 2014, Art. No. 95.

Here presents, a novel approximate Multiplier design is proposed using a simple, yet fast approximate adder. This newly designed adder can process data in parallel by cutting the carry propagation chain (and thus, introducing an error). It has a critical path delay that is even shorter than a conventional one-bit full adder. In a simple tree of the approximate adders is used for partial product accumulation and the error signals are used to compensate the error for obtaining a better accuracy. Compared to the traditional (exact) Wallace and Dada trees, the proposed Multiplier has a significantly shorter critical path as well as a reduced circuit complexity.

2) **“Energy-efficient approximate multiplication for digital signal processing and classification applications,”** IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1180–1184, Jun. 2015

Energy efficiency of multiplication is a critical objective. Since many digital applications use fixed-point arithmetic, it exhibits tolerance for computational errors. In this project, a Multiplier is proposed that can trade off computational accuracy with energy consumption. In this technique performs approximate multiplication exploiting significant segments of operands unlike the existing techniques such as aggressive voltage scaling; truncation of bit-width and use of inaccurate building blocks for approximate multiplication.

2) **“DRUM: A dynamic range unbiased Multiplier for approximate applications,”** Title: S. Hashemi, R. I. Bahar, and S. Reda, in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Nov. 2015, pp. 418–425.

Here presents, a novel Dynamic Range Unbiased Multiplier (DRUM) for approximate applications. The dynamic nature of our design enables the Multiplier to “zoom in” on the most significant digits of the numbers, all while making the Multiplier highly scalable and configurable. Since a typical computation involves a large number of multiplications, the unbiased nature of our Multiplier leads to near-zero average error. As a result, our unbiased design promotes errors to cancel each other rather than accumulate in the final result of the computation. The configurable aspect of our design enables smooth trade-off between accuracy loss and power consumption based on the designer’s priorities. Furthermore, our approximate design utilizes a core accurate Multiplier that is smaller in size than the full Multiplier. Thus, designers can still use their preferred Multiplier design for the core component with no need for sacrificing typical design practices.

3) **“MACACO: Modeling and analysis of circuits for approximate computing,”** Title: R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan,

in Proc. IEEE/ACM Int. Conf. Comput.-Aided Design, Nov. 2011, pp. 667–673.

In this technique, a range of implementations of common arithmetic units. In the case of adders, which are the most fundamental building block, we evaluate the behavior of three different conventional architectures under voltage over-



scaling - ripple carry adder, carry look-ahead adder, and Han-Carlson adder. We also evaluate three architectures that are specifically designed for approximate computing, based on dynamic segmentation with error compensation, reverse carry propagation, and truth table based approximation. Our results reveal interesting insights into the behavior of these approximate arithmetic units and the trade-offs between them. For example, our analysis identifies that functional correlation between the output bits reduces the maximum error introduced by over-scaling, explaining the empirical observation that the average case error in practice is much smaller than the worst-case. For some designs, we also observe that voltage over-scaling introduces errors of certain specific values much more frequently than others, leading to the possibility of low-complexity error detection and correction. We believe that systematic analysis frameworks such as the one proposed in this paper can significantly facilitate the adoption of approximate computing techniques.

4) “IMPACT: Imprecise adders for low-power approximate computing,”

Title: V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, in Proc. Int. Symp. Low Power Electron. Design, Aug. 2011, pp. 409–414. In this proposed work several imprecise or approximate FA cells that can be effectively utilized to build multi-bit arithmetic units and trade off power, area and quality for error resilient DSP systems. Our approach aims to simplify the complexity of a conventional mirror adder cell by reducing the number of transistors and also the load capacitances. When the errors introduced by these approximations are reflected at a high level in a typical DSP algorithm, the impact on output quality is almost negligible. Thus our approach differs from previous approaches where errors are introduced due to VOS. A decrease in the effective switched capacitance results in a lower power dissipation. Moreover, the proposed approximate FA cells also allow the system to operate at a lower supply voltage than the conventional case. This further contributes to a quadratic reduction in power dissipation.

MODEL SIM:

Modelsim is a hardware simulation and debug environment primarily targeted at smaller ASIC and FPGA design. Modelsim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Comprehensive support of Verilog, SystemVerilog for Design, and SystemC provide a solid foundation for single and multi-language design verification environments. Modelsim easy to use and unified debug and simulation environment provide today’s FPGA designers both the advanced capabilities that they are growing to need and the environment that makes their work productive. Modelsim is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed language designs.

.WORKING STEPS FOR MODELSIM:

1. Click the modelsim icon.
2. File -> New -> project -> browse the project location -> enter the project name. (The project created with the name what you have created).
3. Right click the workspace window to add the project file to project (Rightclick -> add -> add existing file -> add the files (by browse)).
4. Right click the workspace -> compile -> compile all.
5. Select library (below in workspace), open the work package and double click the file to be compiled for simulation process).
6. After simulating that file, it will create the simulation window (as sim).
7. In waveform right click the operand and force the value. For clock input, right click the clock operand and give the value (by clicking clock in the option).
8. Finally run the waveform and view the response.

Accuracy Analysis

For analysis, all the 8-bit and 16-bit Multipliers schemes, including the proposed one, have been modeled structurally using Verilog hardware description language (HDL).



The below table shown in 5.1 indicates power to delay product comparison

Table 5.1 Result Comparison

S.No	Existing Method	Proposed Method
1	22.3 PDP	20.7 PDP

II. CONCLUSIONS

Approximate computing offers potential benefits in terms of area, delay, and power. This letter attempts to leverage the inherent error-resilient characteristic in the image processing applications. The proposed DeBAM(N,M) architecture reduces the number of PPS generated, as a result, also simplifies the PP accumulation stage. Error and hardware results prove the energy and area efficacy of the proposed Multiplier compared to the existing designs. Finally, the proposed method achieves a better computation quality-effort trade off and the same is demonstrated on the image sharpening and compression algorithms.

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