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Simulation of SEPIC-CHMLI based micro inverter for high step-up voltage conversion

M.Ram kumar[1], I.Sayed mohammed [2] , J.Manikanda prashath[3]

P.G. Student, Department of Electrical Engineering, PSNA Engineering College, Dindigul, Tamilnadu, India[1]

Assistant Professor, Department of Elecrical Engineering, PSNA Engineering College, Dindigul, Tamilnadu, India[2]

U.G. Student, Department of Electrical Engineering, PSNA Engineering College, Dindigul, Tamilnadu, India[3]

Abstract: Within the photovoltaic power-generation market, the ac PV module has shown obvious growth. This paper proposes an implementation of Single Ended Primary Inductor (SEPIC) converter and cascaded multi level inverter for an AC load using Photovoltaic energy as a source. This paper proposes a converter that employs a continuous-conduction-mode SEPIC converter with low reverse-recovery loss. To convert the boosted DC output voltage from PV module into AC, a cascaded multi level inverter with multi carrier pulse width modulation is implemented. An operation principle and a detailed analysis of the proposed converter are presented. A 12V input voltage, (220-230)V output voltage of the proposed converter has been implemented. The simulation work of these SEPIC converter and cascaded multi level inverter fed RL load have been done using MATLAB software.

Keywords:PV cell, SEPIC converter, cascade multilevel inverter, multi carrier PWM

I. INTRODUCTION

Thephotovoltaic energy system has the advantages of absence of fuel cost, no environmental impacts, low maintenance and lack of noise and also it is a kind of renewable energy system. So it is becoming popular in the recent years, as a resource of energy. Modelling and simulation of PV array based on circuit model and a mathematical equation is proposed [9]. As the photovoltaic (PV) cell exhibits the nonlinear behaviour, while matching the load to the photovoltaic modules, DC-DC power converters are needed. There are several converter configurations such as Buck, Boost, Buck-Boost, SEPIC, ĆUK, Fly-back, etc. Buck and Boost configurations can decrease and increase the output voltages respectively, while the others can do both functions. Buck, Boost, Buck Boost converters as interface circuits are proposed and analyzed in [6]. CUK and SEPIC converters are analyzed in [1,7].the SEPIC converter should operate with high switching frequency. However, as the switching frequency increases, the reverse recovery current of the output diode affects the switching devices in the form of additional switching losses. Other adverse effects of the reverse-recovery problem include electromagnetic interference (EMI) noises and additional thermal management. Also, the switch utilisation factor in the SEPIC converter is much lower than that of other topologies, such as the buck and boost converters. In other words, the power-handling capabilities of the semiconductor devices in the SEPIC converter are much lower than those of the buck or the boost converter at the same power level. Thus, the reduction of reverse-recovery loss is particularly important for the SEPIC converter.

Different topologies MLIs for the conversion from DC to AC are available such as Neutral point clamped MLI (NPC-MLI), Flying capacitor MLI (FC-MLI), Cascade H-Bridge MLI (CHB-MLI) and Asymmetrical Cascade H-Bridge Multilevel inverters. Among them CHB-MLIs are mostly used for PV applications because each cell of CHB-MLI requires separate DC sources which can be easily supplied by individual PV arrays and each H-Bridge cell will be available in a single module**6**. The number of levels of the output wave form increased by cascading the no. of H-Bridge cells. There is a large no. of control techniques developed so far to control the operation of multilevel inverters such as SVPWM, SPWM, OHPWM, SHE-PWM, Hybrid modulation.

In these techniques SPWM is the easy to increase the number of levels in the output waveform with lower harmonic content. In SPWM control technique the gate pulses generated by comparing the sinusoidal reference waveform with the Triangular carrier waveforms. This paper presents the simulation results of a 5-level CHB-MLI with multi carrier PWM control techniques for PV applications. The function of an inverter is to change a dc input voltage to a symmetric

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AC output voltage of desired magnitude and frequency. To drive the AC load, the output dc voltage of SEPIC converter is converted into AC by means ofcascade multilevel inverter.In this paper PV source fed AC load is proposed with SEPIC converter and cascade multilevel inverter as interface circuits. Multi carrier pulse width modulation technique is employed for the control of cascade multilevel inverter. The overall block diagram is shown in Fig.1

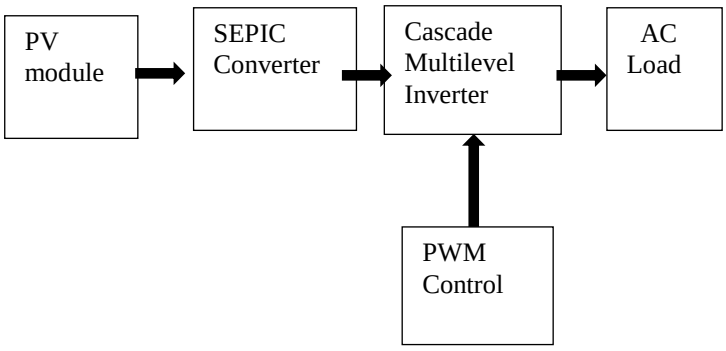

Fig.1 Over all block diagram

II. ANALYSIS OF SEPIC CONVERTER AND PV CELL

PV system directly converts sunlight into electricity. The basic device of a PV system is the PV cell. Cells may be gathered to form modules or arrays. More sophisticated applications require DC-DC converters to process the electricity from the PV device. These converters may be used to either increase or decrease the PV system voltage at the load. The proposed SEPIC converter operates in boost mode.

A. *PV Module Characteristics:*

The practical equivalent circuit of a PV module is shown in Fig.2

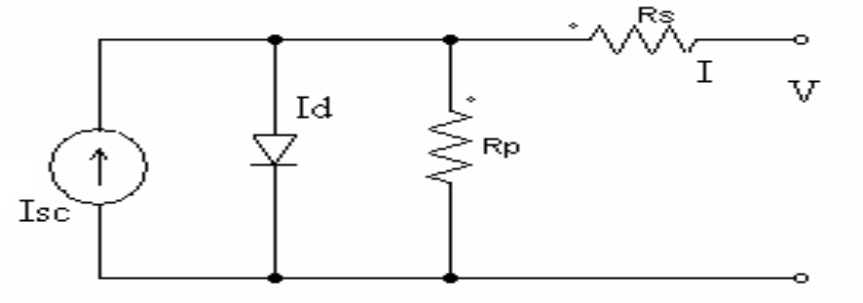

Fig. 2 Equivalent circuit of a PV module

In the equivalent circuit, the current source represents the current generated by light photons and its output is constant under constant temperature and constant irradiance. The diode shunted with the current source determines the I-V characteristics of PV module. There is a series of resistance in a current path through the semiconductor material, the metal grid, contacts, and a current collecting bus. These resistive losses are lumped together as a series resistor (*Rs*). Its effect becomes very noteworthy in a PV module.

The loss associated with a small leakage of current through a resistive path in parallel with the intrinsic device is represented by a parallel resistor (*Rp*). Its effect is much less noteworthy in a PV module compared to the series resistance, and it will only become noticeable when a number of PV modules are connected in parallel for a larger system. The characteristic equation which represents the I-V characteristic of a practical photovoltaic module is given below

$$I = I_{pv} - I_0 \left[\exp\left(\frac{V + IR_S}{V_T n}\right) - 1\right] - \frac{V + IR_S}{R_P} \qquad (1)$$

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Where I and V are the PV cell current and voltage respectively, IPV is the photovoltaic current, Io is the reverse saturation current of diode, Vt= Ns*kT/q is the thermal voltage of the array with Ns cells connected in series, k is the Boltzmann constant (1.3806*10-23J/K), T is the temperature of the p-n junction, q is the electron charge and n is the diode is constant. I_{PV} and I_O are given as follows

$$I_{pv} = \{[1 + a(T - T_{ref}]I_{sc}\}\left[\frac{G}{1000}\right] \quad (2)$$

$$I = I_o(T_{ref}) \quad (3)$$

Where "a" is temperature coefficient of I_{sc}, G is the given irradiance in W/m2 and Egis the band gap energy (1.16eV for Si)

A. Design of SEPIC Converter:

1) Introduction:

Using a coupled inductor takes up less space on the PCB and tends to be lower cost than two separate inductors. The capacitor Cs isolates the input from the output and provides protection against a shorted load.

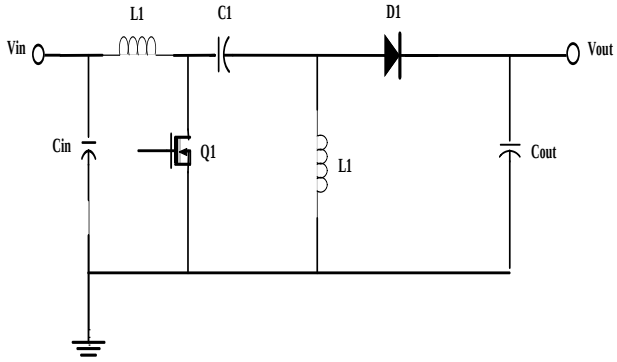
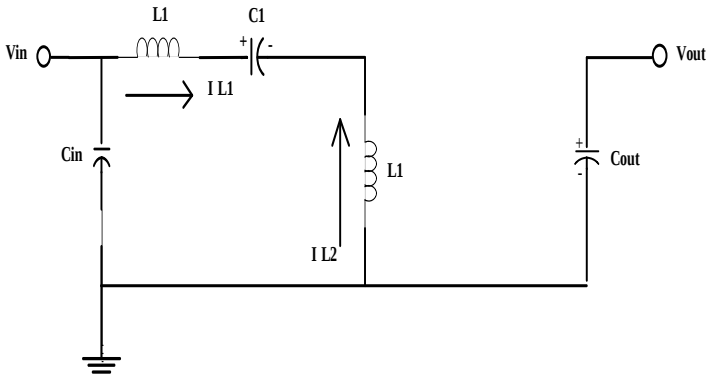


Fig.3 SEPIC Topology



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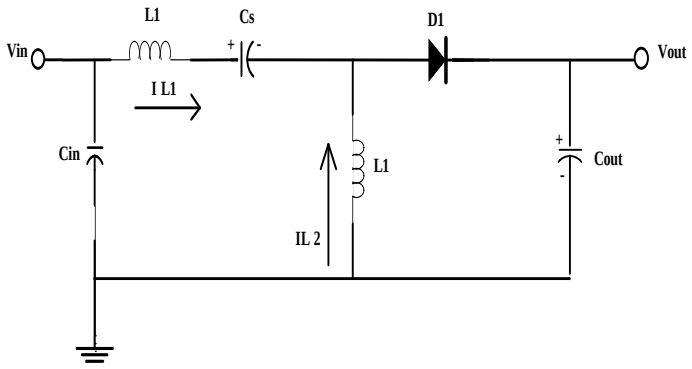

Fig.4 SEPIC Converter Current Flow
Top: During Q1 On-Time, Bottom: During Q1 Off-Time

2) Duty Cycle Consideration:

For a SEPIC converter operating in a continuous conduction mode(CCM),the duty cycle is given by:

$$Duty\ cycle(D) = V_{out} + V_D/V_{in} + V_{out} + V_D \qquad (4)$$

V_D is the forward voltage drop of the diode D_1.The maximum duty cycle is given by

$$D_{max} = V_{out} + V_D/V_{in(min)} + V_{out} + V_D \ (5)$$

3) Inductor Selection:

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_{in} \times 40\% = \frac{I_{out} \times V_{out}}{V_{in(\min)}} \times 40\% \qquad (6)$$

The inductor value is calculated by:

$$L1 = L2 = L = \frac{V_{in(\min)}}{\Delta I_L \times f_{sw}} \times D_{(\max)} \qquad (7)$$

Where,f_{sw} is the switching frequency and $D_{(\max)}$ is the duty cycle at the minimum. The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1(peak)} = I_{out} \times \frac{V_{out} \times V_D}{V_{in(\min)}} \times (1 + 40\%/2) \qquad (8)$$

$$I_{L2(peak)} = I_{out} \times (1 + 40\%/2) \qquad (9)$$

If L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by:

$$L1' = L2' = \frac{L}{2} = \frac{V_{in(\min)}}{2 \times \Delta I_L \times f_{sw}} \times D_{(\max)} \qquad (10)$$

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4) Power MOSFET Selection:

The parameters governing the selection of the MOSFET are the minimum threshold voltage V th (min), the on resistance RDS (ON), gate-drain charge QGD, and the maximum drain to source voltage, VDS(max). Logic level or sub logic-level threshold MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to $V_{in}+V_{out}$. The peak switch current is given by:

$$I_{Q1(peak)} = I_{L1(peak)} + I_{L2(peak)} \qquad (11)$$

The RMS current through the switch is given by:

$$I_{Q1(rms)} = I_{out}\sqrt{\frac{(V_{out}+V_{in(\min)}+V_D)\times(V_{out}+V_D)}{V^2_{in(\min)}}} \qquad (12)$$

The MOSFET power dissipation P_{Q1} is approximately:

$$P_{Q1} = I_{Q1(rms)} \times R_{DS(ON)} \times D_{max} + \left(V_{in(\min)} + V_{out}\right) \times I_{Q1(peak)} \times Q_{GD} \times \frac{f_{sw}}{I_G} \qquad (13)$$

P_{Q1}, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. IG is the gate drive current. The $R_{DS(ON)}$ value should be selected at maximum operating junction temperature and is typically given in the MOSFET data sheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

5) Output Diode Selection:

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current IQ1(peak). The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1}=V_{in(\max)} + V_{out(\max)} \qquad (14)$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode.Schottky diodes are recommended in order to minimize the efficiency loss.

6) SEPIC Coupling Capacitor Selection:

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by:

$$I_{CS(\text{rms})} = I_{out} \times \sqrt{\frac{V_{out} + V_D}{V_{in(min)}}} \qquad (15)$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating. The peak-to-peak ripple voltage onC_s (assuming no ESR):

$$\Delta V_{cs} = \frac{I_{out} \times D_{max}}{C_s \times f_{sw}} \qquad (16)$$

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A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on C_s.Hence, the peak voltage is typically close to the input voltage.

7) Output Capacitor Selection:

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor must be capable of handling the maximum RMS current. The RMS Current in the output capacitor is:

$$I_{Cout(\text{rms})} = I_{out} \times \sqrt{\frac{V_{out} + V_D}{V_{in(min)}}} \qquad (17)$$

TheESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. we assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence,

$$ESR \leq \frac{V_{ripple} \times 0.5}{I_{L1(peak)} + I_{L2(peak)}}$$

$$C_{out} \geq \frac{V_{out} \times D}{V_{ripple} \times 0.5 \times f_{sw}}$$

The output capacitor must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

8) Input Capacitor Selection:

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{c\,in(rms)} = \frac{\Delta I_L}{\sqrt{12}} \qquad (18)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 µF or higher value, good quality capacitor would prevent impedance interactions with the input supply.

III. SIMULATION RESULTS FOR SEPIC CONVERTER

This converter Fig. 5 has two inductors and two capacitors. The capacitor C1 provides the isolation between input and output. The SEPIC converter exchanges energy between the capacitors and inductors in order to convert the voltage from one level to another. The amount of energy exchanged is controlled by switch, which is typically a transistor such as a MOSFET.

The MATLAB simulation model of SEPIC output voltage waveform is shown in Fig. 6.

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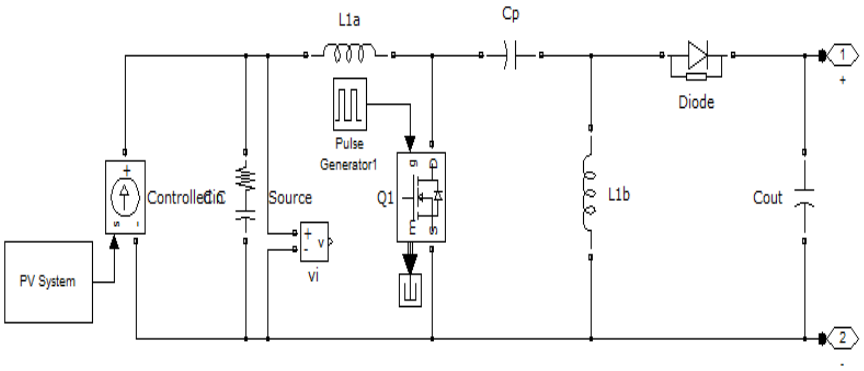

Fig.5 SIMULINK model for SEPIC converter

The duty cycle D can be determined from the steady state condition and the following equation is true:

$$\frac{I_{L1}}{I_{L2}} = \frac{D}{1-D} = \frac{I_{in}}{I_O} \qquad (19)$$

$$P_{in} = P_O \qquad (20)$$

$$V_{in}I_{in} = V_O I_o \qquad (21)$$

the relationship between input and output voltage is:

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \qquad (22)$$

The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated. In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages.

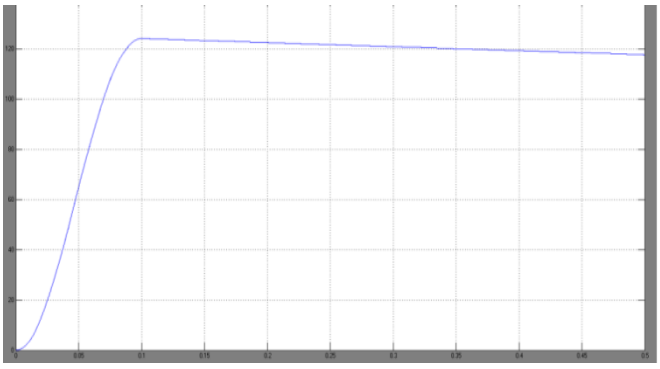

Fig .6 SIMULINK model for SEPIC converter(110V)

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In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H-bridge cell may have positive, negative or zero voltage.Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is five. Cascaded H-bridge five level inverters typically use IGBT switches. These switches have low block voltage and high switching frequency.The MATLAB simulation model of SEPIC converter and CHMLI fed RL load is shown in Fig .7

TABLE-I:SWITCHING TABLE FOR 5-LEVEL CHB INVERTER

Switches Turn On	**Voltage level**
S1,S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

The SEPIC converter output is a boosted DC voltage of PV module output. The output of the SEPIC converter is fed to the cascade multi level inverter . The magnitude of the output voltage of the inverter is controlled by the amplitude of the reference sine wave and hence the amplitude modulation index. The frequency of the inverter output voltage is controlled by the frequency of the reference signal. The current output of the inverter is dependent on the load impedance. The controlledmagnitude and frequency of the inverter output voltage is(220-230v)given to AC load. Finally the voltage of the AC load is measured for the given irradiance and temperature.

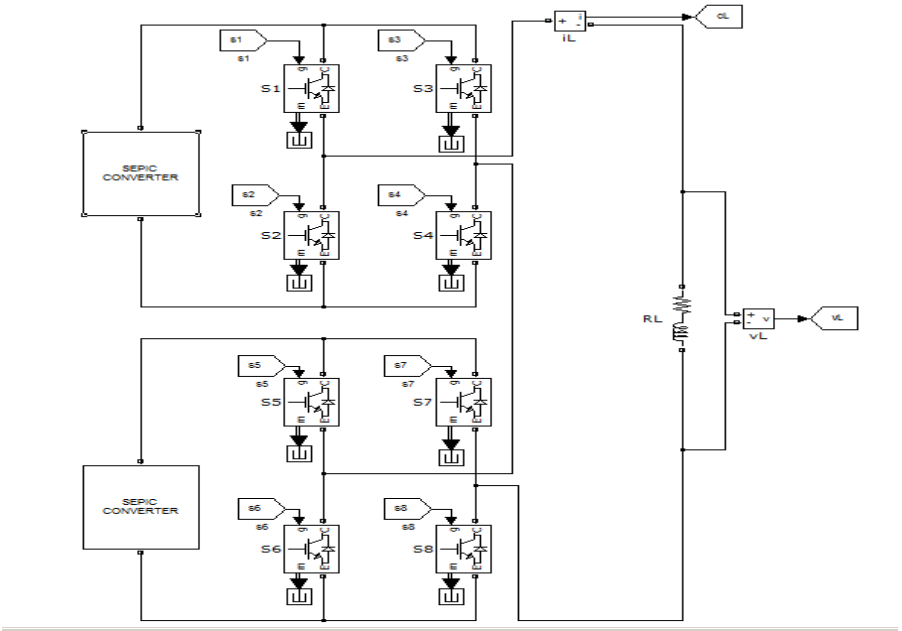

Fig. 7 SIMULINK model for SEPIC&CHMLI

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The MATLAB simulation model of CHMLI output voltage and output current waveform is shown in Fig. 8 and Fig. 9

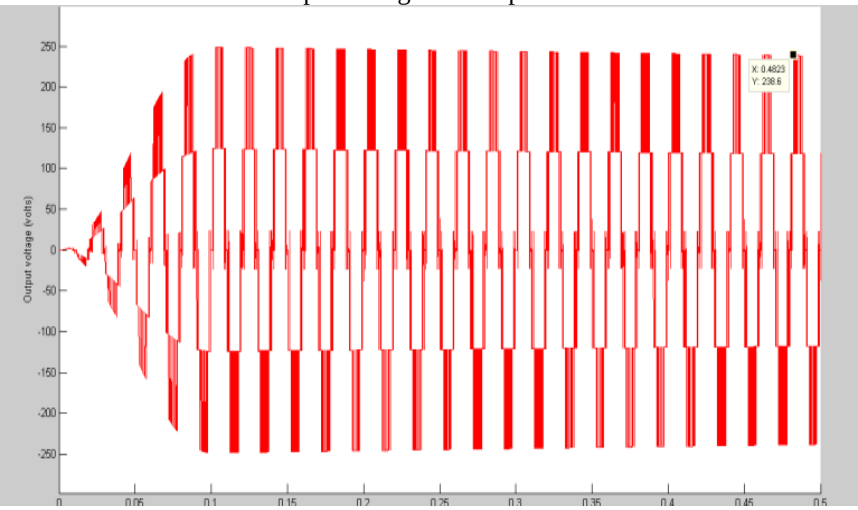

Fig. 8 Output voltage(230V) waveform for CHMLI inverter

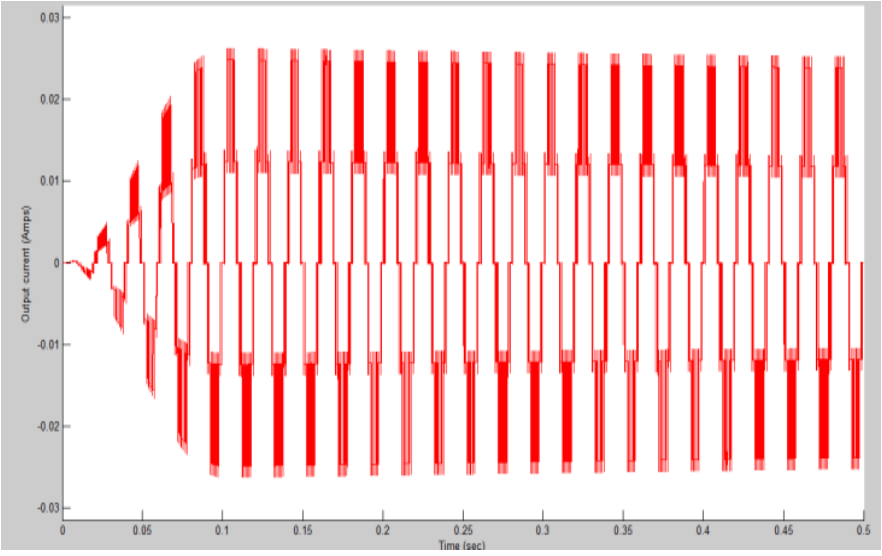

Fig. 9 Output current waveform for CHMLI inverter

IV. CONCLUSION

This paper presented the simulation work of a Photovoltaic array feeding a RL load. SEPIC converter and cascade 5 level inverter were used as interface between PV module and the RL load. The voltage level of the PV panel is improved using SEPIC converter &cascade h-bridge multilevel inverter. The simulation works of these circuits were carried out in the MATLAB software. The proposed SEPIC&CHMLI inverter is to reduce both voltage & current THD of the inverter. The 230v output voltage is obtained with above proposed topology in simulation. The boosted DC voltage of the SEPIC converter circuit output and inverted AC output waveforms were shown in the results.

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