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Implementation of Prescaler in Communication System

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ABSTRACT: Prescaler is an electronic counting circuit used to reduce a high frequency electrical signal to a lower frequency by integer division. Prescaler can be used in communication to provide different frequencies from a single source for different users. So we can avoid the usage of different clock sources to provide access for users, their by reducing the power consumption. In order to understand this concept simple divide-by-16 Prescaler is designed for Convolution encoder and OFDM operates at the main clock source frequency. OFDM designed here effectively mitigates the ISI caused by delay spread of channels. So it is widely used multiplexing technique for communication. Convolution encoding is one of the good encoding techniques in telecommunication for transmitting digital signals without error. This is coded in verilog HDL, simulated on modelsim6.3f and implemented on Vertex-5 FPGA.

KEYWORDS: Prescaler, OFDM–Orthogonal frequency division multiplexing, Convolution encoder.

I. INTRODUCTION

Prescaler has become one of the important devices to increase the operating frequency of the device and to reduce power consumption. As in the case of PLL and frequency synthesizers prescalers are used to get better performance of that. Prescalers can also be of dual-modulus type which will operate in one of the mode depending on the control signal given. On the other side we can use these prescalers as counters for timing devices. It means we can use that to obtain different frequencies from the available in order to run different applications operating on those frequencies, eg. In communication system we will be providing certain frequency for particular user with the usage of a clock source. Next to provide another frequency for other user we need to use different clock source which will be fixed only for that particular user if he is not using currently also. Using as many sources as there is a user leads to a more power consumption, one way to avoid this power consumption is to use a prescaler between user to provide different frequencies, their by avoiding number of clock sources needed.

In digital communication system, error detection and error correction is important for reliable communication. Error detection techniques are much simpler than Forward error correction (FEC). But error detection techniques have certain disadvantages. Error detection pre supposes the existence of an automatic repeat request (ARQ) feature which provides for retransmission of those blocks, segments or packets in which errors have been detected. This assumes some protocol for reserving time for retransmission of such erroneous blocks and for reinserting the corrected version in proper sequence. It also assumes sufficient overall delay and corresponding buffering that will permit such reinsertion.

An additional drawback of error detection with ARQ is its inefficiency at or near the system noise threshold. For, as the error rate approaches the packet length, the majority of blocks will contain detected errors and hence require retransmission, even several times, reducing the throughput drastically. In such case, forward error correction may considerably improve throughput. Froward error correction may be desirable in place of error detection for any of the following reasons:

- When a reverse channel is not available or the delay with ARQ would be expensive.
- The retransmission strategy is not conveniently implemented.



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Since errors are possible in communication channels during the data transmissions, we must apply error correcting codes to combat these errors. The purpose of forward error correction (FEC) is to improve the capacity of the channel by adding some carefully designed redundant information to the data being transmitted through the channel. The process of adding this redundant information is known as channel coding.

Orthogonal frequency division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. OFDM has developed into a popular scheme for wideband digital communication, whether wireless or over copper wires, used in applications such as digital television and audio broadcasting, DSL Internet access, wireless networks, power line networks, and 4G mobile communications.

Fig.1 shows the main module of project. Here a efficient OFDM is designed for a single data transmitted bit which minimises the occurrence of ISI in channel. Convolution encoder designed here for 1/3 code rate operating on the prescaler outputted frequency.



Fig.1: Main module of project

II. RELATED WORKS

The history of OFDM dares back to mid 60's, [1] presents a principle for transmitting messages simultaneously through linear band limited channel without ICI and ISI. A major contribution was given by [2] used the DFT to perform baseband modulation and demodulation. Another contribution was done in [3], introduced the cyclic prefix (CP) or cyclic extension for solving orthogonality problem. Instead of using an empty guard space, they filled a guard space with a cyclic extension of the OFDM symbol. This introduces energy loss proportional to the length of the CP, but the zero ICI generally motivates the loss. By referring [4] different approaches of error control techniques, fundamentals of coding and applications can be known. The limitation is that the mathematics behind error correction can be extremely intensive. By referring [5] we can know the fundamental tools and methodologies used in the analysis and design of modern communication systems. The authors emphasize digital communication systems is the backbone of modern communication systems, including new generations of wireless communication systems. In [6] described the Viterbi decoder as best method for decoding the Convolutional codes and designed it using Register exchange method, which consumes more area.

III. OFDM

Orthogonal frequency division multiplexing (OFDM) is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower rate subcarriers. The main reason to use OFDM is to increase the robustness against the selective fading or narrowband interference. In single carrier system if signal get fade or interfered then entire link gets failed where as in multicarrier system only a small percentage of the subcarriers will be affected. The total signal bandwidth, in a classical parallel data system, can be divided into N non-overlapping frequency sub-channels. Each sub-channel is modulated a separate symbol and then N sub-channels are frequency multiplexed. The general practice of avoiding spectral overlap of sub-channels was applied to eliminate inter-carrier-interference (ICI). This resulted in insufficient utilization of the existing spectrum. An idea was proposed in the mid 1960s to deal with this wastefulness through the development of frequency division multiplexing (FDM) with overlapping sub-channels. The sub-channels were arranged so that the sidebands of the individual carriers overlap without causing ICI. To achieve this, the carriers must be mathematically orthogonal. From this constraint the idea of orthogonal frequency division multiplexing was born. OFDM is a combination of modulation and multiplexing. Multiplexing generally refers to independent signals, those produced by different sources. In OFDM the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is

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a special case of frequency division multiplexing (FDM). OFDM transmitter and receiver designed in this paper is as shown in fig.2 and fig.3. Puncturing step introduced in this paper helps to remove redundant bits. Modulator and 128bit QAM designed effectively helps in avoiding ICI and ISI. Also the Adaptive Viterbi decoder will decodes data with less power consumption and less area.

A. OFDM Transmitter





1) Encoder: Convolution coding and Block coding are two major forms of channel coding. Block codes operate on relatively large message blocks. Convolution codes operate on serial data, one or a few bits at a time. Passing the information sequence to be transmitted through a linear finite shift register generates a convolution code. The shift register consists of k bit stages and n linear algebraic function generators. The contents of shift register are multiplied by respective term in generator matrix and are than added together to generate respective code words. There are four alternative methods that are often used to describe the convolution codes. These are the generator representation, tree diagram, state diagram and trellis diagram. Here code is obtained by generator representation at the code rate of 1/3.

2) *Puncturing:* Puncturing is the process of deleting some parity bits from the codeword according to a puncturing matrix. Puncturing is the trade off between rate and performance. Puncturing increases code rate without increasing complexity for code rate from 1/3 to 1/2 or more and decreases free distance of code. The redundant bits in code decrease the bandwidth efficiency. To achieve system requirement, the puncturing patterns will adjust code rate.

3) Interleaving: The reason why interleaving is used on OFDM is to attempt to spread the errors out in the bit-stream that is presented to the error correction decoder, because when such decoders are presented with a high concentration of errors the decoder is unable to correct all the bit errors, and a burst of uncorrected errors occurs. OFDM is invariably used in conjunction with channel coding (forward error correction), and almost always uses frequency and/or time interleaving. Frequency (subcarrier) interleaving increases resistance to frequency-selective channel conditions such as fading. For example, when a part of the channel bandwidth fades, frequency interleaving ensures that the bit errors that would result from those subcarriers in the faded part of the bandwidth are spread out in the bit-stream rather than being concentrated. Similarly, time interleaving ensures that bits that are originally close together in the bit-stream are transmitted far apart in time, thus mitigating against severe fading as would happen when travelling at high speed. We are used the frequency interleaving here.

4) *QAM Mapping:* Like all modulation schemes, QAM conveys data by changing some aspect of a carrier signal, or the carrier wave, in response to a data signal. In the case of QAM, the amplitude of two waves, 90° out-of-phase with each other (in quadrature) are changed to represent the data signal. Amplitude modulating two carriers in quadrature can be equivalently viewed as both amplitude modulating and phase modulating a single carrier. Here 16-QAM is designed in first quadrant of its constellation diagram.

5) Symbol generator: We used separate symbol generator for both 16-bit real and imaginary values obtained from QAM. It produces 64-bit symbols.



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6) Zero-padding and Cyclic-prefix: In order to avoid inter block interference (IBI) between OFDM blocks arising due to the frequency selective nature of the channel, either cyclic prefix (CP) or zero padding (ZP) is added to each OFDM block before transmission. The length of the CP/ZP should be longer than the channel delay profile to avoid IBI.

7) *Inverse Fast Fourier Transform (IFFT):* It is one of the important module and also critical to design. The IFFT input is from zero-padding. Here, we required two modules of IFFT for real and imaginary values. The IFFT converts the frequency domain symbols to time domain. These time domain symbols are cyclic prefixed and transmitted as OFDM signal, totally of 304-bits. The IFFT designed here is of 128-bit.

B. OFDM Receiver

1) Inverse Cyclic prefix: The first block in the receiver section, OFDM signal received from antenna is fed to this block. It removes the prefixed code from the transmitted data. It separates out the real and imaginary values.

2) Fast Fourier Transform (FFT): FFT is one of the main module in receiver section, it converts back the time domain signal to frequency domain.



Fig.3: OFDM Receiver

3) Inverse Zero-padding and Inverse Symbol generator: Inverse ZP will remove up the added zeroes, obtaining 64-bits of output. Then the Inverse Symbol Generator will decodes the symbol and produces 16-bits of real and imaginary values.

4) QAM-De mapping: Based on the 16-bit real and imaginary input from Inverse symbol generator 16-bit QAM demodulator will produces 4-bit demodulated output.

5) *De-Interleaving and De-Puncturing:* Frequency de-interleaving is performed and De-Puncturing is performed on the 3-bit data.

6) Adaptive Viterbi Decoder: Decoder is the most important block in receiver section. Adaptive Viterbi decoder is used for decoding codes of long constraint length, where as Viterbi decoder is used for decoding short constraint length codes. Also Adaptive Viterbi decoder consumes less power. Fig.4 shows the block diagram of Viterbi decoder. It consists of three main blocks: Branch Metric Calculation (BMC), Path Metric Calculation (PMC) and Survivor Management Unit (SMU).

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Fig.4: Basic building blocks of Viterbi Decoder

IV. EXPERIMENTAL RESULTS

The work presented in this paper is to show how prescaler can be used to get different frequencies in communication system for different users, in order reduce power consumption and necessity of different clock sources for providing various frequencies. Fig.5 shows the result of Prescaler, is designed as a divide-by-16.

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Fig.5: Simulation result of Prescaler

Fig 6 shows the output of main module, where the data inputted to OFDM transmitter will be encoded, interleaved at 50Hz and modulated by 16-bit QAM. 16-bit data is converted to 128-bit data using symbol generator and zero-padding. IFFT is performed on this data, and then transmitter output is obtained by performing cyclic-prefix, which effectively mitigates the ICI and ISI. So the transmitted data will be secured.



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Fig.6: Result of main module

V. CONCLUSION

Prescaler is designed for convolution encoder, OFDM design shown is one of the best method for data transmission in communication, has been designed using verilog HDL. Simulation using modelsim 6.3f is carried out to verify the design. In future Encoder and Viterbi decoder for higher constraint length can be implemented.

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