

DC Characterization of InAl_{0.7}As_{0.5}/InAl_{0.5}As_{0.5}/InP Based Pseudomorphic HEMT (pHEMT)

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ABSTRACT: The aim of this work is to investigate the impact of gate-length (L_g) and doping concentration (N_d) of the donor layer and its thickness (d_a) on the performance of double-gate InAl_{0.7}As_{0.3}/InAl_{0.5}As_{0.5}/InP HEMT. A comparison of the impact of donor-layer doping concentration, donor-layer thickness and gate-length on the channel current, trans conductance, gate-to source capacitance and cut-off frequency for the DG-HEMT has been studied with that for SG-HEMT. As a result of this comparison the DG-HEMT has been seen to exhibit more sensitivity to these device parameters. This is due to greater sheet carrier concentration and better gate-control. Thus, the optimization of the donor-layer doping, donor-layer thickness and gate-length in the case of DG-HEMT is crucial.

In double-gate high-electron-mobility transistor (DG-HEMT) with symmetrical epitaxial layer the different geometries of the gate (T-gate, IL-gate, Γ -gate, etc.) affects the high breakdown characteristics, modifies the trans-capacitance and gate resistance of the device thereby affecting the drain current and the RF performance cutoff frequency (f_T), and maximum frequency of oscillation (f_{max}). In this work, the double gate and the epitaxial structure is taken to be asymmetrical on both sides. In all the geometries of the gate (T-gate, IL-gate, Γ -gate, etc.), the base-gate length which is the lithography-defined gate length is same, and the variation is studied for the upper head of the structure and recess width, which can be extended toward the source or drain side of the gate.

I. INTRODUCTION

Rapid advancement in MMIC Technology and solid state transistor has given rise to the need for extremely high cut-off frequencies (f_T) and high maximum oscillation frequency (f_{max}) for various technologies. A maximum frequency of oscillation of above 1THz with maximum unilateral gain available at 1.2THz and maximum stable gain (MSG) at 1.1THz has already been reported for fabricated sub-50nm InAlAs/InAlAs/InP high electron mobility transistor. A quest to obtain even more superior ultrahigh-frequency and low-noise performance for future military communications, radar and intelligence applications has led to the shrinking of gate-lengths to below 50nm but at such small gate-lengths the device performance is seriously affected by the inevitable short channel effects which include the shift in the threshold voltage towards being more negative, larger sub-threshold slope and reduced transconductance. These short-channel effects can be minimized by making the lateral field much greater than the field in the longitudinal or the channel direction which is accomplished by increasing the donor-layer doping and reducing the donor layer thickness. However, mobility degradation, velocity-overshoot effect and gate leakage current imposes a fundamental limit on the increase in the doping concentration and reduction in the donor-layer thickness in a SG-HEMT. Further miniaturization for ultra high frequency and low-noise applications requires modification in the conventional structure. Thus, the need for the evolution of the standard HEMT design has led to the development of DG-HEMT structure based on transferred substrate technique in which two-gates are placed on each side of the conducting InGaAs channel. This innovative concept earlier employed for Transferred Substrate-HBT enables to eliminate dominant parasitics of the transistor and the suppression of carrier injection in the substrate. Fabricated 100nm Trenched gate DGHEMT have exhibited much superior high-frequency and low noise performance when compared with a conventional single-gate HEMT. In the present work, an accurate one dimensional charge control based model has been used to study the impact of various parameters (N_d , d_a , and L_g) on the input-characteristics (I_d - V_g s), drain

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characteristics (I_d - V_{ds}), transconductance (g_m), gate-source capacitance (C_{gs}) and cut-off frequency (f_T) of InAlAs/InGaAs/InP DG-HEMT as compared to the SG-HEMT. Since the ultimate speed of a switching device is determined by the transconductance divided by the sum of the gate and interconnect capacitances, the larger the transconductance, the higher is the speed. The increase in N_d to obtain improved transconductance must accompany reduction in d_a in order to maintain the threshold voltage of the device. But reduced d_a leads to reduced saturation current density and a greater gate-leakage current. Another parameter which greatly affects the dynamic performance of HEMT in terms of its transconductance is the gate-length (L_g). Reduced L_g also leads to improved transconductance. Thus, in order to obtain maximum current density and maximum transconductance from a device along with reduced short channel effects, a careful optimization of N_d , d_a and L_g is required which is shown to be even more crucial for a DG-HEMT in the following analysis. It is also seen that the increase in the C_{gs} for DG-HEMT which is expected to cause deterioration in f_T and hence the dynamic performance of the device is compensated by the increase in the transconductance which is attributed to the increased charge density in the two 2DEGs. Therefore, node gradation in f_T of DG-HEMT is observed.

A heterojunction is the interface that occurs between two layers or regions of dissimilar crystalline semiconductors. These semiconducting materials have unequal band gaps as opposed to a homojunction. It is often advantageous to engineer the electronic energy bands in many solid state device applications including semiconductor lasers, solar cells and transistors (heterotransistors) to name a few. The combination of multiple heterojunctions together in a device is called a heterostructure although the two terms are commonly used interchangeably. The requirement that each material be a semiconductor with unequal band gaps is somewhat loose especially on small length scales where electronic properties depend on spatial properties.

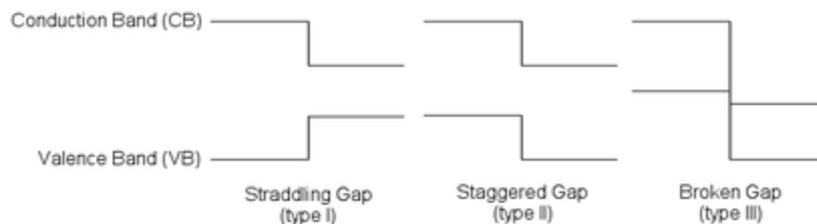


Fig. 1 The three types of semiconductor heterojunctions organized by band alignment.

A more modern definition may be to say that a heterojunction is the interface between any two solid-state materials including crystalline and amorphous structures of metallic, insulating, fast ion conductor and semiconducting material. To allow conduction, semiconductors are doped with impurities which donate mobile electrons (or holes). However, these electrons are slowed down through collisions with the impurities (dopant) used to generate them in the first place. HEMTs avoid this through the use of high mobility electrons generated using the heterojunction of a highly-doped wide bandgap n-type donor-supply layer and a non-doped narrow-bandgap channel layer with no dopant impurities.

II. OBJECTIVE

The objective of this project is to analysis the double gate high-electron-mobility transistor for different gate geometries to improve the DC characteristics and the RF performances and to further explored the effect of gate geometries.

1. To reduce short channel effect in the field of compound semiconductor device with the help of double gate HEMT.
2. To improve the RF performance with reduced parasitic capacitance
3. To analysis the better gate geometries using T-gate with reduced electric field at source and drain side.
4. To show the device modeling and TCAD simulations of $\text{InAl}_{0.7}\text{As}_{0.5}/\text{InAl}_{0.5}\text{As}_{0.5}/\text{InP}$ DG-HEMT to accurately match measured data.
5. To varying the doping concentration of donor layer, transconductance and cut of frequency.

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6. To demonstrate simulation TCAD AC analysis and RF simulations.
7. To improve the breakdown voltages and RF power handling capability.
8. To reduce the parasitic elements with the help of T-gate.
9. To improve the drain current and transconductance of the device
10. Investigate doping concentration, donor layer thickness, and gate length.

III. DISCUSSION

DC Characterization of InAl_{0.7}As_{0.5}/InA_{0.5}lAs_{0.5}/InPbased Pseudomorphic HEMT (pHEMT)

A symmetric DG-HEMT with tied-gate geometry is shown in fig.1 in which the doping profile, doping concentration, nature of the schottky-barrier and the dimensions of various layers in both the hetero structures is the same. The gates are tied together so that the voltage applied to both the gates become equal. This simplified model for DG-HEMT is employed for the purpose of investigating the effect of donor-layer doping, donor-layer thickness and gate-length on its dynamic performance. Thus, with regard to the dynamic behaviour of the device, the net device current can be taken to be almost twice that of a single channel as long as it is operated in the common mode. Based on these assumptions, expression for current and transconductance is derived for a DG InAl_{0.7}As_{0.5}/InA_{0.5}lAs_{0.5}/InP HEMT using an accurate one-dimensional charge control model based on linear velocity field relationship. The various structural and electrical parameters used in the analysis..HEMT was originally developed for high speed applications

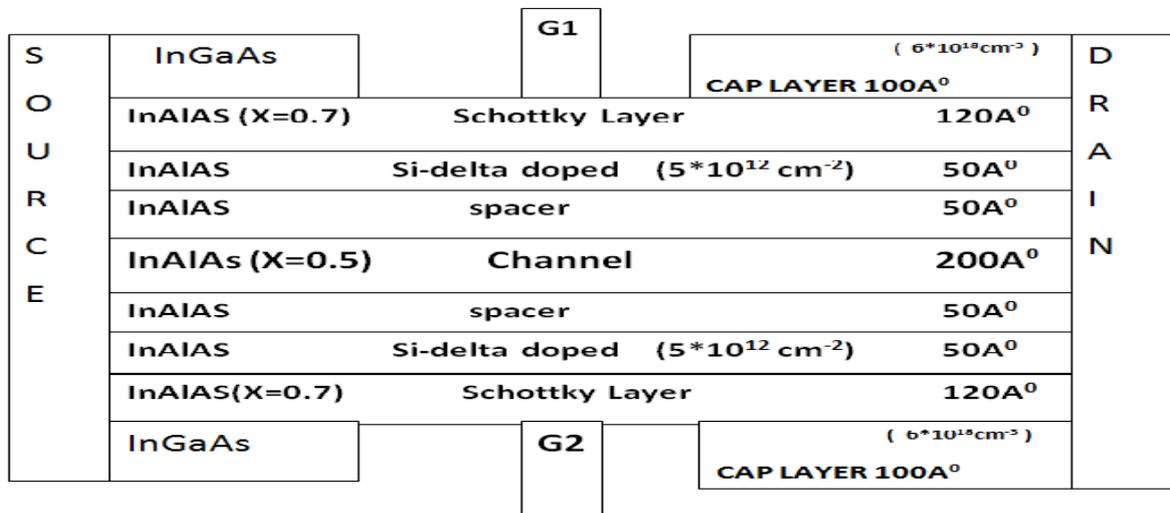


fig 4.1 schamatic of symmetric InAl_{0.7}As_{0.5}/InA_{0.5}lAs_{0.5} HEMT

The conduction-band diagram of symmetric DGInAlAs/InGaAs/InP HEMT with tied gate geometry is shown in Figure2. The dimensions of various layers are shown in fig.1 with L_g= 0.1 um. The current flowing through a single channel with sheet-carrier concentration n_s and width

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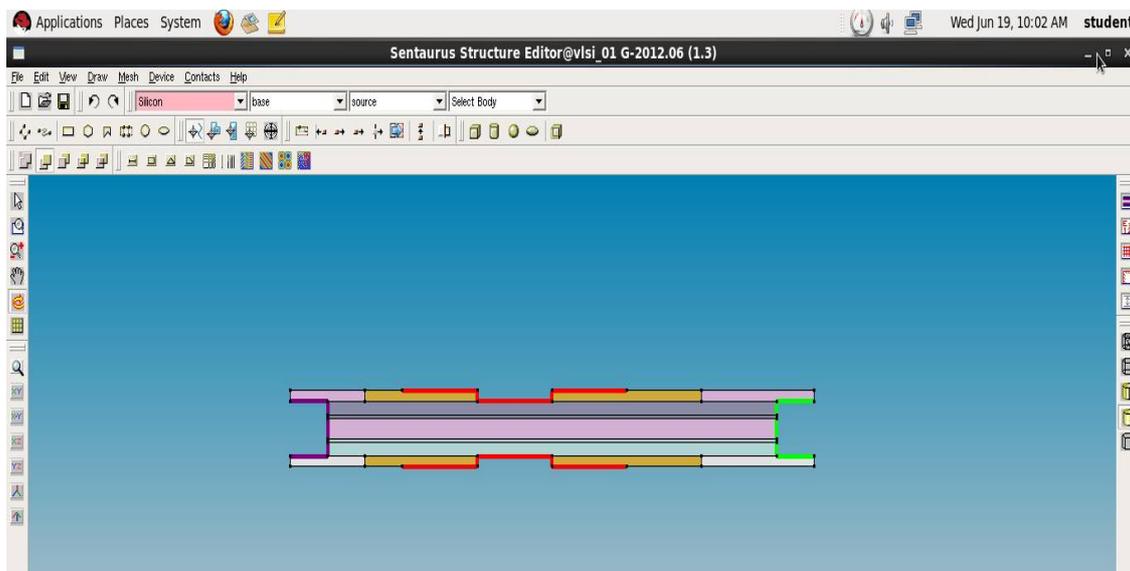


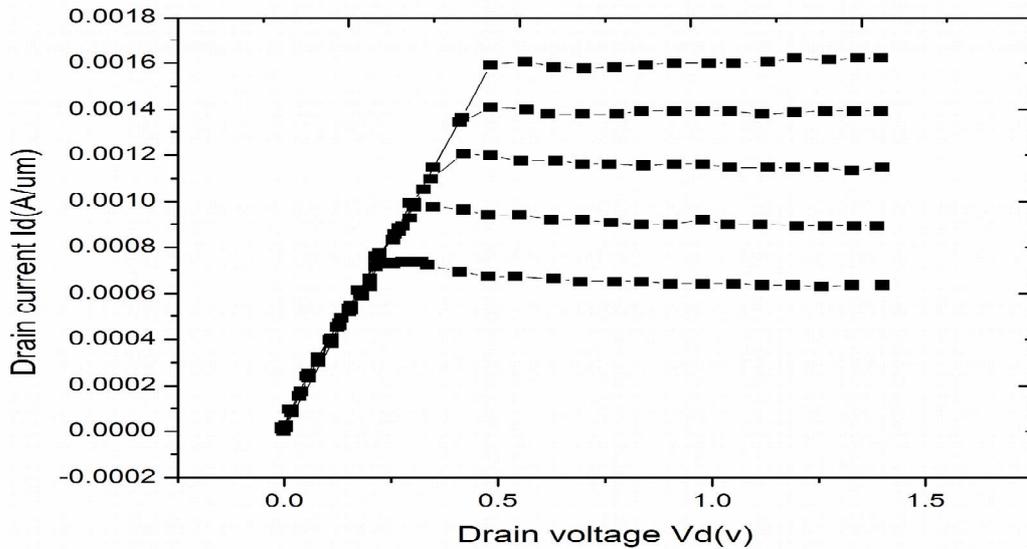
Fig 4.2 The DGHEMT device generated by Sentaurus Structure Editor

RF performances of the device were characterized by on-wafer S-parameter measurements. The measurements were carried out over the frequency from 0.1 to 40 GHz with step of 0.1 GHz at room temperature. S-parameter measurements for open and short pads were also performed on the same wafer in order to calibrate the parasitic capacitance and inductance components related to the pad metals. The frequency dependence of current gain (H21), the maximum available/stable power gain (MAG/MSG) and unilateral power gain (U) power-gain of the HEMT with VDS of 1.5 V and Vgs of 0 V after subtracting the parasitic capacitances due to the probing pads. We determined the value of the f_T by extrapolating H21 and the f_{max} by extrapolating the MAG/MSG and U using a least-squares fitting with a -20 dB/decade slope. Finally, the fT_0 of 204 GHz and the f_{max} of 352 GHz were demonstrated. In the above equation, $d = d_d + d_i$ is the total thickness of the InAlAs layer where d_d is $d_s + d_a$, Δd is the distance of the 2DEG from the hetero interface (~ 60 Å), ΔE_c is the conduction-band discontinuity at the InAlAs/InGaAs interface, ΔE_f is the position of the Fermi-level below the bottom of the conduction-band (~ 0 eV), ΔE_{fl} is the small energy arising from the linear approximation of n_s versus Fermi-level (~ 0 eV) and N_d is the donor concentration of the δ -doped layer ($\sim 0.25 \times 10^{25}$). $V_c(x)$ is the potential in the channel with α , V_{gm} , V_{l1} as the three fitting parameters used to adjust the detailed behaviour of the approximation. The value of α is chosen in the range $0 \leq \alpha \leq 0.5$ and is used to calculate the other two fitting parameters V_{gm} and V_{l1} .

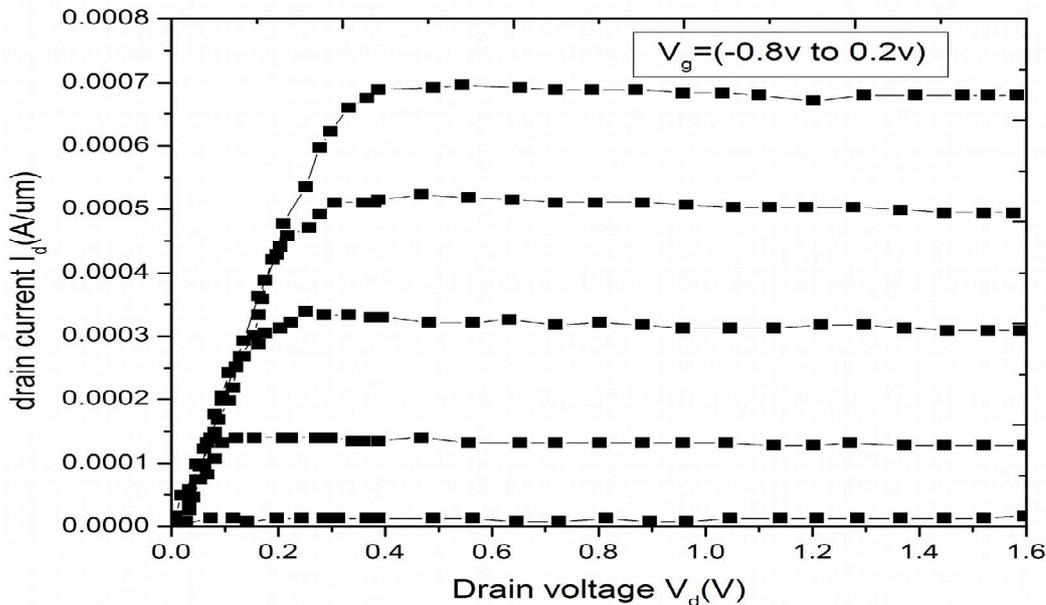
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Drain voltage versus Drain current by using channel of InAlAs



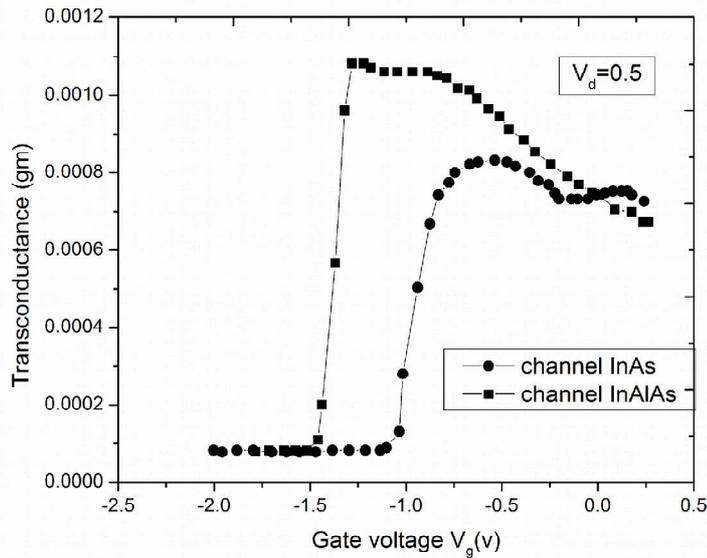
Drain voltage versus Drain current by using channel of InAs

This shows maximum frequency versus gate voltage of InAlAs/InAlAs DG-HEMT. A peak oscillation frequency of by using channel material InAlAs we obtained 395GHz, by replacing of channel that the material of InAs we obtained more frequency is 450GHz is achieved. current gain frequency is mainly used as a measure of physical device performance but a more practical measurement of high frequency performance is the power gain cutoff frequency because it is determined not only the material system but also process technology and device design parameters.

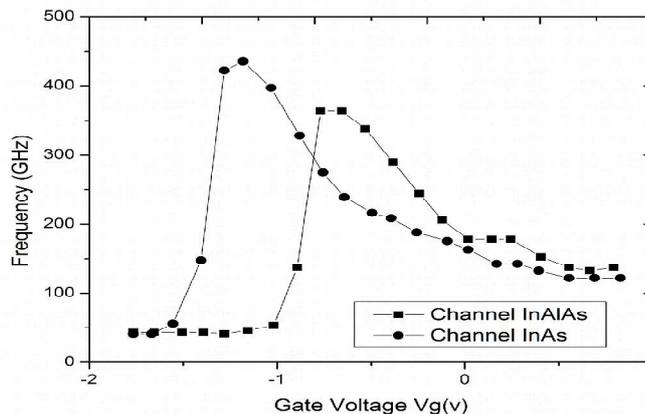
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Gate Voltage versus Transconductance



Transfer Characteristics of Gate Voltage versus Frequency

Technology CAD (or Technology Computer Aided Design, or TCAD) is a branch of electronic design automation that models the semiconductor fabrication and the semiconductor device operation. The modeling of the fabrication is termed as the Process TCAD, while the modeling of the device operation is termed as the Device TCAD. Included are the modeling of process steps (such as diffusion and ion implantation), and modeling of the behavior of the electrical devices based on fundamental physics, such as the doping profiles of the devices. TCAD may also include the creation of compact models (such as the well known SPICE transistor models), which try to capture the electrical behavior of such devices but do not generally derive them from the underlying physics. Technology Computer-Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processing technologies and devices. Figure 1.1 depicts a hierarchy of process, device and circuit levels of simulation tools. On each side of the boxes indicating modeling level are icons that schematically depict the representative applications for TCAD. The left side gives emphasis to the Design For Manufacturing (DFM) issues such as: shallow-trench isolation (STI), extra features required for phase-shift masking (PSM) and challenges for multi-level interconnects that

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IV. CONCLUSION

In general, DG-HEMT consists of two identical T-gates, one at the top and other at the bottom, followed by an doped InAlAs Schottky layer at the top and InAlAs Schottky layer at the bottom of thickness, a doped layer of thickness, with a doping concentration, to provide the necessary 2-DEG sheet chargedensity, and an doped InAlAs spacer layer of thickness. The total thicknesses of $\text{InAl}_{0.7}\text{As}_{0.5}$ and $\text{InAl}_{0.5}\text{As}_{0.5}$ are taken as respectively on both sides of the unintentionally doped InGaAs layer of thickness to form the 2-DEG channel. In this work, the double gate is taken to be symmetrical on both sides of 20-nm-thick InGaAs channel having 9-nm-thick Schottky barrier, 5 nm of doped layer with a doping of $1 \times 10^{18} \text{ cm}^{-3}$, and 3 nm of spacer layer. The cap layers, doped with $6 \times 10^{18} \text{ cm}^{-3}$, are 10 nm thick, and the recess widths on the source (L_s) and drain (L_d) sides are varied within the 100–300-nm range.

In future work is to investigate the impact of doping concentration and gate length of donor layer thickness, gate length channel current, transconductance, gate to source capacitance and cut-off frequency by using double gate HEMT. But going to use same material on both barrier and channel substrate with different mole fraction. After replacing InAs in substrate to perform high frequency in Terahertz

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