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Low Power 32-bit Improved Carry Select Adder based on MTCMOS Technique

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ABSTRACT: The raise in requirement for mobile and electronic devices is causing the necessity of low power. This paper presents the design of Carry Select Adder using MTCMOS technique. A 32-bit CSA is designed. The target technology is Mentor Graphics tool. By utilizing this architecture, power is diminished. This paper shows better results for MTCMOS technique when compared to Improved Carry Select Adder using CMOS and Hybrid Pass Transistor Logic. The comparisons are made between the CMOS logic, Hybrid PTL and MTCMOS. This work is evaluated on the target technology 130-nm Pyxis Schematic Editor.

KEYWORDS: CSA, CMOS logic, Hybrid Pass Transistor Logic, improved CSA, MTCMOS.

I. INTRODUCTION

Area and power reduction are the prominent areas in VLSI system design and data path logic systems. Rapid addition and multiplication have been an initial concern of high performance processors and systems all the time. In digital adders, propagation of carry is the main drawback that affects the speed of addition. The sum is generated continuously for each bit position in a fundamental adder. It is generated only if the preceding bit sum has generated and a carry is propagated into the successive position. The main limitation of the adders is generation and propagation of carry.

Ripple Carry Adder (RCA) includes of cascaded "N" single bit full adders. The carry that is generated as output of the earlier adder becomes the input carry of the next full adder. Hence, the carry of this adder travels the lengthy path. That means if the adder has N stages, it has to travel through N stages. It is the worst case delay path. Fig1 shows the structure of RCA. As the number of stages increments, the delay of adder will also rise in a linear way. RCA is the slowest adder when compared to other adders due to large propagation delay but it consumes less area which is shown in fig.1.

To conquer this delay problem, CSA is used. The implementation of CSA, improved CSA, and CSA using PTL are discussed in section II. Section III discusses the low power CSA using MTCMOS and section IV discusses the simulation results.

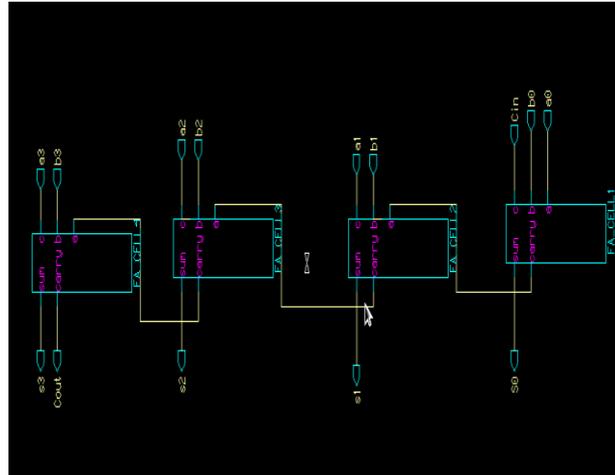


Fig. 1. Ripple Carry Adder

II. LITERATURE SURVEY

Many computational systems use the CSA to balance the problem of carry propagation delay. It produces numerous carries independently and then chooses a carry to provide the sum. However, the CSA is not efficient in terms of area because it employs various pairs of RCA to generate intermediate sum and carry by considering carry input and then the final sum and carry are picked by the multiplexers [1], [2]. To mitigate the above problem, improved CSA is proposed. Here the carry operates as selection line to the multiplexer. Whenever C_{in} is 0, the sum is calculated by means of XOR operation and C_{out} is determined by AND operation. Whenever C_{in} is 1, the sum is computed by means of XNOR operation and the latter is calculated by OR operation.

Carry Select Adder (CSA) is one of the fastest adder and the structure of the CSA displays that there is a chance for improving its efficiency by lowering the power dissipation and area in the CSA. High speed adders are required due to the necessity of high speed and low power computational units in floating point co-processors, image processing units and DSP chips. The most ancient arithmetic operation in processors is addition. The adder is one of the most prominently used computation unit of the processor. Power and delay analysis of various adders and a 32-bit CSA is implemented using Hybrid PTL/CMOS logic style. PTL is considered to be better than static CMOS because it obtains the potential for carrying out a logic function with less number of transistor counts, less delay less power dissipation. The analysis reports discusses that the recommended CSA design displays sophisticated result with respect to area, PDP and power compared to others.

The time required to propagate a carry through the adder is a limitation for the pace of addition in digital adders. In a fundamental adder, the sum for every bit position is provided in order only after the generation of the sum for previous bit position and a carry is propagated into the successive position. The Hybrid PTL/CMOS logic synthesis can develop suitable circuits, taking into account various limitations in the architecture. The multilevel PTL logic cells that are presented, naturally constructed from only a few fundamental cells. In many cases, pure PTL circuits have lesser area and power, but CMOS circuits have shorter delay.

A. Improved Carry Select Adder

It is particularized that output sum (S_0) of a single-bit full-adder is XOR of inputs A and B when initial carry is logic '0' while output S_0 is XNOR of inputs A and B when carry initial is logic '1'.

Hence it is required to utilize XOR gate and INV gate to achieve the output sum signal pair. Sum output either the XOR or the XNOR could be chosen by making use of the multiplexer with select line as prior carry signal. It is shown in the truth table, that the output carry (C_0) is AND of A, B inputs when initial carry is logic '0' while C_0 is OR of A, B

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when initial carry is logic '1'. In the similar way the previous carry is used as selection line to second multiplexer so that the carry output of the first stage is selected. It acts as selection line for the multiplexers in the second stage

TABLE I
TRUTH TABLE OF ONE BIT FULL ADDER

Cin	A	B	SUM (Sout)	CARRY (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B. HYBRID PTL/CMOS logic style

PTL is considered to be better when compared to static CMOS, because it has the capability for carrying out a logic function with less number of transistor counts, delay can be reduced and also power dissipation. Hence PTL is not considered better than CMOS of all kinds of logic structures.

At the circuit level, mixing pass-transistor logic (PTL) with static CMOS has been proposed in a way such that it absorbs less power. In conventional PTL design, committed buffers are introduced in pass transistor trees to bring back driving strength, where as mixed PTL assigns certain number of static gates at optimal points within pass-transistor trees to expand the driving strength as well as performing logic functions.

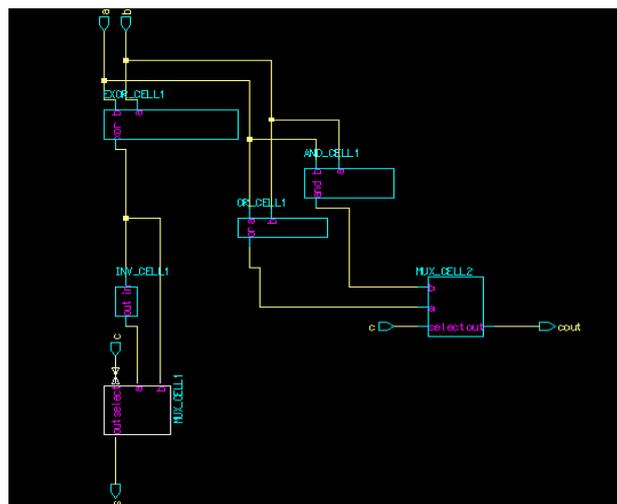


Fig. 2. Improved Carry Select Adder

Consequently, circuit performance and power consumption of mixed PTL circuits are further improved over the conventional PTL circuits. It is concluded by comparing CMOS and complementary CPL, that it is not an alternative of CMOS in terms of power consumption because of huge switching capacitance [5]. The choice of PTL cells directly

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impacts the Boolean matching process in the synthesis phase and has a significant impact on the overall quality of the final synthesized results. NMOS-only and PMOS-only pass transistor trees are used in PTL cells to decrease cell size. The complete rail-to-rail swing of the output signal is restored by the extra level-restoring circuit at the output of a PTL gate. The presence of level-restoring circuit at the output of PTL gates not only slows down the PTL gates due to potential drive-fights, but also increases their power consumption. PTL cells are only used for implementing MUX and XOR/XNOR-type logic functions and static gates are used to implement all the remaining logic functions.

III. LOW POWER CSA USING MTCMOS

Multi-Threshold CMOS (MTCMOS) has evolved as an efficient circuit-level technique. Due to this, high performance high performance is achieved. In standby mode, sub threshold leakage can be reduced by turning off the power of the in active blocks by sleep transistors. As CMOS technology is scaled, the supply and threshold voltages are reduced. A steep increase in the sub threshold current arises from the lowering of the threshold voltages. Recently, 40% of the total energy in active mode is dissipated because of leakage currents. As the number of transistors integrated onto the chip, the leakage currents will dominate the total energy consumption in high performance ICs.

MTCMOS technique is one of the prominent techniques. This technique can be used in the reduction of the leakage current. MTCMOS technique operates in two modes, one is the "active" mode and the other is "sleep" mode. The conventional circuit uses single threshold voltage (V_t) while the circuits employing MTCMOS technique uses two different threshold voltages. They are Low threshold and High threshold voltages. These circuits consists of two different types of transistors: the transistor which works on High V_t are known as "sleep" transistors and the transistors which works on Low V_t constitutes the logical circuit. The sleep transistors are used to achieve high performance by reducing the leakage current while the Low V_t transistors improve the circuit's speed performance. Even though MTCMOS circuit techniques are efficient, a serious drawback occurs which causes internal nodes to float. As a result, this technique cannot be directly used in standard memory cells without corrupting stored data.

The following figures illustrate the implementation of AND, OR, Inverter and XOR gates using MTCMOS technique. A 32-bit CSA is implemented using this adder based on MTCMOS technique.

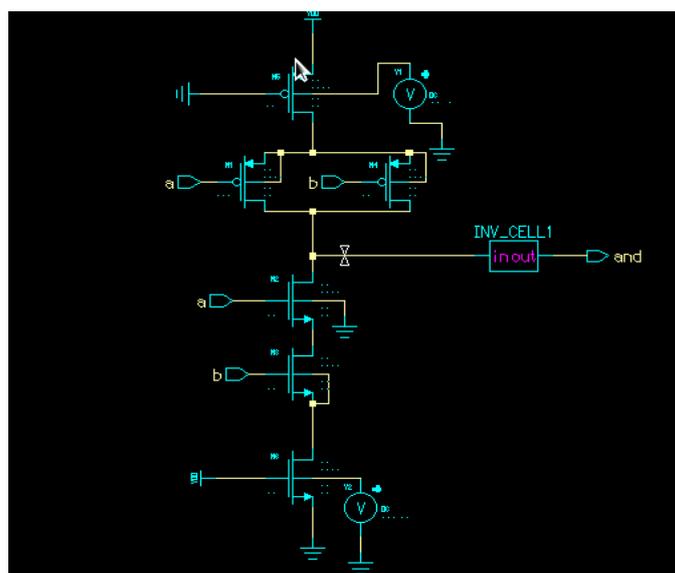


Fig. 3. AND gate using MTCMOS technique

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The above figure illustrates the implementation of the AND gate and its operation using MTCMOS technique. Design of OR gate using MTCMOS technique is shown in below figure.

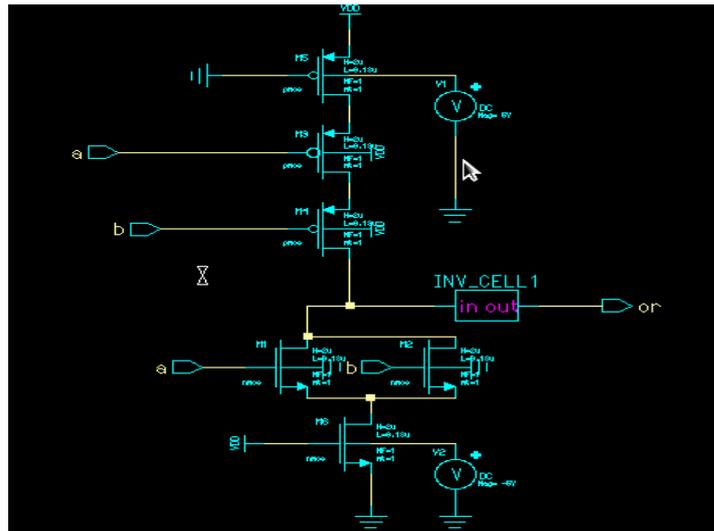


Fig. 4. OR gate using MTCMOS technique

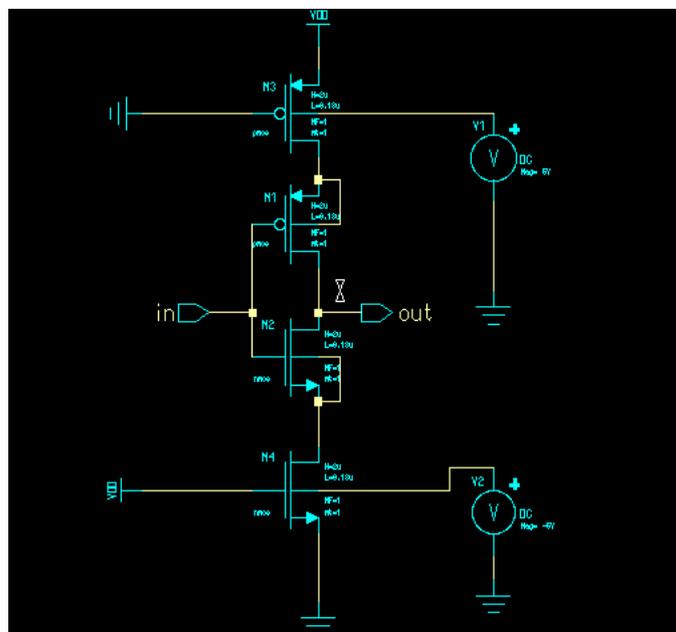


Fig. 5. Inverter using MTCMOS technique

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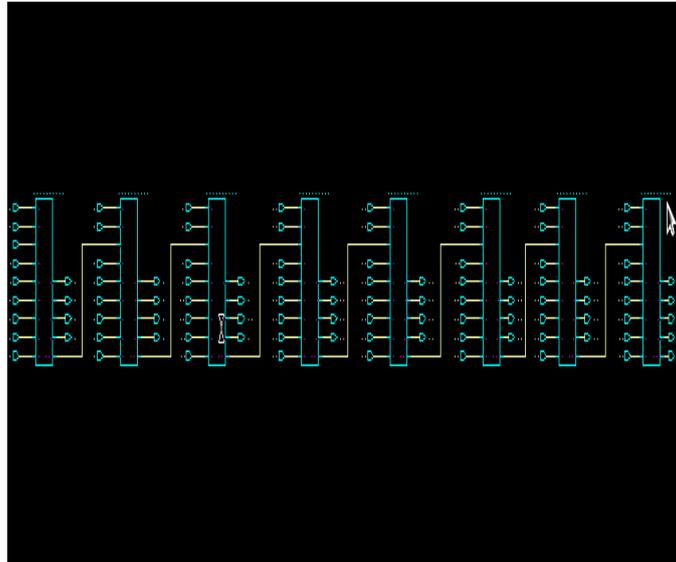


Fig. 6. 32-bit CSA using MTCMOS technique

IV. SIMULATION RESULTS

The target technology is the Mentor Graphics Pyxis Schematic Editor 130-nm technology. The fig. 7, fig. 8 demonstrates the 32-bit improved CSA and MTCMOS logic. The results are simulated using this technology and are illustrated as follows.

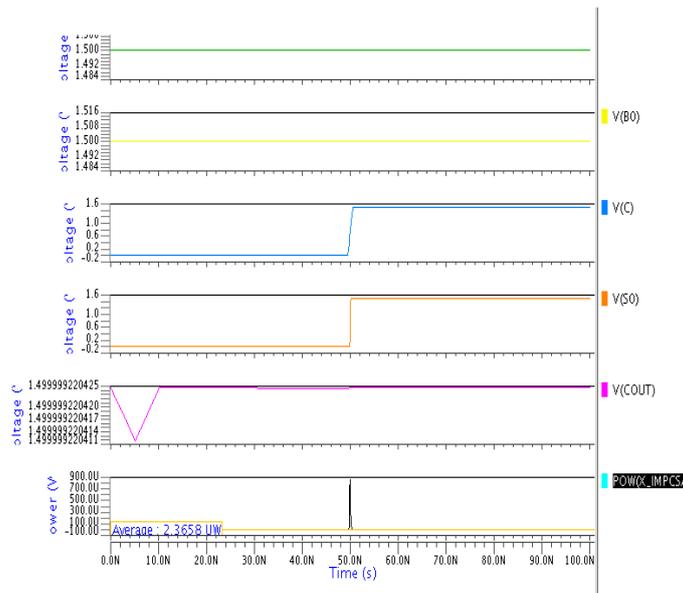


Fig. 7. simulation result of 32bit improved CSA

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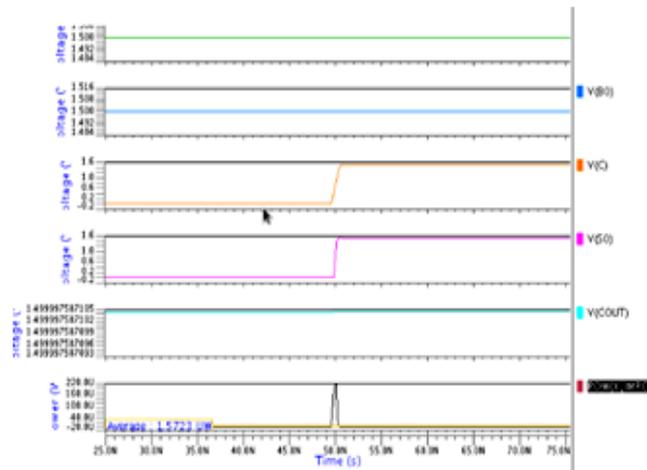


Fig. 8. Simulation result for 32 bit CSA using MTCMOS technique

TABLE 1. COMPARISON OF CSAs

S No	Average power for Improved CSA(μ W)	Average power for CSA using MTCMOS(μ W)
1	2.3	1.572

From the above table it is observed that the average power reduction using MTCMOS Carry Select Adder.

V. CONCLUSION

This paper mainly focuses on the implementation of CSA using MTCMOS technique. The comparison is made between improved CSA and CSA using MTCMOS technique. There is considerable reduction in power dissipated. The designs are evaluated on Pyxis Schematic Editor 130-nm technology.

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