

High Speed Low Power Carry Select Adder Using D-Latch

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ABSTRACT: Carry Select Adder (CSA) is one of many fast adders which can be used in data path applications. We can use new techniques to reduce the area, power and delay in the CSLA structure. This can be achieved by replacing one of the RCA block with any logic circuit which implements a logic to store the sum and carry for carry input 1 and use it later. In our paper, a new design has been used by using a D-latch instead of using an RCA cascade structure for $C_{in}=0$ or $C_{in}=1$. D-Latch is a single bit memory cell which gives same input as output with a delay and is controlled by an enable pin, it works only for enable high. If enable is low it stores the previous input, thus it serves the need of storing the sum and carry bits for RCA. In this way the area and speed can be improved. Hence we are designing 16-bit CSLA with parallel D-Latches which is the best adder design amongst all other previously existing adders.

KEYWORDS: Carry Select Adder, CSLA Structure, D-Latch, RCA.

I. INTRODUCTION

Achieving both high speed and low area consumption in data path logic systems at a time is always a difficult task, so we always have to compromise on anyone of them. Microprocessors, Digital Signal Processors and especially in digital computers we use many arithmetic operations like addition, subtraction, multiplication etc. High speed addition and multiplication is the basic requirement of high-performance processors and systems which mostly use the memory addressing. In implementing arithmetic operations we use adders as the basic building blocks. Hence, for efficient implementation of an arithmetic unit, the binary adder structures are the essential hardware units when used for large number of bits.

In digital adders, the speed of addition is limited by time required to propagate a carry through the adder from one block to other block. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry has been propagated into the next position which leads to unwanted delay in obtaining the output of the adder, and moreover as the number of bits increases the delay increases.

II. RELATED WORK

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\lceil \sqrt{n} \rceil$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays. Here we considered nonlinear structure of 2-bit, 2-bit, 3-bit, 4-bit, 5-bit structure to implement 16-bit adder. However, the carry select adder is not area efficient because it uses multiple pairs of Ripple Carry Adders to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (MUX).

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III. CARRY SELECT ADDER USING D-LATCH

CSLA is modified by using a D-latch which a simple cell compared to binary to excess converter. A BEC uses XORs, AND, NOT gates in designing its cell whereas D-latch uses only four NAND gates which are the universal gates. A D-latch is a memory circuit hence when enable is applied it stores the output for carry input 1 and provides it as an input for mux to select either RCA output or d-latch output for carry input as selection line.

Initially when $en=1$, the output of the RCA is fed as an input to the D-Latch and the output of the D-latch which follows the input is given as an input to the multiplexer. When $en=0$, the last state of the D input is trapped and is held in the latch.

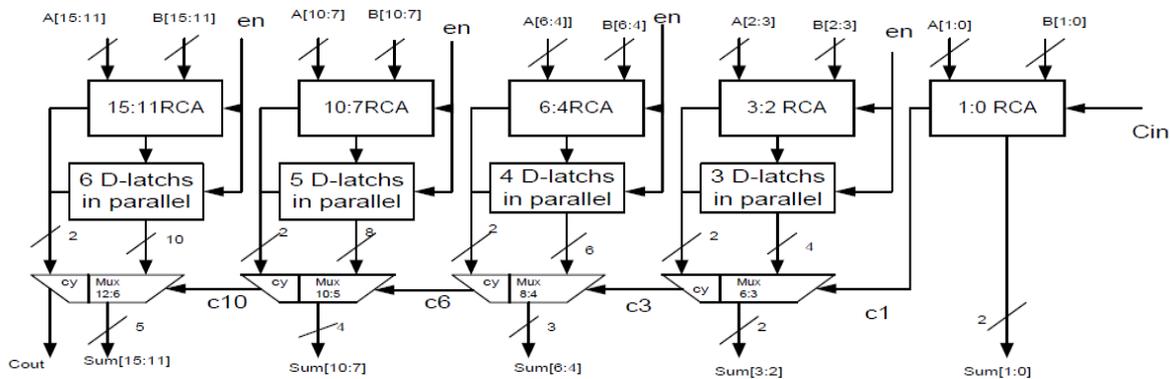


Fig 2.1: CSLA using parallel D-latches and MUXs

In this design, one of the RCA structures (i.e. $cin = 1$ or $cin = 0$) is replaced by a parallel structure of D-latches. For n bit RCA structure it required n D-latches with enable pin as a clk. Latches are used to store one bit information. The RCA structure cin is replaced by enable pin, where enable signal is clk signal. When enable pin $en = 1$ then the RCA structure is calculated for $cin = 1$ that result is stored in D-latch. When $en = 0$ then it will calculate for $cin = 0$ and the D-latch output and full adder output is given to the mux. By using selection line it will give the proper output. Where the enable time period for '1' is very less when compared to the enable pin '0'. Initially RCA structure will calculate for $en = 1$ and then $en = 0$. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle.

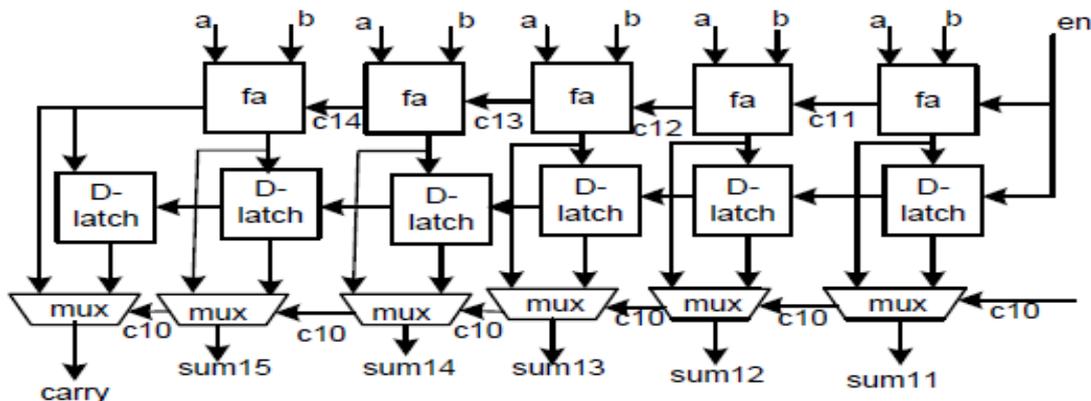


Fig 2.2: Internal structure of 6 D-latches in parallel block

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This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself.

Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

The D latch is used to store one bit of information which is a logic level present on the Data line when the clock input is high. When the clock pulse is high and the data on the D line changes, then the output, Q, follows the input, D and when the clock pulse input falls to logic 0, the last state of the D input is preserved and is in hold position.

IV. RESULTS

Now, let us see the results of the CSLA using D-latch structure.

The Technology schematic shows the LUT diagram which gives complete idea about the wiring of the logical blocks in the FPGA design. Each LUT consists of a truth table type of logic table and respective logic is designed using that LUT.

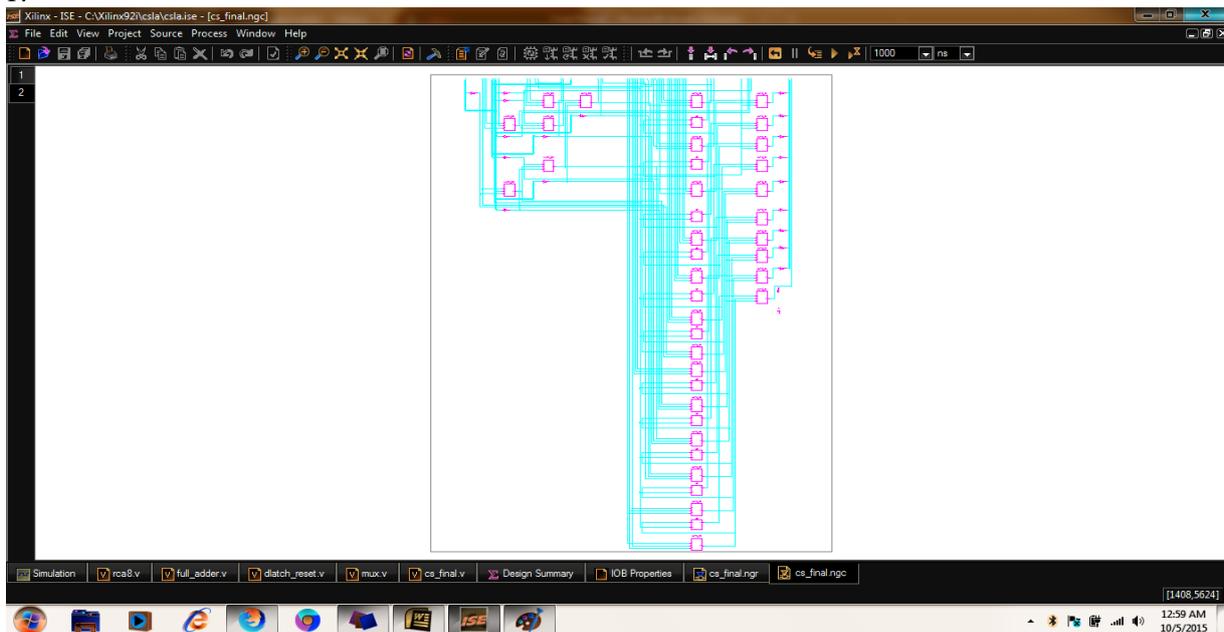


Fig 3.1: Technology Schematic of the implemented structure

This is the output for the inputs $a=1011010100101011$; $b=0100101011010100$;

The inputs are taken such that their output carry and sum varies for carry in 1 and 0.

Here the enable 1 should be initially made high for some time then made zero.

For carry in=0 \Rightarrow sum = $a + b = 1111111111111111$; carry out= 0;

For carry in=1 \Rightarrow sum = $a + b = 0000000000000000$; carry out=1;

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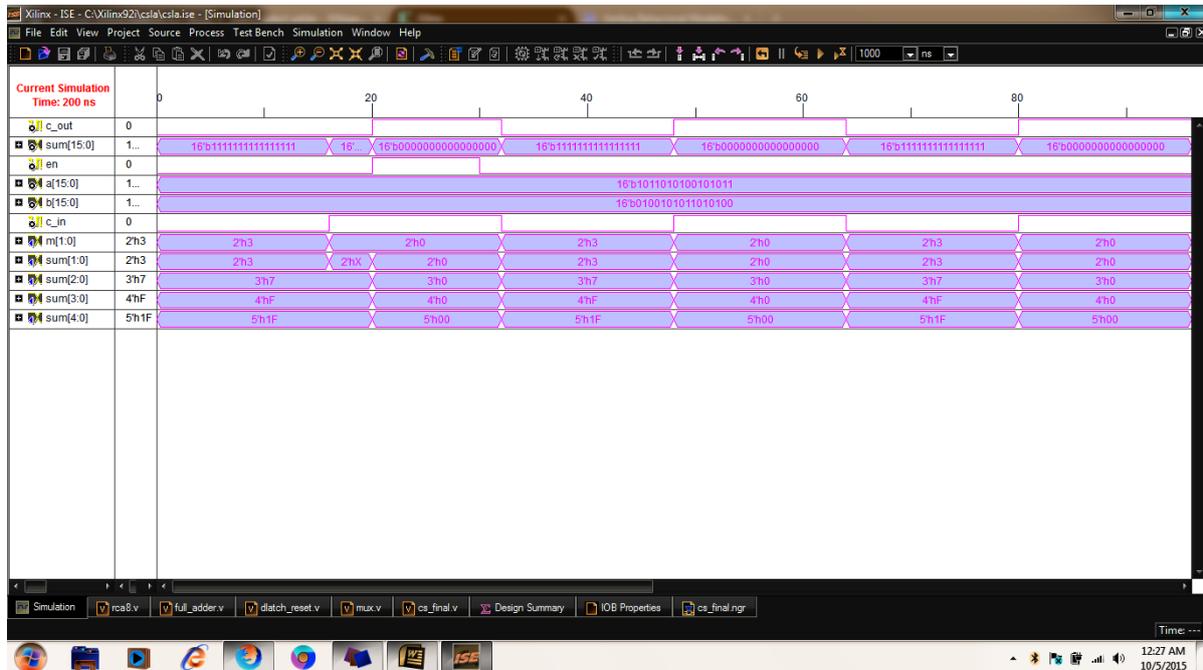


Fig 3.2: Output Waveforms

V. CONCLUSION

This paper deals with the adders which are used to reduce the area and increase the speed. For the improvement in area and speed from the ripple carry adder, first carry look ahead adder was used, then carry select adder and finally to CSLA using D-latches. CSLA using D-latches is the best adder which has minimum delay and area compared to all other earlier discussed adders. Compared to 16-bit Regular CSLA which got a total delay of 21.66 ns CSLA using D-latch has much reduced delay of 15.05 ns. Also the area consumed is very less as one of the RCA is replaced with D-Latch.

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