

# Trends, Opportunities and Challenges of Emerging Memory Technologies

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**ABSTRACT:** In this paper we have a tendency to analyse the chances of making a universal non-volatile memory in a near future. Unlike electric charge storing DRAM and flash memories, an alternative principles of charge-storage memories are required. Increasing leakage power for SRAM and DRAM and the increasing refresh dynamic power for DRAM have posed challenges to circuit and architecture designers of future memory hierarchy designs Emerging memory technologies— such as resistive RAM (RRAM), phase-change RAM (PCRAM), and spin-transfer torque RAM (ST T-RAM) — are being explored as potential alternatives to existing memories and also exhibit low operational voltages, low power consumption, high operation speed, long retention time, high endurance, and an easy structure.

**KEYWORDS:** DRAM, SRAM, Resistive RAM, PCRAM, Spin-Transfer Torque RAM.

## I. INTRODUCTION

In modern microelectronic devices the dominant memory types are DRAM, static RAM, and flash memory. These types of memory store data as a charge state. For many decades these memory technologies have been successfully scaled down to achieve higher speed and increased density of memory chips at lower bit cost [1]. However, memories based on charge storage are gradually approaching the physical limits of scalability and conceptually new types of memories based on a different storage principle are gaining momentum. Apart from good scalability a new type of memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure [2]. In addition, non-volatility is highly desirable to preserve the data when the power is off.

Technology scaling has had a great impact on memory in the areas of power and cost, but challenges due to small geometry are hindering this trend. The three main-stream memory technologies are SRAM, DRAM, and Flash. Table 1.1 compares these three technologies with main memory metrics. SRAM primary use has been for embedded memory due to fast access time. DRAM has been used for main memory due to small size and high density. Its slow access time and refreshing requirements prevent it from being used for on-chip. Flash is used for removable and big capacity memory. Its high voltage requirement for write operation prevents it from being used for on-chip. The SRAM vulnerability to process variation and its rationed logic working principle make it hard to meet the power and yield requirements. Figure 1.1 shows the scaling result of SRAM cell size and supply voltage below 90 nm. It is clear from the plot that voltage scaling has levelled out. DRAM however is facing challenges in small geometry due to cell-to-cell interference and capacitor size. Floating gate or Flash also has limitations due to stress-induced leakage current during programming with high voltage, and cell-to-cell parasitic that affects stored charge on closely packed cells.

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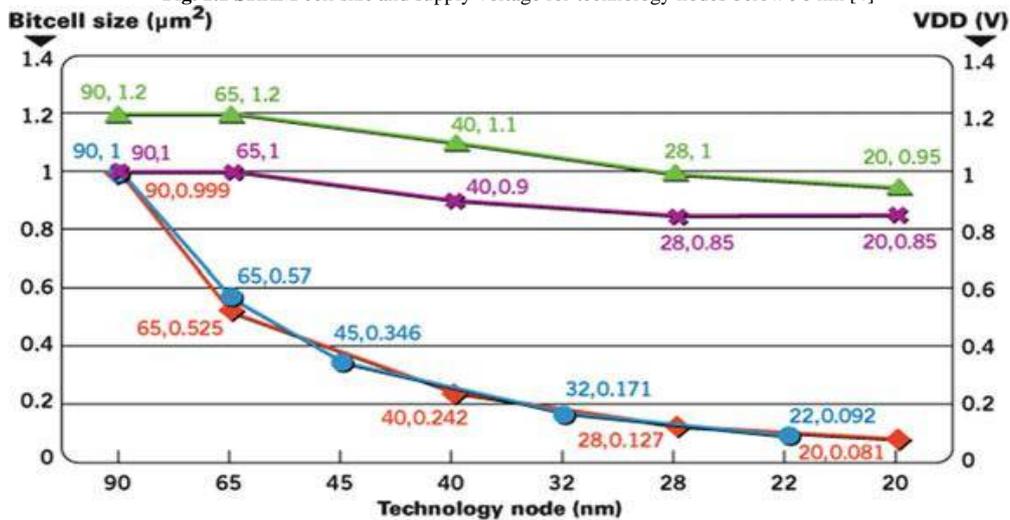
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**Table 1.1** Mainstream semiconductor memory and their parameter [3]

	SRAM	DRAM	Flash
Storage mechanism	Inter-locked state of logic gates	Charge on a capacitor	Charge trapped in the floating gate
Cell element	6 Transistors	1 transistor and 1 capacitor	1 transistor with floating gate
Feature size (F)	45 nm	65 nm (embedded) 36 nm (standalone)	90 nm NOR (embedded) 22 nm NAND (standalone)
Smallest cell area (F <sup>2</sup> )	140	12–30 6	10 4
Read time	0.2 ns	<10 ns (embedded) 2 ns(standalone)	15 ns (embedded) 0.1 ms (standalone)
Write time	0.2 ns	<10 ns	1 μs (embedded) 1 ms (standalone)
Retention time	As long as the power supply is on	4 ms 64 ms	10 years
Read operating voltage (V)	1	1.7 1.8	1.8
Write operating voltage (V)	1	2.5	10 (embedded) 15 (standalone)
Write endurance	>1e <sup>16</sup>	>1e <sup>16</sup>	1e <sup>5</sup> (embedded) 1e <sup>4</sup> (standalone)
Write energy (J/bit)	5e <sup>-16</sup>	5e <sup>-15</sup> 4e <sup>-15</sup>	1e <sup>-10</sup> >2e <sup>-16</sup>

**Fig. 1.1** SRAM cell size and supply voltage for technology nodes below 90 nm [4]



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## II. EMERGING MEMORY TECHNOLOGIES

3D NAND memories are nevertheless complex structures, with memory transistors subjected to traditional physical and electrical scaling limits. It is still not clear if this solution will be able to keep the cost reduction driven by Moore's law. In this context, in the last years, research in the memory fields has generally converged in the approach of a two terminal memory resistive devices, which are already available as product (such as phase change RAM (PCRAM), magnetoresistive RAM (MRAM), and ferroelectric RAM (FeRAM)), others only as prototype (such as carbon nanotube RAM (CNRAM), copper bridge RAM (CBRAM), spin-torque transfer RAM (STTRAM, STT-MRAM), and resistive RAM (RRAM)), while racetrack memory is available only as a memory concept.

Two of the most promising memory technologies are STT-RAM and PCRAM. STT-RAM is a new type of magnetic RAM that features nonvolatility, fast writing and reading speeds ( $< 10$  ns), high programming endurance ( $> 1,015$  cycles), and zero standby power. Compared to STT-RAM, PCRAM is even denser, with an approximate cell area of  $6$  to  $12F^2$ , where  $F$  is the feature size. In addition, phase-change material has a key advantage with its excellent scalability within current CMOS fabrication methodologies, featuring continuous density improvement. Table 2.1 lists the conventional and three promising emerging memory technologies comparing density and latency. Emerging memory technology is based on resistive RAM where a material changes its resistivity due to current passing through it. Then the material is able to remember the previous resistance state even after the current stops. This is why all the three types are considered as non-volatile memory. They all share the read disturb challenge which is due to the two-terminal bidirectional nature of the device [5]. The next section describes in more details about this emerging technology.

**Table 2.1** Memory type, mechanism, density, and latency ( $F$  is minimum feature size)

Memory type	Mechanism	Density ( $F^2$ )		Latency	
		2012	2015	Read	Write
SRAM	Oscillation	120	~60	1–4 ns	1–4 ns
DRAM	Charge on capacitor	6	4	25 ns	25 ns
Flash	Charge in floating gate	4	4	25 $\mu$ s	200 $\mu$ s
Spin torque transfer memory (STTM) (MRAM)	Spin dependent scattering in the ferromagnetic layers through magnetic tunnel junction	64	15	29.5 ns	95 ns
Phase change memory (PCM)	Contrast change between crystalline (low) and amorphous (high) resistance state	10	4	67.5 ns	215 ns
Memristor	ON/OFF resistance due to ion drift	4	4	60 ns	120 ns

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## III. RESISTIVE MEMORY PRINCIPLE

Most promising emerging memory technologies are based on resistive RAM. The device exhibits different resistance values that are controlled by passing electric current through it. The mechanism for each one is different, as will be discussed later in details, but from a circuit point of view, they all share same abstract. Its basic idea is to use RC constant with R being the memory element resistance and the capacitance is the parasitic capacitance of wires connecting the same cells from the same column [6].

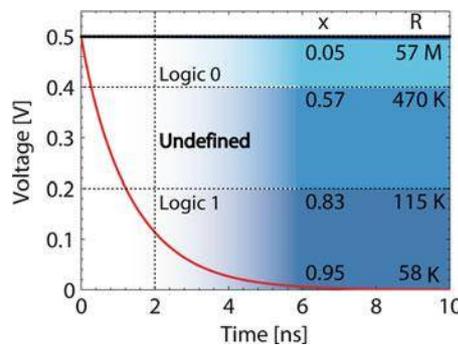


Fig. 3.1 Example of resistive memory implementation

Figure 3.1 shows an example of logic 0, logic 1, and an undefined state for memristor. This can also be used for multi-cell storage (MCL) [7] where different levels of voltage can be mapped to different bit combinations.

Despite the fact that PCRAM also uses resistance variations to store bit values, the term Resistive RAM (RRAM or ReRAM) has been applied to a distinct set of technologies that explore the same phenomenon.

## IV. SPIN TORQUE TRANSFER MEMORY (STT-MRAM)

Traditional toggle mode MRAM uses current-induced magnetic field to switch magnetic tunnel junction (MTJ). The challenge in this type of memory is the amplitude of the magnetic field increase when the MTJ size scale. STTRAM is a special type of MRAM that tries to achieve better scaling by using the spin characteristic instead of the magnetization. The basic principle of STT is to use the spin property of electron rather than the charge to distinguish between high and low resistance state [8]. The key building block for the cell structure is the MTJ as shown in Fig. 4.1.

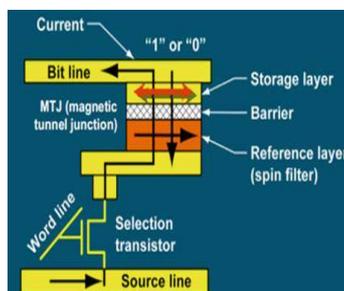


Fig. 4.1 Memory cell structure of STT RAM

It consists of two layers of ferromagnetic layers (FM) like iron with an insulator sandwiched between them [9]. One of the layers has a fixed magnetic direction while the direction of the other is controlled by injecting a spin polarized current. Logic states are realized by the ability to flip the magnetization of the direction of the free layer. If

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both spin directions are parallel, then it has small resistance and can resemble logic “0” while the anti-parallel has higher resistance and can resemble logic “1.” The insulator is thin to enable tunnelling of spins when a spin polarized current is injected (Fig 4.2).

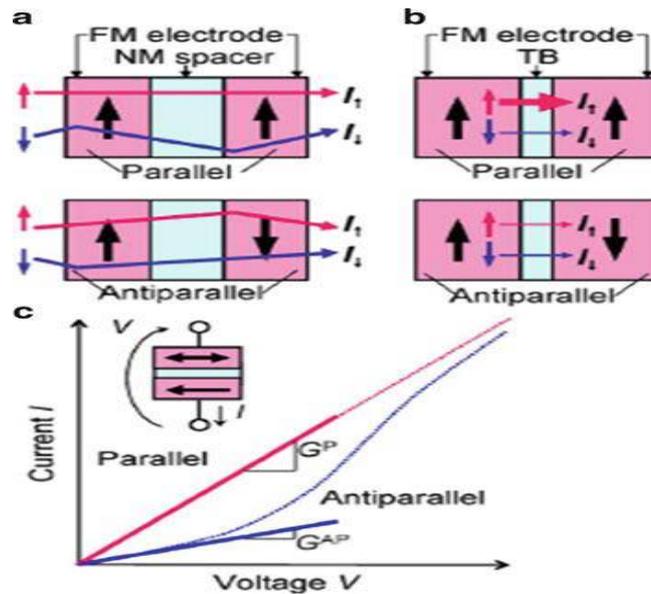


Fig. 4.2. STT RAM Structure and behaviour

There are three important layers in this device, namely the two ferromagnetic electrodes (FM1 and FM2), and an organic layer as a spacer. The device may be built on any suitable substrate material. The ferromagnetic electrodes can be metallic (e.g. Co, Ni, Fe or their alloys), half-metallic (e.g. ReMnO<sub>3</sub>, Re being a rare earth element, or CrO<sub>2</sub>), or semiconducting (e.g. GaMnAs). The organic layer can incorporate  $\pi$ -conjugated semiconductor polymers or small molecules (e.g. Alq<sub>3</sub>). In the vertical spin-valve devices that we have demonstrated so far, FM1 was a ferromagnetic oxide, La<sub>0.7</sub>Sr<sub>0.3</sub>MnO<sub>3</sub>, (LSMO). spin polarization show an oscillatory behaviour as a function of the spacer thickness and the bias voltage.

## V. PHASE CHANGE MEMORY

The basic principle of phase change memory (PCM) is based on proper heating and cooling of a two-state material [10]: the crystalline state which exhibits low electric resistivity (high conductivity) and amorphous state which tends to have high electric resistivity (low conductivity), sometimes three or four orders of magnitude higher. PCM exploits the large resistance contrast between the amorphous and crystalline states in the so-called phase change materials [11]. Due to this large resistance contrast, the change in read current is quite large, opening up the opportunity for the multiple analog levels needed for multi-level-cell (MLC) operations [11].

PCM has been considered as replacement for Flash but its temperature dependency and high current during phase change (write) has been a challenge for it to penetrate main market. Even though PCM is the known memory since the 1960s, renewed interest in PCM has increased due to new development in materials that improves its characteristics and temperature dependency.

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## VI. MEMRISTOR

Memristor was postulated by Leon Chua in 1971 but has not been realized until 2008 by HP [12,13]. It is the fourth fundamental passive element that relates (M(q)) flux to charge.

$$M(q) = \frac{d\Phi}{dq} = \frac{d\Phi}{dt} / \frac{dq}{dt}$$

Since the dynamical electrical characteristics of the memristor depend on the history the current passing through it and on the current voltage bias, the memristor requires two equations. One that relates the voltage applied  $v$  (across the device) and the current passing through it ( $i$ ). While the other explains an intrinsic property called the state variable ( $x$ ) and how it changes with time as a function of current [14,15].

$$v = M(x)i$$

$$\frac{dx}{dt} = f(i)$$

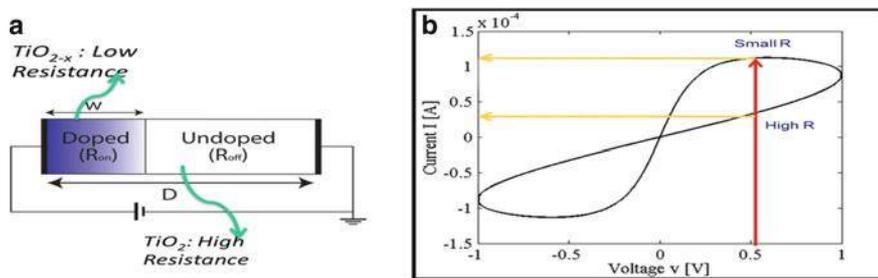


Fig. 6.1 Cross section of HP thin-film memristor and I-V characteristics

Figure 6.1 shows a cross section of Hewlett-Packard memristor consisting of a thin oxide film structured as Pt/TiO<sub>2</sub>/Pt with the TiO<sub>2</sub> divided into two regions. A region highly doped with oxygen vacancies TiO<sub>2-x</sub> acts as a conductor with low resistance. A TiO<sub>2</sub> undoped region acts as an insulator. Memristor exhibits bipolar switching characteristics. When a positive voltage is applied, oxygen vacancies are pushed to the undoped region resulting in a metal-insulator transition and turning the device on. Reversing the polarity of the applied voltage turns the device off. Moving the boundary between the doped and undoped regions changes the state variable giving rise to different resistance states. When no voltage is applied, the oxide thin film is capable of remembering the last resistance state it had. The current-voltage relationship of an AC signal is also shown in Fig. 6.1 and for the same voltage different current is observed based on the state variable value.

Different mathematical and spice models exist in literature [13,14,15], tries to capture and explain the dynamical behavior of the memristor. The exponential model described in [15] captures the non-linearity of the electric field seen within the memristor and it is the one that is a close match to the published data for real device.

Memristors are considered as one of the possible future alternatives to current CMOS technology. Memristor-based technology provides much better scalability, higher utilization when used as memory, and overall lower power consumption. The basic principle of memristor is ionic drift where charged ion (O<sub>2</sub><sup>-</sup>) in the case of HP-memristor is moved from the doped region (R<sub>on</sub>) to the undoped region (R<sub>off</sub>). The theory that tries to explain this behavior is based on small area (<10 nm). When a voltage of 2-3 V is applied, a huge electric field is created across the junction, which causes ions to move.

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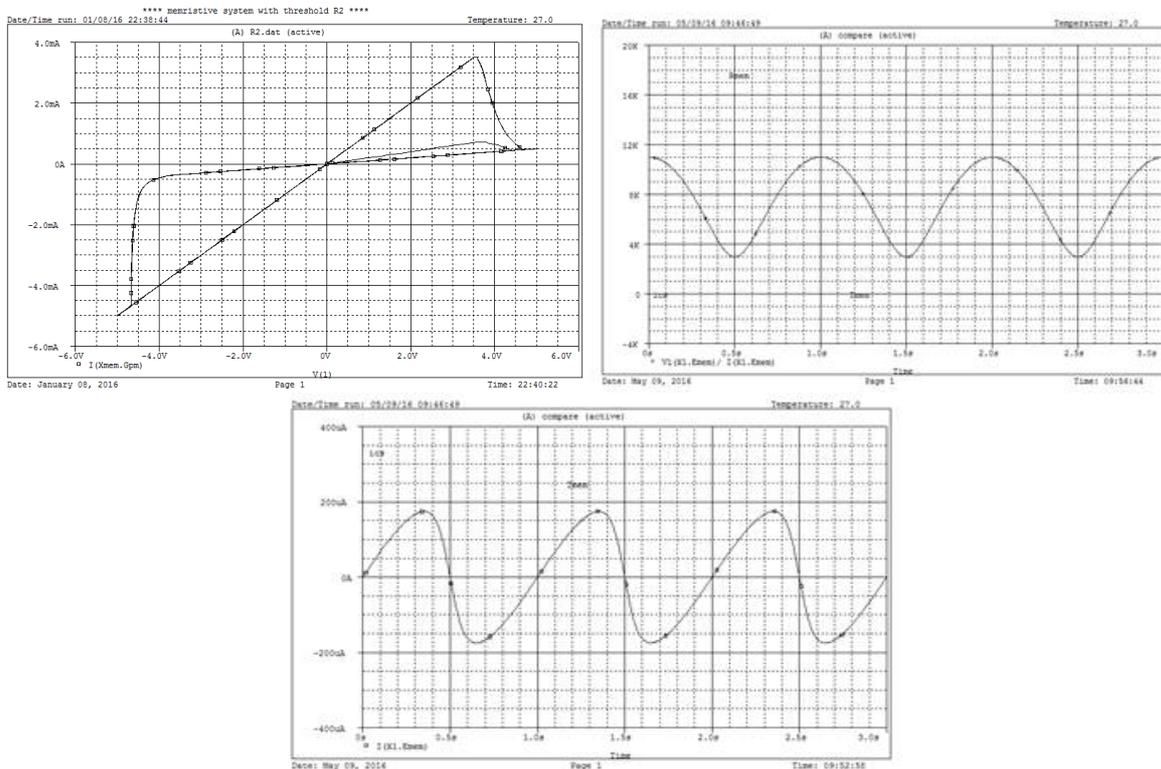


Figure 6.2: threshold memristor model.

In this model the current-voltage relationship is undefined and can be freely chosen from any current-voltage relationship, The dependence of the internal state derivative on current and the state variable itself can be modeled as independently multiplying two independent functions; one function depends on the state variable and the other function depends on the current. the characteristic I/V curve of a memristor showing hysteresis behavior is depicted. Increasing the frequency of the external voltage leads to a smaller  $q(t)$  with respect to  $w(t)$ , thus the hysteresis behavior of the memristor is decreased until asymptotically passing over to the characteristic curve of a conventional resistor.

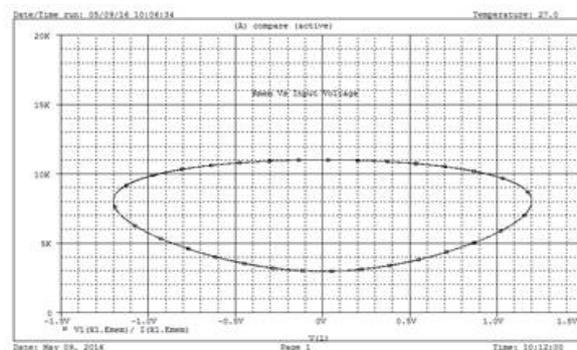


Figure 6.3: I-V Hysteresis Loop

Above figure shows the simulated  $i-v$  response of our model for a sine wave input of 2V at 1 Hz and 100 Hz. shows resistance response for the same stimulus. The  $i-v$  curve at 1 Hz resembles a inched hysteresis curve, which is a memristor fingerprint, while at the higher frequency the response resembles a linear resistor. Therefore the added volatility behavior does not interfere with the fundamental memristor model characteristics.

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Despite several announcements by HP to productize this technology, the device is still in research stage and no actual product has been developed. In addition to high write energy, memristor has challenges similar to all other resistive RAM cells.

## VII. CONCLUSION

In this paper, we discussed the limits of current charge-storage Silicon Non Volatile Memory technologies and the opportunities offered by the new resistive memory technologies. Significant advances in new materials, device technologies and circuits have made emerging memories good candidates to address, firstly, the huge business opportunities for low density NY memories (embedded flash microcontrollers and SoC) and, with a higher maturity level, also the applications of leading memory technologies. It should also be underlined that these emerging memories potentially combine the advantages of SRAM, DRAM, and Flash, so that they offer the opportunity to completely re-think the design of the memory subsystem to gain orders of magnitude improvements in speed and/or power consumption. Finally, resistive memories offer potential for exciting new applications and markets, as new functionality coupled with logic circuits to enable block power-down, or use as synapses in neuromorphic circuits [8].

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