

Bridgeless Topology for Power Quality Improvement in Switching Power Supply

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ABSTRACT: Many electronic appliances such as personal computers require Switched Mode Power Supplies (SMPS) for powering up. Normally, a Diode Bridge Rectifier (DBR) followed by a filter capacitor is used at the front end of these SMPSs. DBR causes significant deterioration in the power quality leading to very low power factor and high harmonic distortion at the ac mains. This work deals with the design, analysis, and simulation of a power factor correction SMPS using a bridgeless buck-boost converter at the front end. Single-phase ac supply is fed to a pair of back-to-back-connected buck-boost converters to eliminate the diode bridge rectifier, which results in reduction of conduction losses and power quality improvement.

KEYWORDS: Switch mode power supply, power quality, bridgeless, buck-boost.

I. INTRODUCTION

The growth of consumer electronics has meant that the average home has a lot of mains driven electronic devices such as low energy lighting, battery chargers, televisions, and computers their peripherals etc. Invariably these electronic devices have mains rectification circuits, which is the dominant cause of mains harmonic distortion. Most applications comprising of ac-dc power converters need the output dc voltage to be well regulated with good steady-state as well as transient performance.

The circuit which was typically favoured until recently (diode rectifier-capacitor filter) for the utility interface minimizes the cost, but it severely deteriorates the quality of the supply thereby affecting the performance of other loads connected to it also causing other well-known problems. The current waveform is very peaky, non-sinusoidal, and highly distorted; the PF is around 0.48. At full load, the total harmonic distortion (THD) of input ac mains current is 83.5%. The performance of the power supply is violating the limits set by various international standards such as the International Electrotechnical Commission (IEC) 61000-3-2.

Due to these issues, improved-power-quality SMPSs are extensively being researched, which are expected to draw a sinusoidal input current at a high PF. Improvement in power quality also results in better reliability and enhanced efficiency. To achieve a perceivable improvement in power quality, PF correction (PFC) circuits are employed in these SMPSs at the utility interface point. Active power factor correction refers to the method of increasing PF by using active electronic circuits with feedback that control the shape of the drawn current. High-frequency switching techniques have been used to shape the input current waveform successfully.

II. RELATED WORK

The use of non-isolated PFC converters at the front end of these power supplies is a commonly accepted solution to achieve a good power quality at varying input voltages and loads. Single-ended primary inductance converter (SEPIC) topology utilizes a bidirectional switch and two fast diodes [9]. The absence of an input diode bridge and the presence of only one diode in the owing current path during each switching cycle result in less conduction loss and improved

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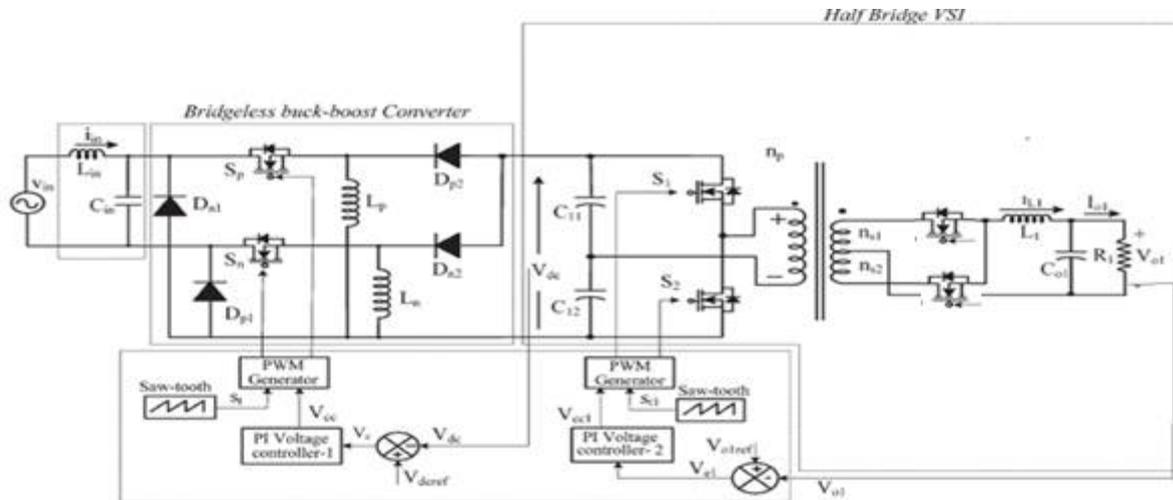
thermal management compared to existing PFC rectifiers. These advantages are desirable features for high-power and high-voltage applications.

Various bridgeless single ended primary-inductance converter and Cuk converters are proposed in the literature, which result in low voltage stress, improved thermal management, and low conduction losses [10] - [12]. New bridgeless single-phase ac-dc power factor correction (PFC) rectifiers based on Cuk topology are proposed in [13]. The absence of an input diode bridge and the presence of only two semiconductor switches in the current owing path during each interval of the switching cycle result in less conduction losses and an improved thermal management compared to the conventional Cuk PFC rectifier. These are designed to work in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion of the input current.

In another bridgeless Cuk topology, two input rectifier diodes are replaced by two switches in order to eliminate one switch in the conventional CUK PFC rectifier. By using DCM operation mode in the proposed converter, the control circuit is simplified and the current loop is omitted. However, the component count is increased in these converters, which is not suitable for low-power SMPS applications, although the output voltage range is fairly large.

While the high-frequency switching PFC stage reduces the line current harmonics, it also has drawbacks, such as: it introduces additional losses, thus reducing the overall efficiency; it increases the EMI, due to the high-frequency content of the input current; and it increases the complexity of the circuit, with negative effects on the reliability of the equipment, as well as on its size, weight and cost. The general aim of this thesis work is to investigate use of bridgeless buck-boost topology in the front end for rectification and power factor correction and to use synchronous switching at the back end converter.

III. CIRCUIT CONFIGURATION AND ANALYSIS



(a) Proposed convertor

The system configuration of the proposed SMPS is shown in Figure (a). Single-phase ac supply is fed to two buck-boost converters through an inductor-capacitor (L_{in} - C_{in}) filter to eliminate the high-frequency ripples. This EMI filter, or electromagnetic interference filter, is an electronic passive device which is used in order to suppress conducted interference that is present on a signal or power line.

In the bridgeless buck-boost stage, two buck-boost converters are connected back-to-back so that each takes care of one half cycle of the ac supply. The upper buck-boost converter that conducts during the positive half cycle of the ac supply consists of one high-frequency switch S_p , inductor L_p , and two diodes D_{p1} and D_{p2} . Similarly, the lower buck-boost converter that operates during the negative half cycle consists of one high-frequency switch S_n , inductor L_n , and two diodes D_{n1} and D_{n2} . Both inductors L_p and L_n of buck-boost converters are designed in DCM to obtain inherent PFC at the input ac mains.

Operation of bridgeless buck-boost converter: The bridgeless buck-boost converter is designed in DCM for single control loop and for inherent PFC.

Mode 1: In the first state, when the upper switch S_p is on, inductor L_p starts storing energy from the input, and the inductor current increases to the maximum value. Diode D_{p1} completes the current flow path in the input side.

Mode 2: In the second state, S_p is turned off, and the energy in inductor L_p is transferred to the output, thus reducing its current from maximum value to zero.

Mode 3: In the last state of one switching cycle, neither the switch and nor the diode conducts, and the inductor current remains zero, ensuring DCM operation.

In the next switching cycle, the same sequence of operation repeats itself. Similarly for negative half cycle of the input voltage, the lower buck-boost converter operates, and the same sequence of operation continues.

The controlled output dc voltage of the dual buck-boost converter is fed to the half-bridge VSI for high-frequency isolation, for voltage scaling. The use of synchronous switching will improve the efficiency of the converter. The operation of the half-bridge VSI in one switching cycle can be described in four states.

IV. DESIGN AND CONTROL

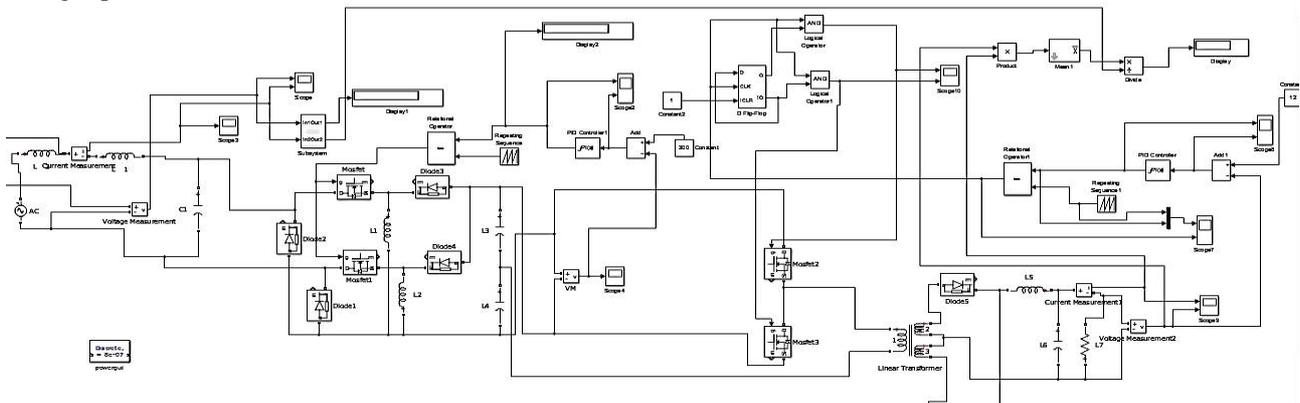
Buck boost converter has to be designed to operate in discontinuous conduction mode (DCM). So the value of upper and lower inductors need to be calculated cautiously. The values of upper and lower inductors are the same, and they are chosen based on the change in input current in one switching cycle during on condition of the switch. The inductor value for a specified current ripple is expressed as $L_p = DT V_{avg} / \Delta I_{L_{pon}}$ where D is the duty cycle, i.e., $t_{ON} = T$, where t_{ON} is the 'on' time of the switch and T is the total period in one switching cycle, and V_{avg} is the average of single-phase ac input voltage across the input of the buck-boost converter. In DCM condition, the inductor current ripple is considered maximum, and it must be equal to twice the input current.

$$L_p = \frac{DT V_{avg}}{2 * I_{in}} = 607 \mu H$$

The control of the SMPS is carried out using two independent controllers. The front-end bridgeless buck-boost converter utilizes the voltage follower approach, while the half-bridge VSI utilizes the average current control. Initially the control loop computes the output voltage error and then the voltage error is given to a PI voltage controller and the output of this is further given to a PWM generator to obtain the ON/OFF control pulses.

V. MODELLING AND SIMULATION

Performance of the proposed multiple-output SMPS is simulated in MATLAB/Simulink environment using SimPower-System toolbox and discrete time sampling. A sampling time of 0.8 sec is considered during simulation. Various power quality indices such as true power factor PF, and input current THD are analysed for assessing the power quality at single-phase ac mains.

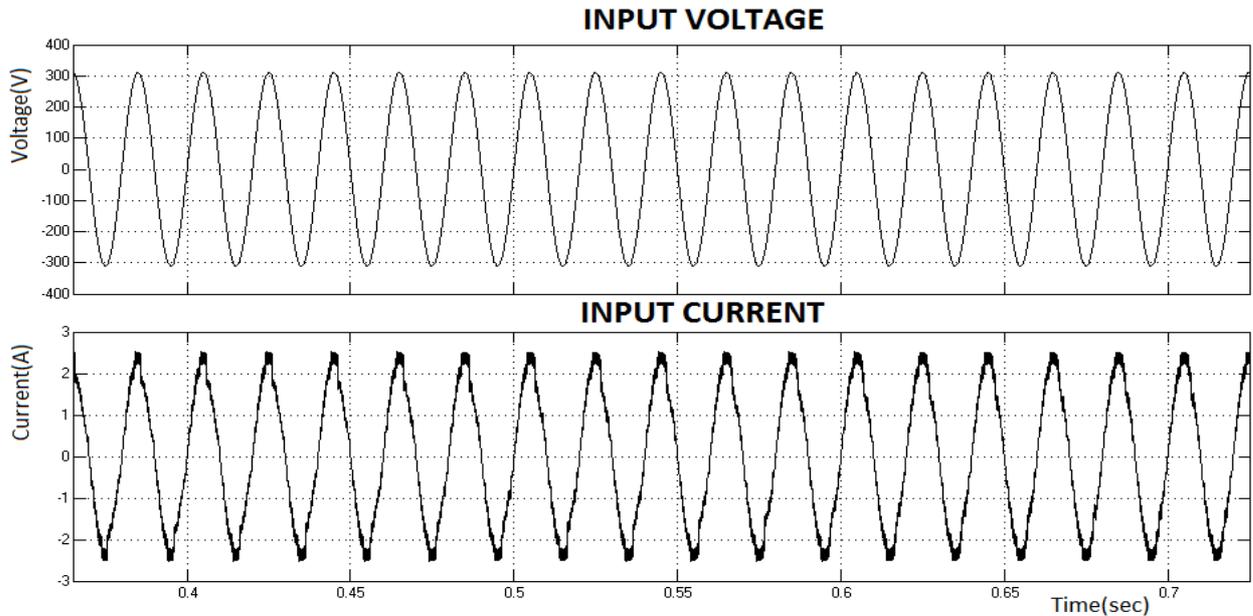


(a) Proposed Converter

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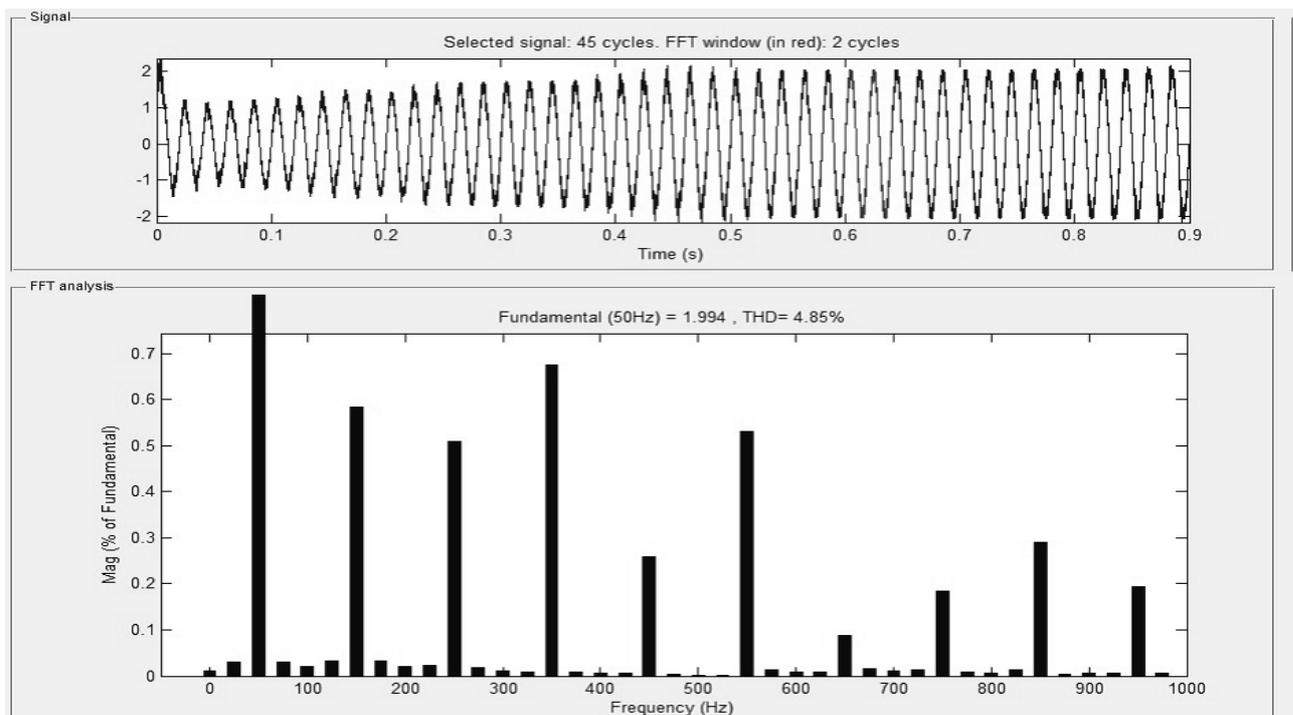
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(b) Input Voltage and Current

Input voltage waveform which is shown in Figure (b). It shows that the voltage is purely sinusoidal. The input current is sinusoidal and in phase with the ac input voltage, ensuring high PF operation with very low harmonic distortion.



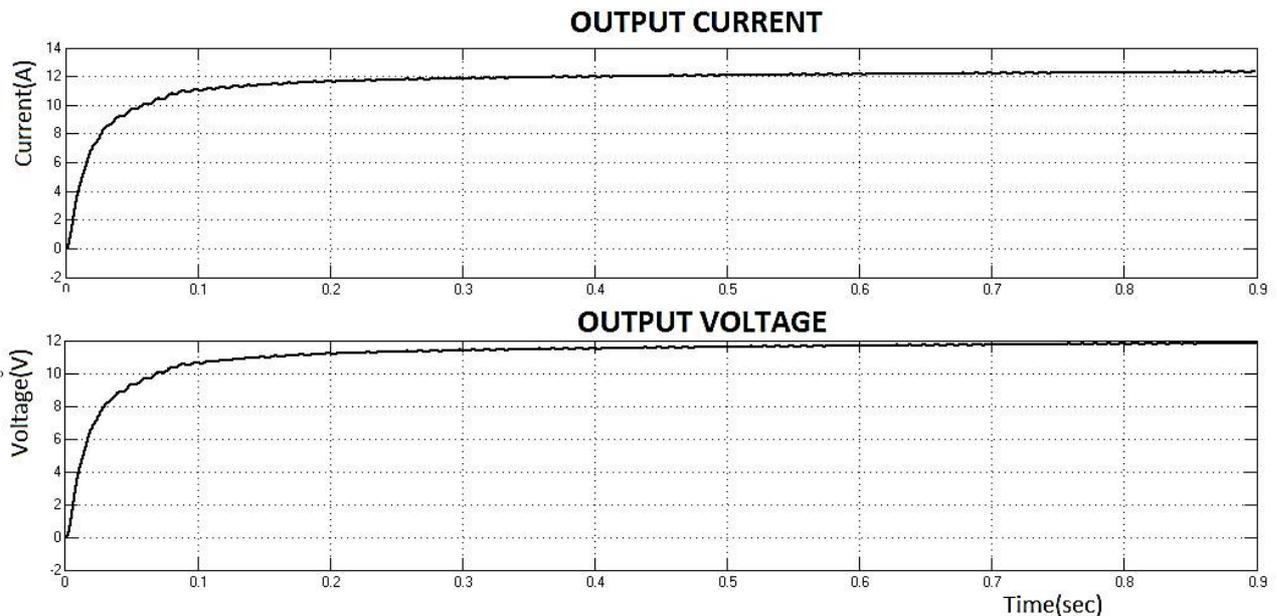
(c) Harmonic spectrum of input current

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Harmonics of line current using FFT analysis is as shown in Figure (c). Power factor of 0.99 and THD of 4.8% is achieved at mains.



(d) Output voltage and current 12V/12.5A

Output current and voltage for range is as shown in Figure (d). The output voltage of the buck-boost converter and output dc voltages of VSI are maintained constant.

VI. CONCLUSION

A bridgeless converter based multiple-output SMPS has been designed and simulated. The output dc voltage of the first stage buck-boost converter has been maintained constant and it is operated in DCM to achieve inherent PFC at the single-phase ac mains. A satisfactory performance has been achieved with power quality indices remaining within the acceptable limits set by IEC 61000-3-2. Power factor of 0.99 and THD of 4.8% is achieved at the mains.

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