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HEVC /H.265 Architecture Using GPU Parallelization

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ABSTRACT: The added encoding efficiency and visual quality that is offered by the latest HEVC(HIGH EFFICIENCY VIDEO CODING) standard is mostly attained at the cost of a significant increase of the computational complexity at both the encoder and decoder. However, such added complexity greatly compromises the implementation of this standard in computational and energy constrained devices, including embedded systems, mobile and battery supplied devices. To circumvent this limitation, this paper proposes the exploitation of embedded GPU devices already equipping many state of the art SoCs to accelerate the HEVC in-loop filters (i.e. de-blocking filter and sample adaptive offset). The presented approaches comprehensively exploit both fine and coarse-grained parallelization opportunities of these filters in an NVIDIA Tegra GPU.

KEYWORDS: HEVC, embedded system, GPU, NVIDIA.

I. INTRODUCTION

EXISTING SYSTEM:

- This paper presents a low-power programmable solution for HEVC in-loop filtering based on three identical TTA cores.
 - The TTA cores are synthesized using the UMC 90-nm standard cell library and the gate count of each core is 80K gate equivalent and the power consumption is between 12.6 and 13.1 mW per core depending on the executed program.
 - The production quality H.264/AVC encoder is compared with eBrisk Video (production quality HEVC implementation). Viewers favoured eBrisk encoded video at roughly half the bit rate compared to x264 in 62.4% trials. These tests confirm that HEVC yields similar subjective quality at half the bit rate of H.264/AVC.
- Compression performance analysis in HEVC – by Tabatabai et al in [E200] describes in detail the subjective and objective quality comparison of HEVC with H.264/AVC.

PROPOSED SYSTEM:

- ❖ To circumvent the added complexity of the decoding procedure defined by the HEVC standard, this paper proposed an efficient parallelization of the in-loop filtering modules (DBF and SAO) of the HEVC decoder by adopting low power GPU accelerators of embedded systems.
- ❖ To attain such objective, the presented approaches extensively exploit both fine and coarse-grained parallelization techniques in an integrated perspective, by re-designing the execution pattern of the involved modules, while simultaneously coping with their inherent computational complexity targeting embedded GPUs.

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II. CONSTRUCTION AND WORKING

EVOLUTION OF VIDEO CODING STANDARDS:

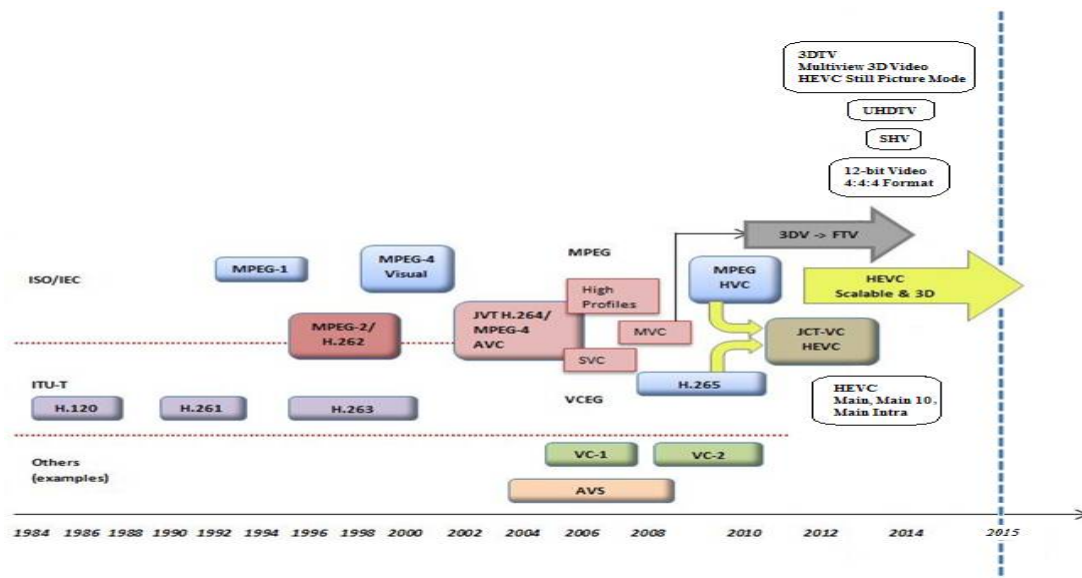


Fig 1. Evolution of video coding standards

HEVC ENCODER BLOCK DIAGRAM WITH LOSSLESS CODING MODE:

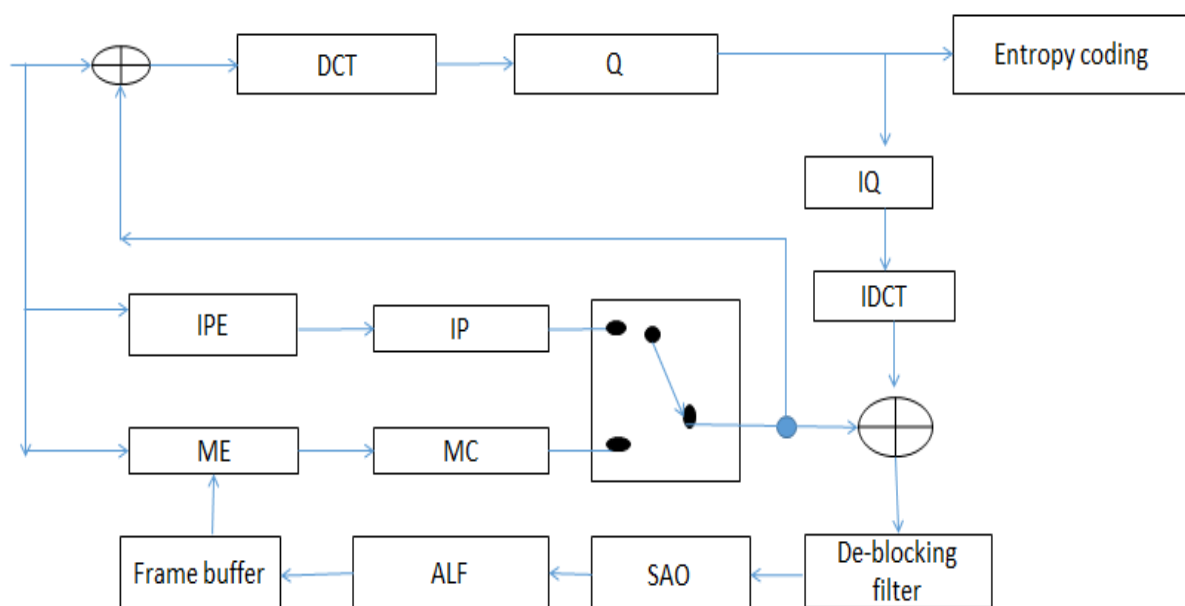


Fig 2. HEVC encoder block diagram with lossless coding mode

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III. EXPLANATION

DCT:

The discrete cosine transform (DCT) helps separate the image into parts (or spectral sub-bands) of differing importance (with respect to the image's visual quality). The DCT is similar to the discrete Fourier transform: it transforms a signal or image from the spatial domain to the frequency domain.

CODING TREE UNIT:

Coding tree unit (CTU) is the basic processing unit of the High Efficiency Video Coding (HEVC) video standard and conceptually corresponds in structure to macroblock units that were used in several previous video standards. CTU is also referred to as largest coding unit.

ENTROPY CODING:

The process of entropy coding (EC) can be split in two parts: modeling and coding. Modeling assigns probabilities to the symbols, and coding produces a bit sequence from these probabilities. As established in Shannon's source coding theorem, there is a relationship between a symbol's probability and its corresponding bit sequence. A symbol with probability p gets a bit sequence of length $-\log(p)$.

In order to achieve a good compression rate, an exact propability estimation is needed. Since the model is responsible for the probability of each symbol, modeling is one the most important tasks in data compression.

SAMPLE ADAPTIVE OFFSET:

The key idea of SAO is to reduce sample distortion by first classifying reconstructed samples into different categories, obtaining an offset for each category, and then adding the offset to each sample of the category. The offset of each category is properly calculated at the encoder and explicitly signaled to the decoder for reducing sample distortion effectively, while the classification of each sample is performed at both the encoder and the decoder for saving side information significantly.

ADAPTIVE LOOP FILTERING:

Adaptive Loop Filtering that reduce memory bandwidth, memory size requirements, and number of computations.

MOTION COMPENSATION:

Motion compensation (MC) is a critical component in terms of computational complexity and memory bandwidth. MC has high resolution significantly increases throughput and reduces memory traffic.

IV. RESULT

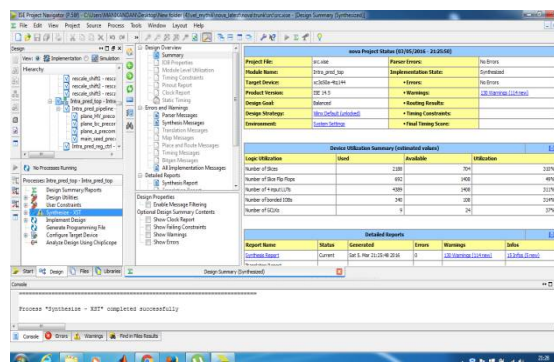


Fig 4: performance of area report

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SIMULATION OUTPUT:

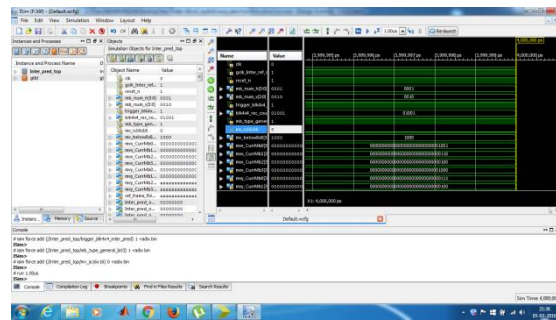


Fig 5:simulation output

RTL DESIGN:

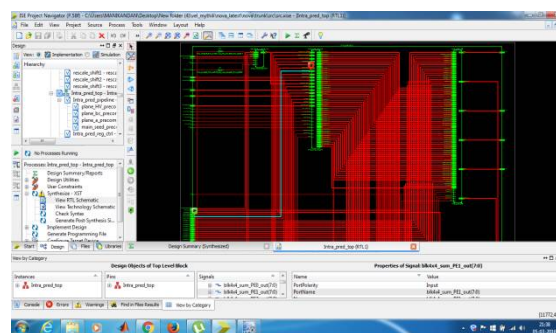


Fig 6.Performance of RTL diagram

INTRA PREDICTION DESIGN:

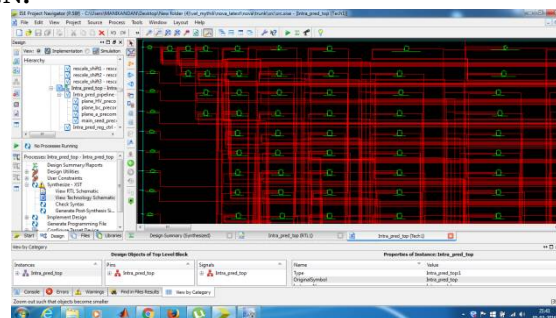


Fig 7.intra prediction design

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