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Design and Analysis of Analog to Digital Converter for Biomedical Applications

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ABSTRACT: In recent years, the need for Analog to Digital Converter (ADC) in biomedical applications is growing. Pacemaker, one of the important biomedical electronic equipment, has ADC which consumes more power. This paper presents a low power 8-bit Successive Approximation Register (SAR) ADC, suitable for biomedical applications. The 8-bit SAR ADC is designed and implemented in 180 nm CMOS technology using Cadence Virtuoso tool. Transient analysis is performed using supply voltage of 1 V and sampling rate of 111 kS/s. The measured maximum DNL and INL of the ADC are 1.25LSB and 1LSB respectively with power consumption of 5.25 μ W.

KEYWORDS: ADC, DAC, SAR ADC, DNL, INL.

I. INTRODUCTION

In most of the electronic systems, the input and output signals are analog in nature and use analog processing devices like amplifiers as input and output devices. Signals can easily be stored and transmitted in digital form. Most of the electronic systems require Analog to Digital Converter (ADC) at the input side for converting the analog signals into digital signals. Digital signals are further processed and Digital to Analog Converter (DAC) is used for converting digital signals back into analog signals.

In the biomedical field, most signals are in the analog domain. This signal is converted into an electrical signal by a sensor. These sensor devices are utilized for sensing biomedical signals from the human body such as ElectroCardioGraphy (ECG), ElectroEncephalo Graphy (EEG), and ElectroMyoGraphy (EMG). Further signal is processed by analog or digital circuitry. Nowadays digital signal processing requires digital form of signals rather than analog form. So ADC is required for converting the analog signals which are sensed from the human body into digital signals for next processing stages. The main goal of ADC is to convert the analog signal into digital form and then used for data transmission and processing systems. Bio-signals are usually noisy signals and their frequency is low to medium [4].

In biomedical devices, energy efficiency and long battery life are paramount design goals. Most of the biomedical signals are in mV range. There are many different ADC Architectures available. Successive Approximation Register (SAR), Delta-Sigma ($\Delta\Sigma$), Pipeline, Flash type, integrating or Dual slope.

Design of low power systems uses ADC as a key component for the purpose of keeping power utilization as low as possible. Examples for low power consumption equipment are pacemakers and cardiac defibrillators. Since the ADC consumes more power, it is the main part of an implantable pacemaker. Here focus is on decreasing the power consumption of an ADC. Biomedical application requires ADCs with low power and medium resolution (8-12 bits) and sampling rate of 1-1000 kS/s [1]. Hence SAR ADC is suitable for biomedical applications because of its simple structure and low power consumption.

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II. RELATED WORK

SAR ADC architecture with modification in DAC module is presented in [7]. SAR ADC has been preferred in most of the application because of their compact circuitry as compared with other ADC which makes this SAR ADC inexpensive.

An ultra-low power 8-bit Successive Approximation Register (SAR) ADC, suitable for biomedical applications is presented in [1]. The SAR ADC was designed and implemented in 180 nm CMOS technology with supply voltage of 1V. The proposed SAR ADC consumed a power of 164.97 μ W.

The design challenges of low power ADCs for biomedical implantable devices are presented in [8]. The comparator block consumed more power compared to other blocks of SAR ADC. In this paper low power comparator is designed for reducing power consumption in SAR ADC.

III. DESIGN METHODOLOGY

Successive Approximation Register (SAR) controls the operation and stores the converted digital data. The digital data can be taken serially from the comparator block or parallel from the SAR block. The DAC dominates the accuracy and speed of the SAR ADC [1]. A separate Sample and Hold circuit is used to reduce the power consumption of the SAR ADC. The first block, Sample and Hold (SH), takes samples from a continuous voltage and then hold the level for a certain time interval. Figure 1 shows the block diagram of SAR ADC. Figure 1 shows the block diagram of SAR ADC.

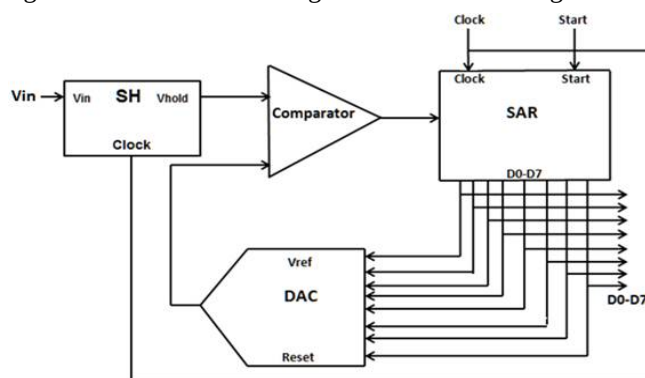


Figure 1: Block Diagram for SAR ADC

IV. IMPLEMENTATION AND SIMULATION RESULTS

A. Sample and Hold circuit

Sample and Hold (S/H) circuit contains a switch and the capacitor. In sampling mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value as soon as the sampling signal goes to low in the hold mode. During conversion, the Sample and Hold provides a constant voltage to the input of the ADC. To reduce charge injection problem, one technique is to use dummy transistor beside the switch shown in Figure 3. Figure 3 shows the schematic of Sample and Hold.

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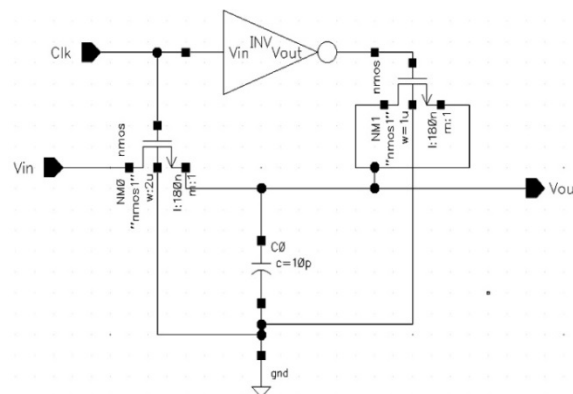


Figure 3: Schematic of Sample and Hold

Figure 4 shows the simulation result of Sample and Hold circuit. The Sample and Hold circuit consumed a power of 21.19 nW.

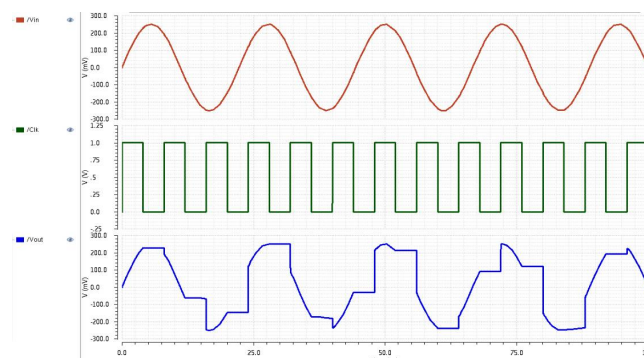


Figure 4: Simulation Result of Sample and Hold

B. Comparator

Comparator is the main analog block of SAR ADC. It performs the actual conversion and consumes more power compared to other blocks. From the available comparator architectures, the two stage differential type comparator architecture is selected and designed for low power applications. The comparator circuit compares an analog signal with reference signal and produces a output signal which is a binary signal (0 or 1). Design parameter for differential type comparator is shown in Table 1.

Table 1: Design parameters for Comparator

V_{DD}	1 V
Common Mode Range(CMR)	-0.5 V to 0.5 V
Output range	0 V to 1 V

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Figure 5 shows the schematic of comparator circuit.

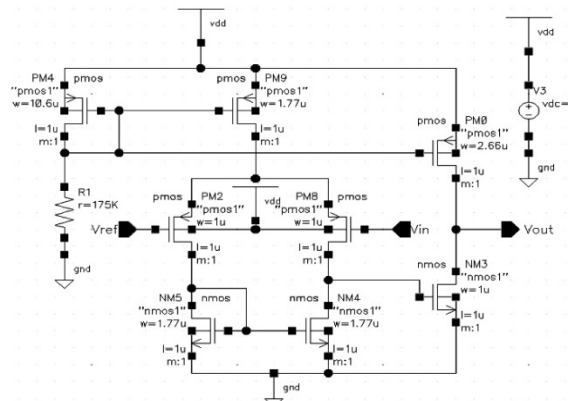


Figure 5: Schematic of Comparator

Figure 6 shows the simulation result of comparator circuit. The comparator circuit consumed a power of 3.718 μ W.

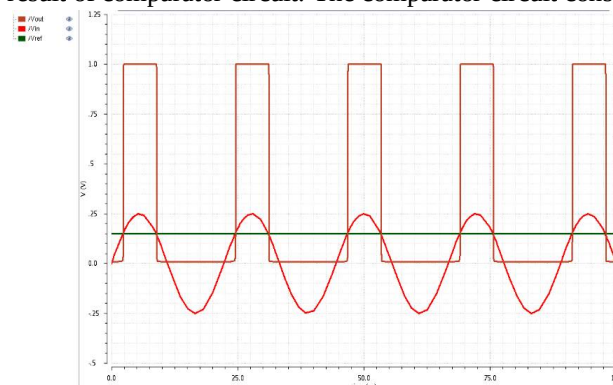


Figure 6: Simulation Result of Comparator

C. Digital to Analog Converter

A Charge redistribution DAC is a parallel array of binary-weighted capacitors. It is well suited for MOS and CMOS technologies. The array has total capacitance of $2^N C$ including the terminating capacitor of weight corresponding to the least significant bit (LSB). They operate on the principle that charge stored in a capacitor is proportional to the voltage across it [2].

Initially the top and bottom plate of the capacitor are connected to ground. The top plate is grounded through the reset switch; therefore the net charge stored in the capacitor array is zero. This phase is called as the reset phase. If the bit value is '1' then the switch is connected to V_{ref} (or) if the bit value is '0' then the switch is connected to ground. The output voltage is calculated based on voltage divider principle between the capacitors. This phase is called Evaluation phase. For example if the MSB is high and the remaining bits are low, then only the switch D_{N-1} is connected to V_{ref} and all other switches are connected to ground. Figure 7 shows the schematic of 8-bit charge redistribution DAC.

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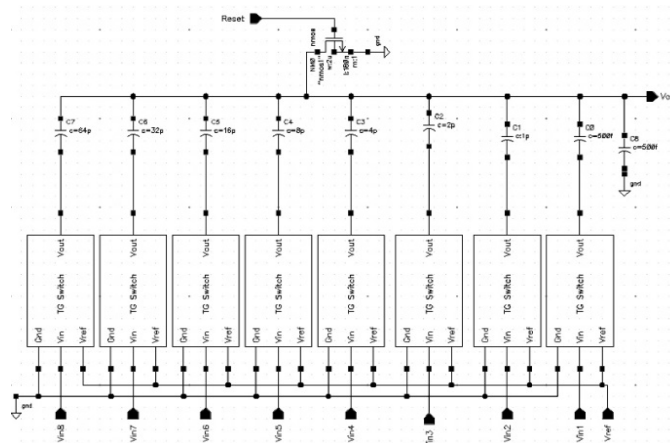


Figure 7: Schematic of 8-bit DAC

Figure 8 shows the simulation result of 8-bit charge redistribution DAC. DAC circuit consumed a power of 75.45 nW.

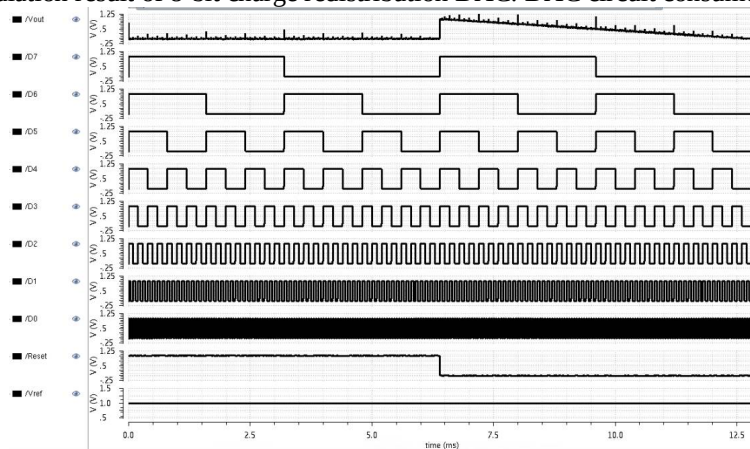


Figure 8: Simulation Result of 8-bit DAC

D. SAR Logic

SAR control logic determines each bit successively. The N-bit ADC requires N bit SAR logic for its control operation. For an N bit SAR ADC, digital control logic needs at least N flip-flops to perform conversion [3]. Therefore, a non-redundant SAR employs minimum number of flip-flops. At the initialization step (step 0), all output bits are reset to '0'. At step 1 SAR assigns MSB to 1 and the other bits to 0. At step 2, the SAR control logic makes its decision based on the output of the comparator. If it is high, MSB remains 1 otherwise SAR changes MSB to 0. Thus the value of MSB is defined now. Simultaneously SAR sets next MSB to 1. The output of SAR is then applied to DAC. The Sample and Hold output is compared with DAC output and given to SAR. Now SAR computes the value of next MSB based on results obtained from comparator. Therefore, successive approximation logic determines all the bits sequentially [6]. Figure 9 shows the schematic of 8-bit SAR logic.

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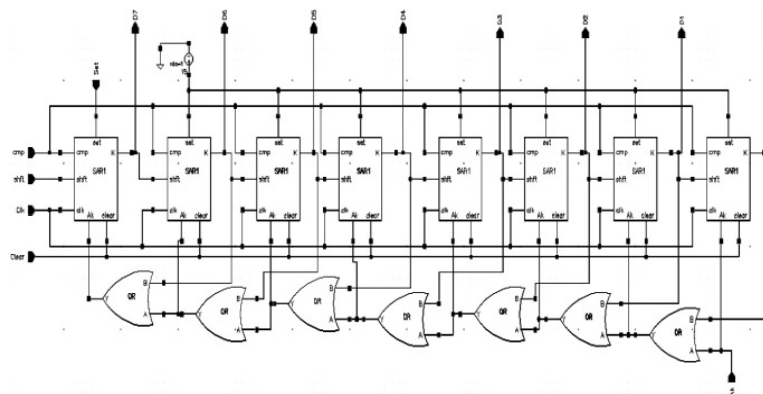


Figure 9: Schematic of 8-bit SAR logic

Figure 10 shows the simulation result of 8-bit SAR logic with comparator output 00000000. SAR logic consumed a power of 19.78 nW.

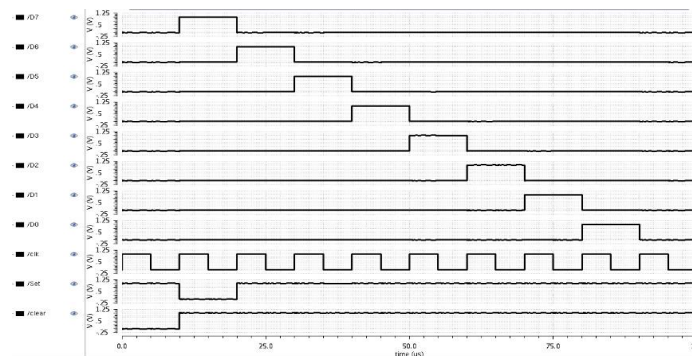


Figure 10: Simulation Result of 8-bit SAR logic

E. Successive Approximation Register ADC

Figure 11 shows the schematic of complete SAR ADC.

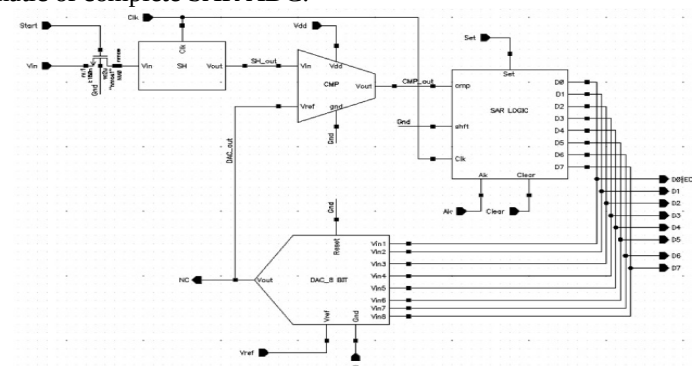


Figure 11: Schematic of 8-bit SAR ADC

Figure 12 shows the simulation result of 8-bit SAR ADC with $V_{in} = 5mV$ V_{dc} . SAR ADC consumed a power of 5.258 μW .

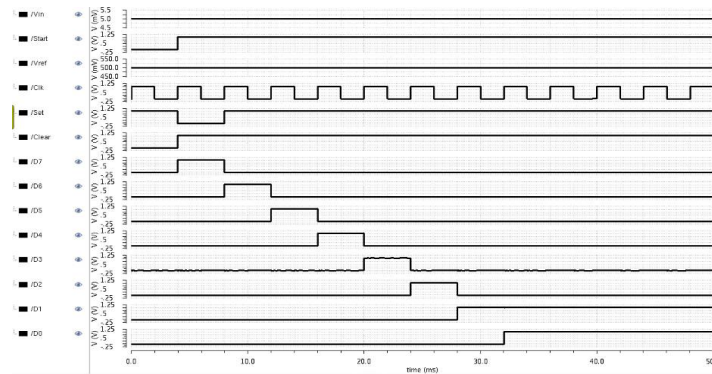


Figure 12: Simulation Result of 8-bit SAR ADC

The DNL and INL values are calculated and simulation graph for the same is drawn using MS-Visio are shown in Figure 13 and Figure 14 respectively.

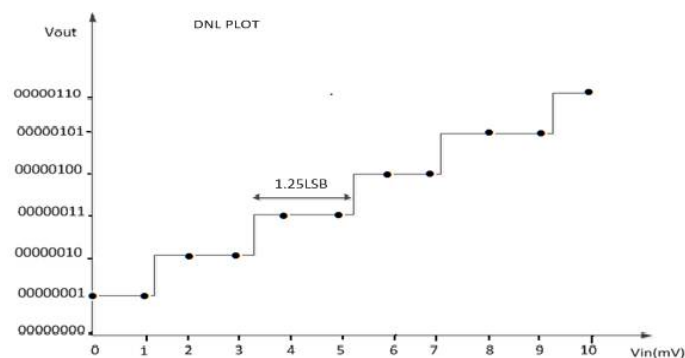


Figure 13: DNL plot for 8- bit SAR ADC

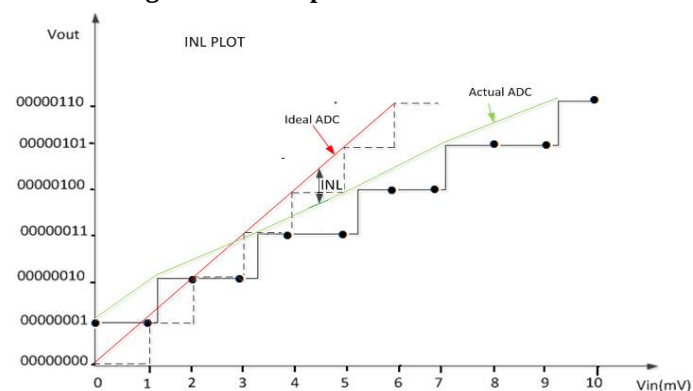


Figure 14: INL plot for 8- bit SAR ADC

The performance characteristic is explained using DNL and INL measurement. The measured DNL and INL are +1.25 LSB and +1/-1.1 LSB, respectively.

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V. CONCLUSION

In modern life, electronic equipment is frequently used in different fields such as biomedical, communication, transportation, entertainment etc. Data converters namely, ADCs and DACs are very important component in electronic equipment as most real world signals are analog in nature.

In this paper a 8-bit SAR ADC is simulated in 180 nm technology using Cadence Virtuoso tool at 1V supply voltage and sampling rate of 111 kS/s. DNL and INL for 8-bit SAR ADC are plotted. The measured DNL and INL are +1.25LSB and +1LSB/-1.25LSB respectively. SAR ADC required 9 clock cycles for converting one analog signal complete to digital form. Power consumption of 8-bit SAR ADC is 5.258 μ W.

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