

Design and Implementation of 2.4 GHz band Zigbee Transmitter for an Acknowledgement Frame Using Verilog HDL

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ABSTRACT: Zigbee standard consists of a set of communication protocols for wireless networking. This standard is suitable for communications with low power and low data-rate devices. This technology was developed for Wireless Personal Area Networks (WPAN). Zigbee Alliance is the development authority of this standard. Zigbee standard is compliant with the IEEE standard 802.15.4 as well since it has adopted the Physical layer (PHY) and Medium Access Control (MAC) layer protocols of IEEE 802.15.4 standard. The implementation cost of zigbee devices are less. This is achieved by simplifying the protocols and reducing the data rates. Zigbee devices are more responsive compared to Bluetooth devices. Most of the time zigbee devices will be in the sleep mode. So the average power consumption will be low.

Main blocks in zigbee transmitter section includes: CRC-16 generator, bit-to-symbol block, symbol-to-chip block, OQPSK block and pulse shaping block. In this paper, the zigbee transmitter blocks are modelled using Verilog HDL, it is then simulated using Xilinx and finally implemented on Virtex-5 LX50T Field-Programmable Logic Array (FPGA).

KEYWORDS: Zigbee, Verilog HDL, FPGA, CRC, Bit-to-symbol, Symbol-to-chip, OQPSK.

I. INTRODUCTION

In the past several years, the technologies in the wireless network area have developed rapidly. The need for low-cost, low-power wireless communication systems have increased. Zigbee technology is very suitable for these requirements. Zigbee standard is developed by the Zigbee Alliance [3]. The Zigbee Alliance was formed in 2002 as a non-profit organization open to everyone who wants to join [10]. The physical layer in the zigbee standard can support three bands: 2.45 GHz band, 915 MHz band and 868 MHz band with channels 16, 10 and 1 respectively. Major applications of zigbee focuses on sensor and automatic control such as health care, industrial control, home automation, remote control and monitoring systems[10].

In the zigbee digital transmitter [2], power amplifier is used after the modulation of signals. This will result in the inter symbol interference. Instead of this power amplifier section, a pulse shaping block can be used [1]. So that the inter symbol interference problem can be solved.

The work in this paper is divided into two stages. 1) Design and coding of different blocks in the zigbee transmitter. 2) Simulation and implementation of the transmitter blocks. The blocks in the transmitter section includes: CRC-16 block, bit-to-symbol block, symbol-to-chip block and finally OQPSK block. After the coding these block using Verilog HDL, simulated the code and obtained the results through Xilinx. It is then implemented on Virtex-5 LX50T FPGA.

Paper is organized as follows. Section II describes the blocks in the transmitter section and the flow of input signals through the blocks. Section III describes the design methodology of the transmitter blocks. Section IV presents experimental results showing the waveforms. Finally, section V presents conclusion.

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II. RELATED WORK

The zigbee transmitter blocks are shown in Fig. 1. It consists of CRC-16 generator, Bit-to-symbol block, Symbol-to-chip block and OQPSK block.

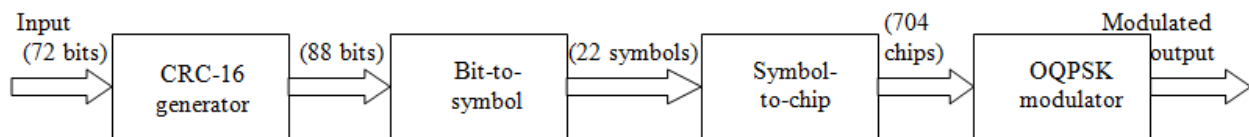


Fig.1. Zigbee transmitter blocks architecture

The working of the transmitter section in Fig. 1 is summarized as follows:

1. CRC-16 generator: This block is implemented using 16 shift registers. All the registers are initialized to zero. Then, input bits are shifted into this registers, starting with LSB. Modulo-2 division is performed in this register arrangement. The remainder after the division process is the CRC checksum value. Those 16 bits are appended with the 72 bits input data and passed it to the next block. So next block will have an input of 88 bits in total.
2. Bit-to-symbol block: Input data have 88 bits, including 16 bits CRC checksum value. In this block, the four LSBs of each octet are mapped into one data symbol. Then the four MSBs are mapped into another data symbol. So the output of this block has 22 symbols.
3. Symbol-to-chip block: This block utilizes DSSS method and each symbol input is mapped into a 32 bits unique PN sequence. So the output will have 704 chips.
4. OQPSK modulator: Last block in the transmitter section is the modulator block. In this work OQPSK modulator is used. It has I-phase carriers and Q-phase carriers. These two carriers are delayed by an amount of T_c . the output of this modulator will have 352 chips for I-phase and Q-phase respectively.

III. DESIGN METHODOLOGY

A transmission is completed successfully only if the transmitted data reaches the receiver end without any errors. Detection and correction of these errors are one of the major sections in a communication system. Cyclic Redundancy Check (CRC) is one of the most reliable error checking methods available. In this work, CRC-16 is used for the error detection. In the generation of CRC, there is a message polynomial and a generator polynomial. The message polynomial is divided using the generator polynomial. The remainder is the Block Check Character (BCC). This BCC is appended with the message and will send to the next block. In the receiver side, the received data will divided with the same generator polynomial. A zero remainder implies that no errors are occurred during transmission. The division in this is performed by modulo-2 division (XOR operation).

The generator polynomial [1] used in this work is

$$P(x) = x^{16} + x^{15} + x^2 + 1$$

CRC-16 generation circuit can be generated using shift registers. It requires 16 shift registers. Fig. 2 shows the CRC-16 generation circuit.

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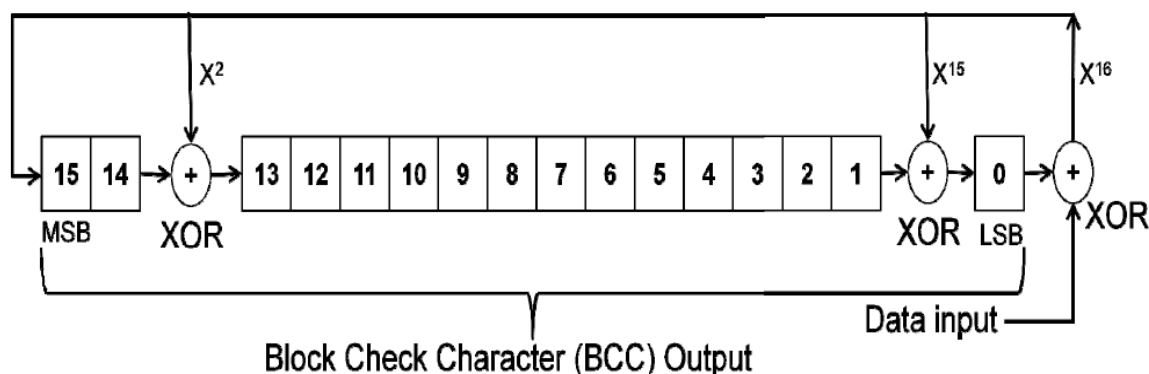


Fig.2. CRC-16 generator circuit [1]

The generation circuit is implemented by using 16 shift registers as shown in Fig. 2. Input 72 bits will give to the CRC-16 generator. The generator will operate according to the CRC polynomial. XOR operation is performed wherever the polynomial terms are valid as shown in Fig. 2. After the operation, 16 bits are generated (BCC). The 72 bits inputs along with these 16 bits are given to the next section.

Outputs from the CRC-16 block along with the input data bits are inserted into the bit-to-symbol block. In this block, each octet is mapped into one data symbol. Each octet of the input is processed through this block sequentially. So the output of this block contains 22 symbols.

Symbol-to-chip block uses DSSS (Direct Sequence Spread Spectrum) technique and maps each symbol from the bit-to-symbol block to a unique PN sequence of 32-bits length [10]. The IEEE 802.15.4 uses this method to improve the receiver sensitivity level and increase the jamming resistance [10]. The DSSS method is also necessary in improving receiver performance in a multipath environment because in most practical scenarios, the transmitted signal may find several different paths to the receiver due to reflections, diffractions and scatterings. These signals have different delays and phase shifts; therefore, the summation will be a distorted signal [12]. Table 1 shows the symbol-to-chip mapping using DSSS method.

Data Symbol (decimal)	Data Symbol (binary) (b0 b1 b2 b3)	Chip Values (c0 c1 c30 c31)
0	0000	11011001110000110101001000101110
1	1000	11101101100111000011010100100010
2	0100	00101110110110011100001101010010
3	1100	00100010111011011001110000110101
4	0010	01010010001011101101100111000011
5	1010	00110101001000101110110110011100
6	0110	11000011010100100010111011011001
7	1110	10011100001101010010001011101101
8	0001	10001100100101100000011101111011
9	1001	10111000110010010110000001110111
10	0101	01111011100011001001011000000111
11	1101	01110111101110001100100101100000
12	0011	00000111011110111000110010010110
13	1011	01100000011101111011100011001001
14	0111	10010110000001110111101110001100
15	1111	11001001011000000111011110111000

Table1. Symbol-to-chip mapping using DSSS [4]

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Symbol-to-chip block in the transmitter section uses the mappings in Table 1 to generate output chips. For each data symbol, there is a corresponding 32 bits chip. Each chip is unique. Implemented this table for obtain the functionality of symbol-to-chip block.

Final block is the OQPSK (Offset Quadrature Phase-Shift Keying) block. This modulator is an improved version of QPSK. There are even-indexed chips and odd-indexed chips. This method processes the in-phase (I-phase) signal with a quadrature-phase (Q-phase) signal, and delayed by half a cycle to avoid sudden phase-shift changes [13].

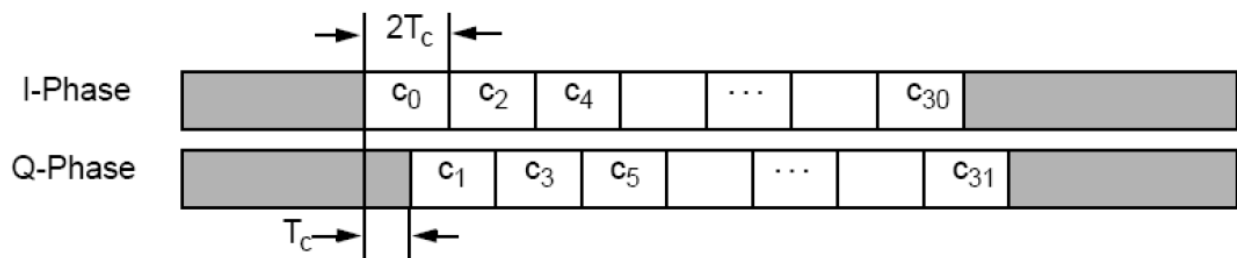


Fig.3. OQPSK chip offsets [14]

As shown in Fig. 3, to form the offset between I-phase and Q-phase chip modulation, the Q-phase chips shall be delayed by T_c with respect to the I-phase chips. T_c is the inverse of the chip rate. The chip rate is nominally 2 Mchip/s which is 32 times the symbol rate [13]. In-phase (I) carrier is used for the modulation of even-indexed chips and quadrature-phase (Q) carrier is for the odd-indexed chips.

IV. EXPERIMENTAL RESULTS

Figures show the simulation results of each block in the transmitter section of zigbee. Figs. 4 (a) shows the output of the CRC-16 block, (b) is the output from the bit-to-symbol block, (c) is the obtained output from the symbol-to-chip block and finally (d) is the output from the OQPSK modulator block.

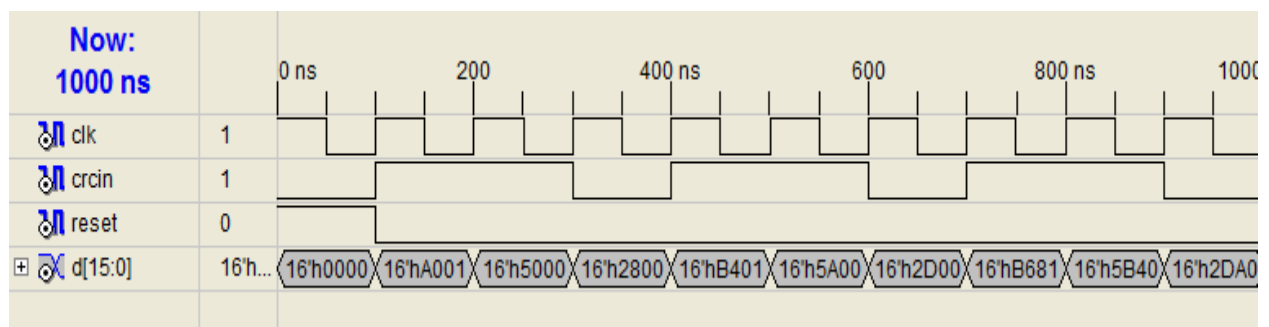


Fig.4. (a) Output simulation waveform of CRC-16 generator

In Fig.4 (a), input signal is represented by crcin. The signal d [15:0] represents 16 bits CRC values. These 16 bits along with the input 72 bits are the input of the bit-to-symbol block.

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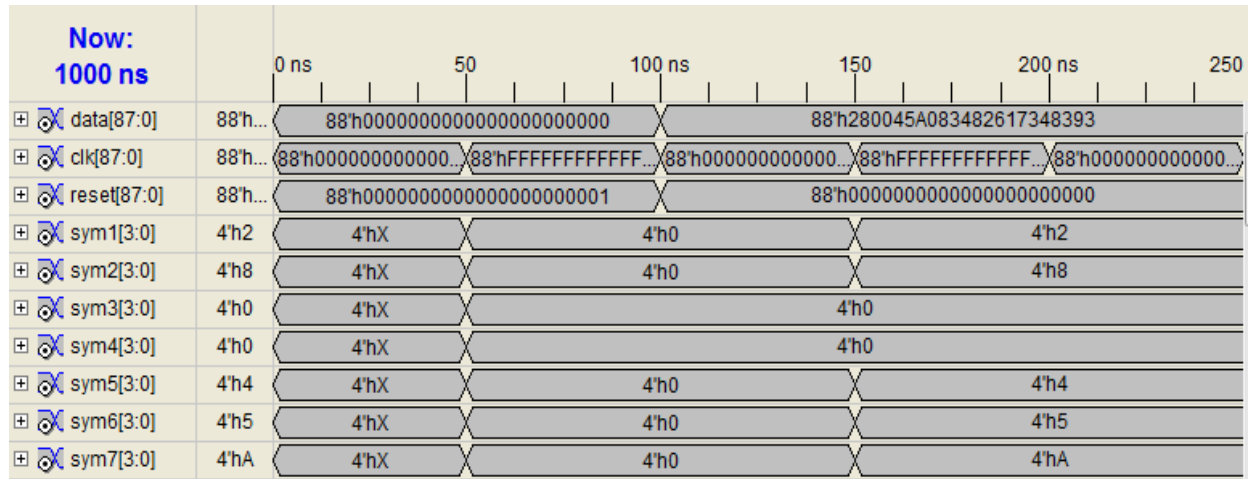


Fig.4. (b) Output simulation waveform of Bit-to-symbol block

The 88 bits inputs are represented by the signal data [87:0] in Fig.4 (b). In the same figure, different symbol outputs are given. Not all the symbols are shown in the figure. In actual case, there are 22 symbols.

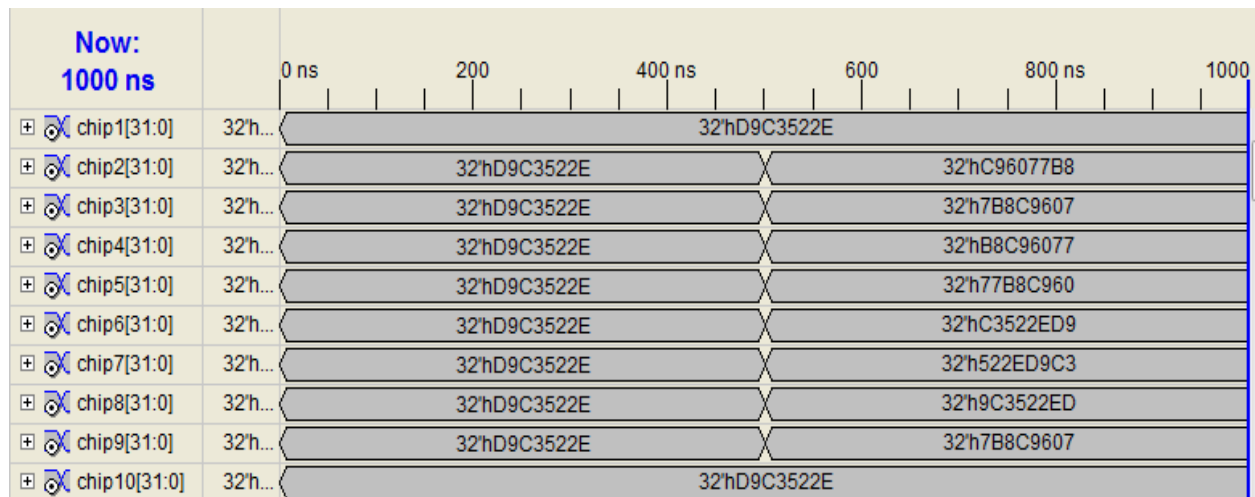


Fig.4. (c) Output simulation waveform of Symbol-to-chip block

In Fig.4 (c) different chip values are shown according to Table 1. Each symbol from the bit-to-symbol block is mapped into unique chips of 32 bits. The output chips from this block have given to the input of OQPSK modulator.

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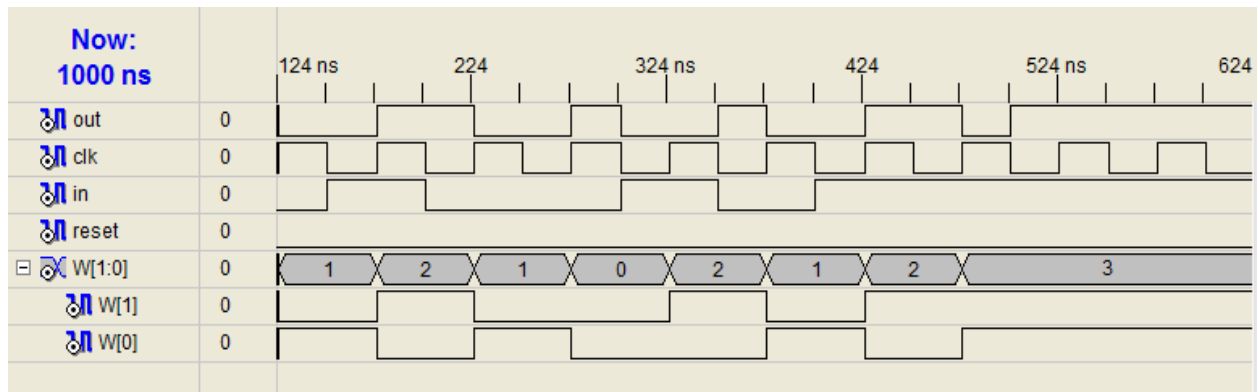


Fig.4. (d)Output simulation waveform of OQPSK modulator

The simulated output of the modulator block is shown in Fig.4 (d). In Fig.4 (d), the signal out gives the simulated output waveform of the OQPSK modulator. This modulated signal is further passed through a pulse shaping block before transmission to avoid inter symbol interferences and other effects of noise. After verifying the working of the transmitter blocks using simulated waveforms, implemented these blocks on Virtex-5 LX50TFPGA.

V. CONCLUSION

This work includes Verilog HDL based design and simulation of Zigbee transmitter blocks and the implementation of these blocks on FPGA. CRC-16 block, Bit-to-symbol block, Symbol-to-chip block and OQPSK modulator block are coded in Verilog HDL and then simulated using Xilinx. Finally these blocks are implemented on Virtex-5 LX50T FPGA.

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BIOGRAPHY



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