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Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials

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ABSTRACT: To extend the use of CMOS technology beyond 14 nm node technology, new device materials are required that can enhance the performance of MOSFETs. The use of high-k materials in double gate (DG) MOSFET can triumph over the problem of power dissipation and leakage current. In this paper, we investigated various high-k dielectrics as the gate oxides in a 12 nm SOI FinFET and the performance potential of SiO₂, SiON, Al₂O₃, Y₂O₃, HfO₂ and La₂O₃ gate dielectrics for Si based DG-FinFET has been explored based on 2-D numerical simulations. The results demonstrate that La₂O₃ can replace SiO₂, SiON, Al₂O₃, Y₂O₃ and HfO₂ owing to its high transconductance, reduced sub-threshold swing (~ 40 %), increased threshold voltage and reduced DIBL (~ 81%).

KEYWORDS: FinFETs, Short channel effects (SCEs); Lanthanum oxide (La₂O₃); Drain induced barrier lowering (DIBL); Subthreshold swing (SS).

I. INTRODUCTION

Over the past few decades, the technology is oriented towards the miniaturization of electronic components and transistors in integrated circuits (ICs). The main aim is to increase the chip density i.e. more transistors per unit area that can improve circuit performance without compromising device manufacturing cost. Gordon Moore in 1965 predicted that the no. of transistors in a chip doubles every two years [1], however, the reduction in the transistor dimension is obstructed by the short channel effects.

Beyond 16 nm technology, the CMOS technology can be implemented with the invention of multigate transistors like FinFET and is considered to be the best candidate to support the subsequent International Technology Roadmap for Semiconductors (ITRS) scaling trends. Multigate FinFET includes double-gate FinFET (DG-FinFET), Tri-gate FinFET (TG-FinFET) and Gate-all-round (GAA) FinFET. Double-gate FinFET has been considered in the present work because of its better gate control over the channel which allows an enhanced device performance [2-4].

FinFET is basically a fin type FET structure and very frequently named as a double-gate transistor. It consists of a thin body of silicon wrapped by gate electrodes or poly silicon layer and the current flows in the channel from source to drain [5]. FinFET has many advantages such as good scalability and excellent electrostatic control with promising performance for the present day nanoscale technology [6]. As DG-FinFET consists of two gates, the gate oxide material plays an important role with regards to device performance. Moreover, as the thickness of SiO₂ reduces below 1.5 nm, the thin gate oxide layer results in direct tunneling of gate leakage current [7] and ultimately results in high power dissipation which can degrade device performance and stability. These crucial issues can be overcome by using high-k dielectric materials which have attracted the semiconductor industry in the past decade due to their great potential for maintaining further down-scaling in EOT (equivalent oxide thickness) with a physically thicker film and a low dielectric leakage current [8-10].

In this work, we report the simulation study of nanoscale double gate n-FinFET with Si channel using various high-k materials such as Silicon dioxide (SiO₂), Hafnium oxide (HfO₂), Silicon oxynitride (SiON), Aluminum oxide (Al₂O₃), Yttrium oxide (Y₂O₃) and Lanthanum oxide (La₂O₃). The effect of high-k dielectrics on the electrical characteristics

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such as threshold voltage (V_{th}), subthreshold swing (SS), transconductance (g_m) and drain induced barrier lowering (DIBL) has been critically studied. After investigation of various high-k dielectrics, it has been observed that La_2O_3 based double-gate FinFET has an excellent capability of enhancing the device performance with the suppression of short channel effects (SCEs).

II. LITERATURE SURVEY

FinFET technology has been born as a result of the relentless increase in the levels of integration. The term FinFET was coined by University of California, Berkeley Researches (Prof. Chenming Hu, Tsu-Jae King-Liu and Jaffrey Bokor), to describe non planar, double gate transistor built on an SOI substrate. FINFET is named so because its structure contains the ultra thin vertical channel that resembles with fins of a fish surrounded by gate along its three sides. The first article on the double-gate MOSFET transistor was published by T. Sekigawa and Y. Hayashi in 1984. The paper reveals that one can obtain significant reduction in short channel effects by sandwiching a fully depleted SOI device between two gates electrodes internally connected. SOI FinFETs with thick oxide on top of fin are called “Double- gate” and device with thin oxide on top as well as on sides are called “Triple-gate FinFET. There are two types of DG-FinFETs such as symmetric and asymmetric. The device with two gates of identical work function is known as symmetric DG-FinFET and device with two gates of different work function is known as asymmetrical DG-FinFET [11].

Gate oxide material plays an important role in determining the device performance and can meet the demand of low current while keeping power consumption under control. The semiconductor industry has made a tremendous effort to introduce high-k dielectric material in double-gate transistor manufacturing process. The 2010 ITRS (International Technology Roadmap for Semiconductor) update clearly explained that we are progressing towards high-k dielectric materials that will soon replace SiO_2 in the MOSFET. The 2003 ITRS Edition states that “The gate dielectric has emerged as one of the most difficult challenges for future device scaling”. Indeed, the conventional gate dielectric SiO_2 obviously cannot survive the challenge of an $EOT = 2$ nm. Successful integration of high-k materials as gate dielectric gives a remarkable results with regards to double gate transistor. Unlike conventional SiO_2 dielectric, where short channel effects was a serious problem, high-k materials can replace such low-materials i.e. SiO_2 with improved performance of double-gate transistors. So, it is highly preferable to make use of materials with high-k dielectric constant and lesser physical thickness in the modern FinFET devices [12].

III. DEVICE STRUCTURE AND SIMULATION DETAILS

The schematic structure of double gate FinFET used in the simulation work is shown in Fig. 1.

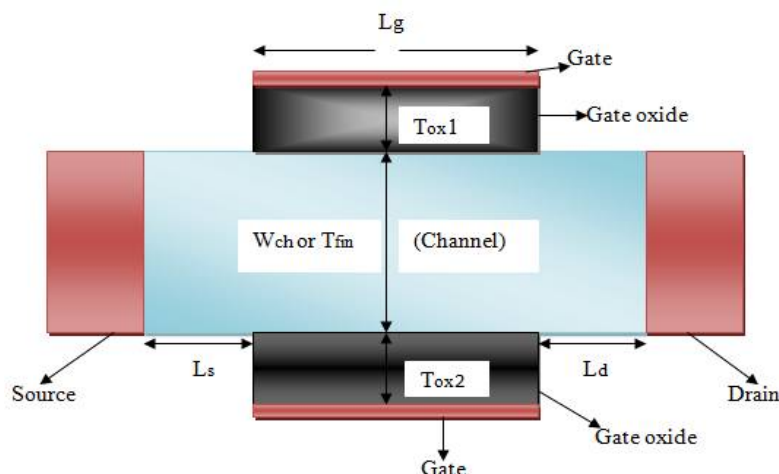


Fig. 1. Two dimensional double gate n-FinFET structure

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The DG-FinFET structure can be characterized in terms of fin length (L_g) and fin thickness (T_{fin} or W_{ch}). Here, the channel is of silicon material with N-type doping concentration of $1e+16 /cm^3$, whereas doping concentration of drain/source is $1e+16/cm^3$ and oxide thickness is 2 nm. The value of the gate contact work function is 4.6 eV and the band gap of Si is 1.12 eV at 300 K. The device simulations have been carried out using PADRE simulator from MuGFET, which is based on the drift-diffusion theory and provides self consistent solution to the Poisson and drift-diffusion equations. Infact, drift and diffusion simulations are significantly faster than quantum ballistic simulations and also fairly well fitted to experimental results. Moreover, it includes hot-carrier transport by solving energy balance equation and the velocity of carriers in the channel region is fitted to the Monte Carlo simulation results [13].

The associated high-k values for various gate dielectric materials are given in Table 1 and the parameters used for the present simulation work are shown in Table 2.

Table 1: Dielectric constant values for various dielectric materials

Dielectric Materials	Dielectric Constant (K)
SiO ₂	3.9
SiON	7.9
Al ₂ O ₃	9
Y ₂ O ₃	15
HfO ₂	25
La ₂ O ₃	30

Table 1 shows the different dielectrics materials with their associated dielectric constants. Among these materials, Hafnium oxide (HfO₂) is often used because of its low leakage current property. However, when compared with other high-k oxides, it suffers from the drawback of low crystallization temperature. So, an alternative is needed which can give better outcome and overcome such drawback. Infact, the analysis of different materials has suggested Lanthanum oxide (La₂O₃) as a better option for double gate FinFET device relative to the other high-k materials.

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Table 2: Parameters used in simulation

Device parameters	Values
Length of the gate (L_g)	12 nm
Equivalent oxide thickness (EOT) T_{OX1}, T_{OX2}	2 nm
Fin width (W_{ch})	10 nm
Extension length to source/drain (L_s & L_d)	20 nm
Channel doping	$1e+16/cm^3$
Drain/source Doping	$1e+19/cm^3$
Channel doping type	N

The different parameters of the designed structure are shown in table 2, since various dielectric material are being considered to meet the improved result of various electrical characteristics of double gate n- FinFET, the choice of the material to be used as gate oxide in such devices will be depend on that which of the material provides improvement in the electrical characteristics of such device as according to device structure parameter variations.

IV. RESULTS AND DISCUSSION

In this section, we present various results pertaining to gate dielectric materials such as SiO_2 , SiON, Al_2O_3 , Y_2O_3 , HfO_2 and La_2O_3 for Si based DG-FinFET.

3.1. Threshold Voltage (V_{th})

Maintaining higher threshold voltage is a key requirement for low standby power (LSTP) logic technologies and the main cause for threshold voltage rolls off is charge sharing. The threshold voltage (V_{th}) variations for various high-k dielectric materials are shown in Fig. 2. From the graph, it can be seen that the threshold voltage values for SiO_2 , SiON, Al_2O_3 , Y_2O_3 , HfO_2 and La_2O_3 are 0.17 V, 0.32 V, 0.34 V, 0.38 V, 0.41 V and 0.42 V respectively. The higher value of V_{th} is obtained for La_2O_3 , thereby, resulting in 147% improvement in comparison to SiO_2 as gate dielectric. As the length of the channel is shortening in CMOS devices, the threshold voltage (V_{th}) begins to decrease because the charge in the depletion region is supported by the drain and the source also. In this case, gate needs to support less charge in the region and as a result V_{th} falls down, thereby degrading device performance. This phenomenon is known as charge sharing effect. The Threshold voltage (V_{th}) expression of MuGFET device can be expressed as [3]:

$$V_{th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{ss}}{C_{ox}} + V_{in} \quad (1)$$

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Where, Φ_{ms} represents metal-semiconductor work function difference between the gate electrode and the semiconductor, Φ_f is the Fermi potential, Q_D is the depletion charge in the channel, C_{ox} is the gate capacitance and Q_{ss} represents charge in the gate dielectric.

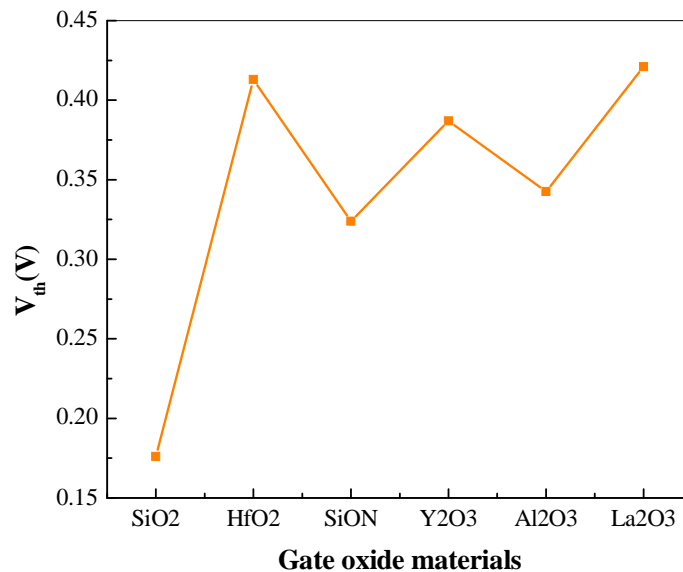


Fig. 2. Threshold voltage variation for different gate dielectric materials at $V_D = 1$ V.

3.2 Subthreshold Swing (SS)

One of the major parameters for a MOSFET device is subthreshold swing (SS) which determine the holding time in dynamic circuits and static power dissipation in static CMOS circuits. SS is a parameter for the calculation of leakage current and it can be expressed by the following equation [3]:

$$SS \text{ (mV/dec)} = \frac{dV_{GS}}{d(\log_{10} I_{DS})} \quad (2)$$

For a MuGFET, typical value for SS parameter is 60 mV/decade i.e. 60 mV change in gate voltage brings about a tenfold change in drain current.

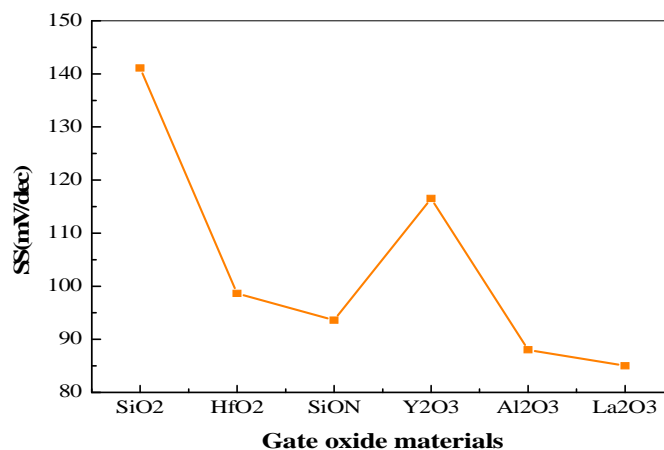


Fig. 3. Subthreshold slope variation for different gate dielectric materials at $V_D = 1$ V.

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Fig. 3 shows the subthreshold swing variation for different high-k dielectric materials at $V_D = 1$ V. The SS values for SiO_2 , SiON , Al_2O_3 , Y_2O_3 , HfO_2 and La_2O_3 are found to be 141 mV/dec, 94 mV/dec, 88 mV/dec, 117 mV/dec, 99 mV/dec and 85 mV/dec respectively. La_2O_3 shows 40% reduction in subthreshold swing relative to SiO_2 as gate oxide for Si based double-gate FinFET having gate length of 12 nm. The reason behind the reduced SS for La_2O_3 is its higher dielectric constant (~ 30) and reduced leakage current. Additionally, high-k value leads to increase in the capacitance between the channel and the gate, which results in less leakage current between drain and gate and further improves the subthreshold swing.

3.3. Drain Induced Barrier Lowering (DIBL)

Another short channel effect is DIBL and is defined as the reduction in the potential barrier when the drain voltage is increased. The value of the drain induced barrier lowering (DIBL) is calculated by using following expression [14]:

$$\text{DIBL (mV/V)} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (3)$$

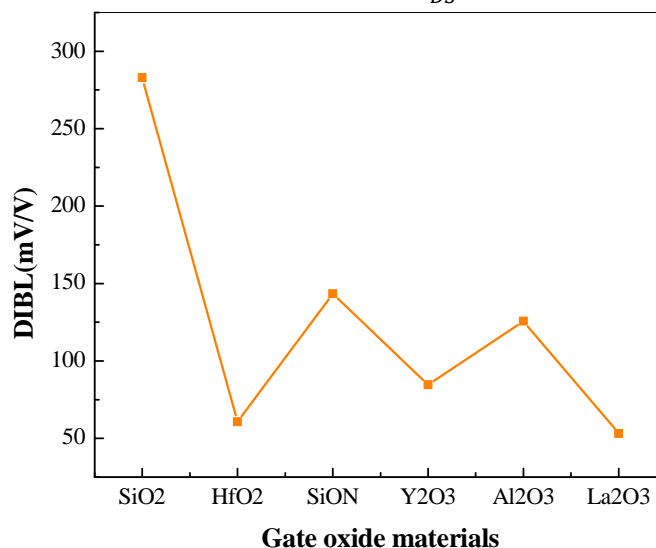


Fig. 4. DIBL variation for different gate dielectric materials at $V_D = 1$ V.

Fig. 4 shows the DIBL variation for different high-k dielectric materials at $V_D = 1$ V. The DIBL values for SiO_2 , SiON , Al_2O_3 , Y_2O_3 , HfO_2 and La_2O_3 are found to be 283 mV/V, 143 mV/V, 126 mV/V, 85 mV/V, 61 mV/V and 53 mV/V respectively. La_2O_3 has shown 81% reduction in DIBL in comparison to SiO_2 as gate oxide material for DG-FinFET. Infact, the DIBL value for La_2O_3 is quite appreciable and reveals that it exhibits better gate control over the channel relative to other dielectric materials. Moreover, it has been seen that with the reduction in the source junction barrier, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current. That's why oxide materials having high dielectric constant values are preferred for nanoscale devices.

3.4. Transconductance (g_m)

The Transconductance (g_m) quantifies the drain current variation with a gate source voltage variation while keeping drain source voltage constant [15] and can be calculated by the following relation:

$$g_m = \frac{d I_D}{d V_{GS}} \quad (4)$$

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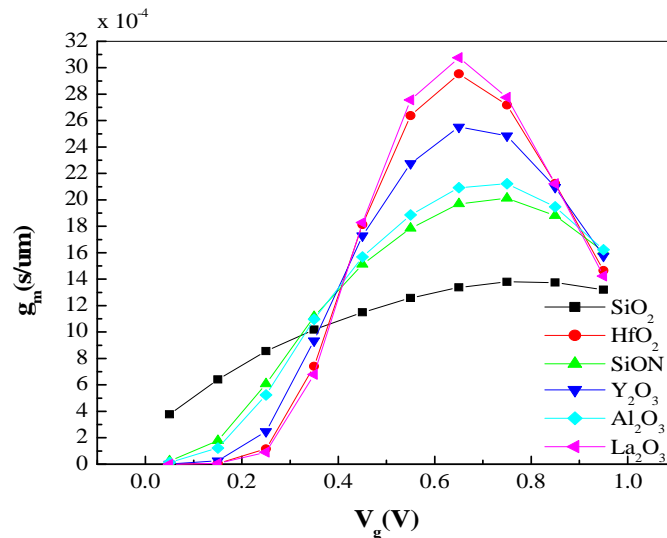


Fig. 5. Transconductance variation for different gate dielectric materials at $V_D = 1$ V.

Fig. 5 shows the transconductance variation with respect to gate source voltage for various high-k dielectric materials at $V_D = 1$ V. From the graph, it is clear that the values of transconductance for SiO₂, SiON, Al₂O₃, Y₂O₃, HfO₂ and La₂O₃ are found to 13.39×10^{-4} S/μm, 20×10^{-4} S/μm, 21×10^{-4} S/μm, 26×10^{-4} S/μm, 30×10^{-4} S/μm and 31×10^{-4} S/μm respectively. La₂O₃ shows 132 % increase for transconductance in comparison to SiO₂ and has the capability of keeping drain current under control with respect to gate bias and further enables faster carrier transport with 12 nm gate length.

IV. CONCLUSIONS

Performance analysis of DG-FinFET based on SiO₂, SiON, HfO₂, Al₂O₃, Y₂O₃ and La₂O₃ gate dielectrics for 12 nm node technology has been studied using numerical simulations. La₂O₃ demonstrates high transconductance, better threshold voltage, reduced SCEs such as sub-threshold swing and DIBL and is amongst the best when compared to the other gate dielectric materials. Additionally, La₂O₃ based DG-FinFET shows improved device performance, better gate control over the channel, effective reduction of the leakage current and could offer high amplification values to meet the predictions and goals set by the international technology roadmap for semiconductors (ITRS).

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