

Design of $\Delta\Sigma$ DAC for SAR ADC

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ABSTRACT: SAR ADC plays an important role in converting the analog signal to digital signals in applications which require moderate speed, resolution, and low power operation at lower cost. Limitation associated with conventional SAR ADC is its resolution. This is because of the capacitive DAC employed. As the resolution of ADC increases, the number of capacitors required for the DAC will also increase, this will lead to a lot of mismatch between the capacitors during the fabrication process. The mismatch in the capacitors causes non-linearity errors, more area is required to accommodate more number of capacitors and also consumes more power. Hence to overcome this limitation of resolution associated with SAR ADC, a different architecture of DAC is proposed and it is referred to as $\Delta\Sigma$ DAC. In $\Delta\Sigma$ DAC, the digital bits generated from SAR logic are converted into bit streams. The bit stream is used to estimate the corresponding analog voltage with the help of an analog computation block. The working principle of $\Delta\Sigma$ DAC is analyzed and verified using a Verilog model. Building blocks needed to implement the 3-bit $\Delta\Sigma$ DAC are discussed, implemented in SPICE and the simulation results are documented. This paper consists of a detailed description of the working principle of $\Delta\Sigma$ DAC, implementation and partial results of $\Delta\Sigma$ DAC.

KEYWORDS: $\Delta\Sigma$ DAC, ADC, Bit stream.

I. INTRODUCTION

The conventional SAR ADC employs a charge distribution capacitive DAC. The limitation of the charge distribution capacitive DAC is that the number of capacitors used for each bit of DAC input. The resolution of DAC which is used in N-bit SAR ADC should be the same as N-bit. As the resolution of ADC increases, the number of capacitors used for DAC will also increase. This will lead to a lot of mismatch occurring between these capacitors during the fabrication process, increased power consumption in charging and discharging these capacitors. To overcome this limitation with the capacitive DAC, a new architecture of DAC is introduced which is referred to as $\Delta\Sigma$ DAC. The idea behind the $\Delta\Sigma$ DAC is to produce a stream of bits corresponding to given N-bit data input and charge a single capacitor to a voltage level which can be mapped to an analog voltage corresponding to given digital input bits.

II. ARCHITECTURE

Proposed architecture is called as $\Delta\Sigma$ DAC, which is designed to achieve higher resolution for SAR ADC architecture by replacing the capacitive DAC.

1. **$\Delta\Sigma$ DAC:** Fig.1 shows the block diagram of $\Delta\Sigma$ DAC. It consists of two blocks such as $\Delta\Sigma$ modulator and an analog value computation block. The input bits are converted into a bitstream by the modulator and then it will be quantized to a stable analog voltage by the analog value computation block.

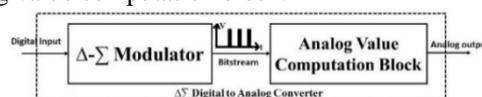


Fig.1 Block diagram of $\Delta\Sigma$ DAC

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2. **$\Delta\Sigma$ Modulator:** Fig.2 shows the block diagram of $\Delta\Sigma$ modulator. Major building blocks of $\Delta\Sigma$ Modulator are Δ Adder, Σ Adder, Σ Register and Δ Sequence Generator. Function of $\Delta\Sigma$ modulator is to take the digital input of N-bits and convert them in to a bitstream.

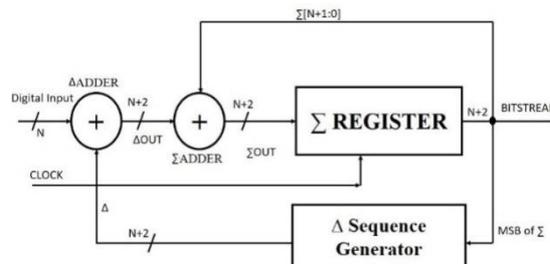


Fig. 2 Block diagram of $\Delta\Sigma$ Modulator

- A. **Δ Adder:** This will calculate the sum of the Δ sequence and input data DACIN. The Δ sequence is generated based on the content of the MSB of Σ Register. If the content of the MSB of Σ Register is '0', then Δ is an N+2-bits number with all '0's otherwise its two '1's concatenated as MSBs to an N bit number of all '0's.
- B. **Σ Adder:** This will calculate the binary addition of Δ OUT and the data in Σ Register represented as Σ . The result will be updated in Σ Register.
- C. **Σ Register:** This is the block which will latch the output of Σ Adder back to Σ Adder in the next clock cycle to produce the stream of bits. MSB of the Σ Register is taken out as a single bit of bitstream at every clock cycle. The bitstream taken out of Σ Register at every clock cycle is used to quantize as analog output voltage. For example for a data input '011', the output of $\Delta\Sigma$ modulator would be '0100101'. Using this bitstream it is possible to quantize the analog voltage using a special circuit presented in subsequent section of the paper.
- D. **Δ Sequence Generator:** Δ Sequence generator is used to generate two bits of a sequence used for the computation. Δ Sequence is N+2-bits. Out of N+2-bits, MSB and the lower bit next to MSB are dependent on the status of MSB of Σ Register. Hence the function of Δ sequence generator is to set of rest the MSB and the lower bit of MSB of Δ sequence. Rest of the bits are '0' always.

The working principle of $\Delta\Sigma$ modulator can be explained by considering a 3-bit $\Delta\Sigma$ modulator. At time T_0 , the value of Σ Register is initialized to '10000'. Δ is the output of Δ sequence generator. Δ OUT is output of Δ adder which is added with data in Σ register with the help of Σ adder. Σ OUT is the output of Σ adder which will be stored in Σ register. During the next clock cycle, based on the status of MSB of Σ Register, Δ sequence will be generated and used for the calculation of the next pulse of the bitstream. For the given DAC input '011', the bitstream output from time T_0 to T_7 has three logic high pulse. The ratio of on-time to frame time is 3/8. Hence output voltage of analog computation block will be $3 \cdot FS/8$.

Table.1 shows the truth table of a 3-bit $\Delta\Sigma$ modulator. DACIN is the input bits given to the modulator. For a 3-bit modulator, input data is of 3-bits. But as per the logic, 5-bits are considered. Hence the 3-bit data input is converted to 5-bits by attaching two '0's to the MSB without altering the data. Table.1 describes the steps involved in generating bitstream for an input '011' in detail.

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Table.1 Truth table for $\Delta\Sigma$ modulator with input '011'

	TIME								
	T ₀	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	T ₇	T ₈
DACIN	00011	00011	00011	00011	00011	00011	00011	00011	00011
Δ	11000	00000	00000	11000	00000	00000	11000	00000	11000
Δ_{OUT}	11011	00011	00011	11011	00011	00011	11011	00011	11011
Σ	10000	01011	01110	10001	01100	01111	10010	01101	10000
Σ_{OUT}	01011	01110	10001	01100	01111	10010	01101	10000	01011
BITSTREAM	1	0	0	1	0	0	1	0	1

Table.2 shows the bitstream for all the different inputs combination for a 3-bit DAC and their corresponding output voltage is tabulated. Since DACIN is 3-bit data, there are eight different combination of input data as tabulated in the first column of Table.2. For all these eight different input combinations, there will be different bitstream with corresponding number of '1's used to charge the capacitor in the analog value computation block produces different analog output voltage.

Table.2 mapping of 3-bit DACIN to analog voltage

DACIN	Decimal Value of DACIN	DACOUT(BITSTREAM)	Analog Output Voltage (FS=VREF)
000	0	00000000	0
001	1	00000010	FS*/8
010	2	00100010	(2*FS)/8
011	3	01001010	(3*FS)/8
100	4	10101010	(4*FS)/8
101	5	10110110	(5*FS)/8
110	6	11101110	(6*FS)/8
111	7	11111110	(7*FS)/8
1000	8	11111111	FS

Output of Modulator after T₂ time period is used for generating the Analog voltage using a special circuit called Analog value computation block.

3. **Analog Value Computation Block:** Fig.3 shows the block diagram of analog value computation block consists of two inputs and one output ports. Bitstream is the stream of bits generated from the modulator and IREF is the reference current used to charge the capacitor to calculate the analog output voltage corresponding to bitstream. Function of the Analog Value Computation Block is to quantize the bit stream generated by the $\Delta\Sigma$ modulator. FS is the full scale voltage of DAC which will be divided into number of levels to given digital input into a stable analog voltage as described in Table.2 Considering the 3-bit DAC, the full scale voltage is divided into 8 different levels. The smallest voltage difference is known as 1LSB = FS/2^N. The Analog Value Computation Block will read the bitstream generated by the $\Delta\Sigma$ modulator and it will keep on integrating this 1LSB voltage whenever there is a '1' in the bitstream.

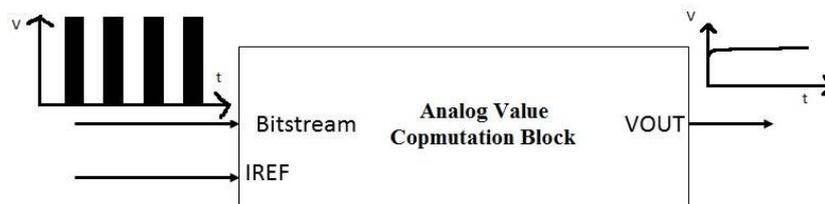


Fig.3 Block diagram of Analog Value Computation Block

In Analog Value Computation Block, a reference current is used to charge the output node whenever logic ‘1’ arrives in the bitstream as shown in Fig.3 The Analog Value Computation Block can be implemented by using a capacitor which will be charged using a constant current source through a switch. The gate of the switch will be driven by bitstream generated by $\Delta\Sigma$ modulator.

III. IMPLEMENTATION

In order to implement the $\Delta\Sigma$ DAC, its working principle of modulator is verified by developing a Verilog model of the 3-bit modulator and verified for different inputs using the flowchart as shown in Fig.4

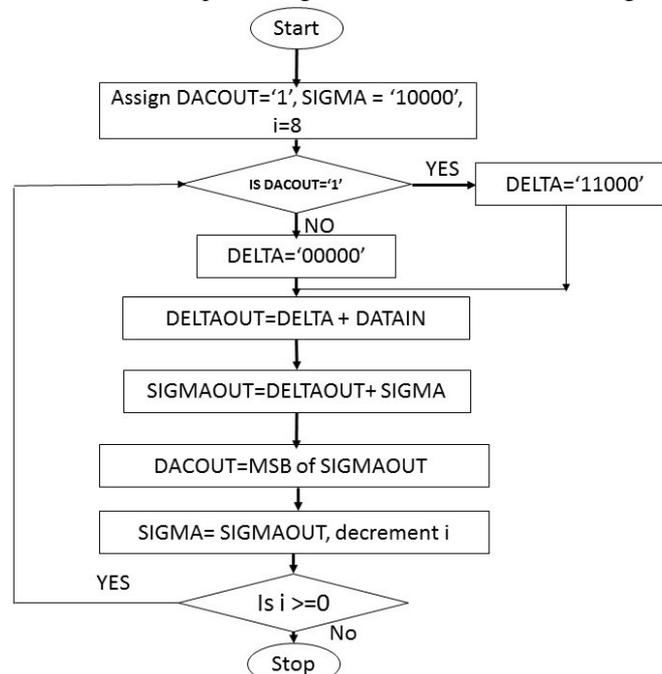


Fig.4 Flowchart used to develop Verilog model for $\Delta\Sigma$ Modulator

Fig.4 shows the flow chart developed for a 3-bit modulator which will produces the stream of bits. As described in the flow chart the loop is executed for 9 times. That means for a 3-bit modulator to produce the bitstream 9 clock cycles are required. After 9th clock cycle, the registers will be initialised as per the required logic. Once the desired output is obtained from the Verilog model of $\Delta\Sigma$ modulator with different input bits, it is implemented in SPICE level using LTSpice tool.

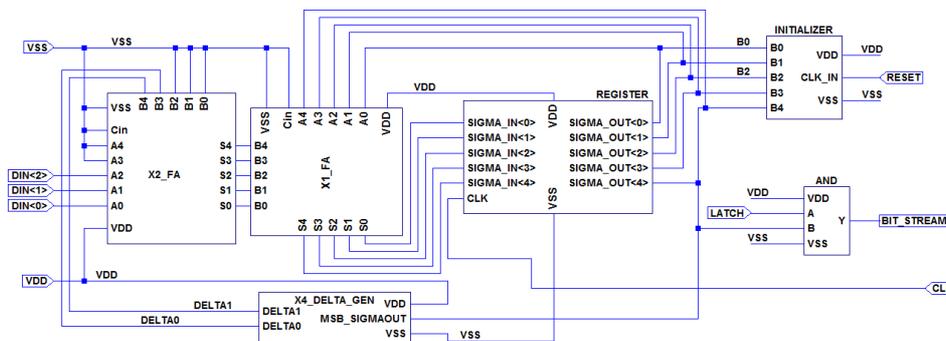


Fig.5 Schematic diagram of $\Delta\Sigma$ modulator

Fig.5 shows the schematic diagram for the 3-bit $\Delta\Sigma$ modulator. This model consists of the two 5-bit Full adders, Σ register and Δ sequence generator. Function of the modulator is to convert the given digital input bits into a bitstream. This 3-bit modulator will generate the bitstream of 7 pulse. Digital input bits are fed to the first adder which is 5-bit full adder. This adder is referred as the Δ adder which will add the Δ sequence of 5-bits generated by Δ sequence generator and the input digital bits. The output of Δ adder is referred as the Δ OUT. The second 5-bit adder is referred as Σ adder which will add the Δ OUT and the output of Σ register resulting in 5-bit data. The output of the Σ adder is given to the Σ register which will latch its data back into the Σ adder as input upon the arrival of the next clock pulse. During the first clock pulse of the modulator, SIGMA_OUT<4:0> are set as '10000'. This is the initialization phase. Upon the arrival of the next clock pulse the Δ sequence generator will produce output bits DELTA0, DELTA1 as '110000'. This will be the input to the Δ adder.

1. 5-bit Full Adder

Fig.6 shows the block diagram for 5-bit full adder which is designed using five 1-bit full adder blocks and connecting them in series. Cout of first full adder is connected to the Cin of next full adder circuit. This type of adder is referred as ripple carry adder. In order to analyse and implement the working principle of $\Delta\Sigma$ DAC, 3-bit of $\Delta\Sigma$ modulator is analysed. This requires two 5-bit full adders to perform the addition process by Δ adder and Σ adder.

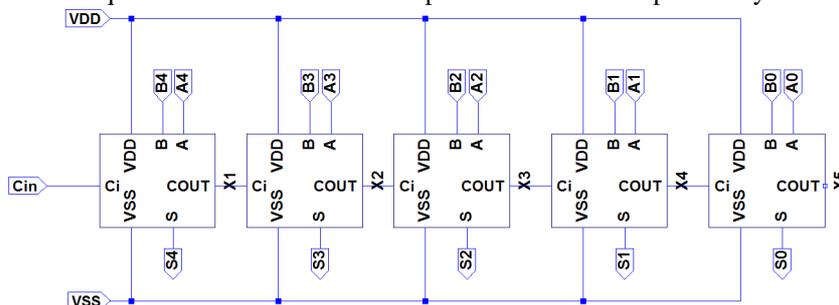


Fig.6 Schematic diagram of 5-bit ripple carry adder

2. 1-bit Full Adder

Function of full adder is to perform the binary addition of inputs and produce two outputs namely sum and carry. 1-bit full adder performs addition operation on three inputs of one bit each and produces two outputs which are Sum and Carry. A full adder can be constructed using two half adders cells which are connected to input A and B of one half adder and other is being connected to sum. Each of these two half adders has Cin as one of the three inputs.

$$S = A \oplus B \oplus C$$

$$C_{out} = AB + BC + CA$$

$$C_{out} = C(A + B) + AB$$

$$S = ABC_{in} + \bar{C}_{out}(A + B + C)$$

Fig.7 shows the simplified circuit diagram for a cmos full adder. C_{out} and S are the carry and sum outputs of full adder and A , B and C_i are the inputs for the full adder. VDD and VSS are the power and ground nets respectively.

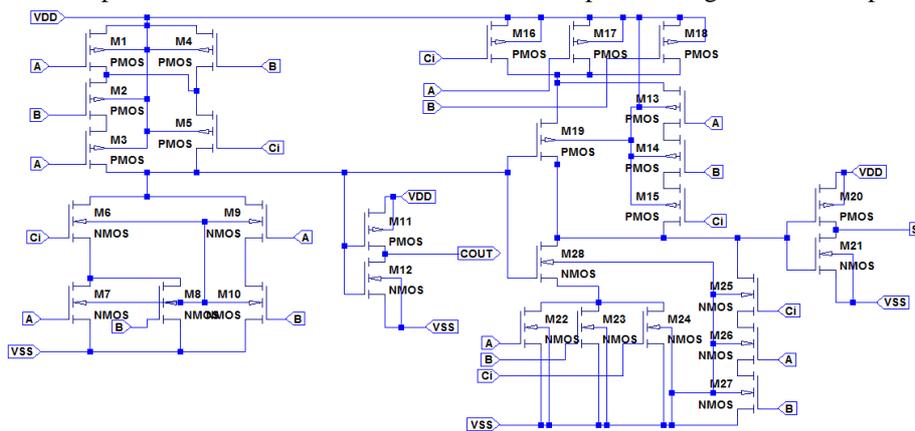


Fig.7 Simplified circuit diagram of 1-bit full adder

3. Σ Register

Σ Register will be acting as a 1-bit data holder which will hold the data till the arrival of next clock pulse. Once the Σ adder gives the sum of the ΔOUT bits and the previously stored content of Σ register, this output of Σ adder will be updated in the Σ register and it will remain same till the next clock pulse.

Fig.8 shows the circuit diagram for 5-bit Σ register implemented using a D flip-flop for each bit of the register and driven by same clock pulse. Once the clock pulse arrives at the D flip-flop gate, this will latch the output of Σ adder into the register.

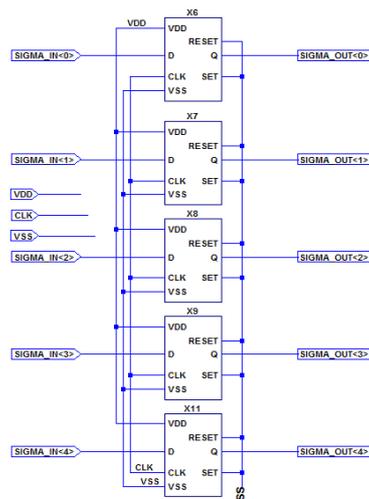


Fig.8 Schematic diagram for Σ Register

In Fig.8, $SIGMA_IN<0:4>$ are the input bits generated by the Σ adder and $SIGMA_OUT<0:4>$ are the output bits of the register which are going to be treated as the input for Σ adder in the next clock pulse.

4. D Flip-Flop

The basic building block of most of the sequential circuits such as shift register and counter is D flip-flop. It is very important discuss the D flip-flop circuit. Table.3 is the truth table for D flip-flop with SET and RESET control signals. D flip-flop consists of D, CLK, SET and RESET as input pins. Q is the output pin.

Table.3 Truth table for D flip-flop

CLK	D	SET	RESET	Q
X	X	0	1	0
X	X	1	0	1
1	1	0	1	0
1	1	1	0	1
1	0	0	0	0
1	1	0	0	1
0	X	0	0	No Change

Circuit diagram for D flip-flop is shown in the Fig.9 consists of four transmission gates and four 2-input OR gates. The OR gates are used to update the Q output based on the SET and RESET inputs.

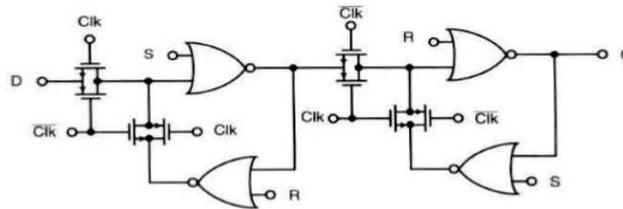


Fig.9 Circuit diagram of D Flip-Flop

Fig.9 shows the circuit diagram of the Master-slave D Flip-flop. Both master and slave section composed of 2 transmission gates, 2 OR gates each. Master will be enabled in the negative cycle of the clock whereas the slave section will be enabled in the positive clock cycle. Such arrangement is needed to transfer the data in the presence of clock and hold the data in the absence of the clock signal. Fig.10 shows the circuit diagram for D flip-flop which is implemented in the SPICE level.

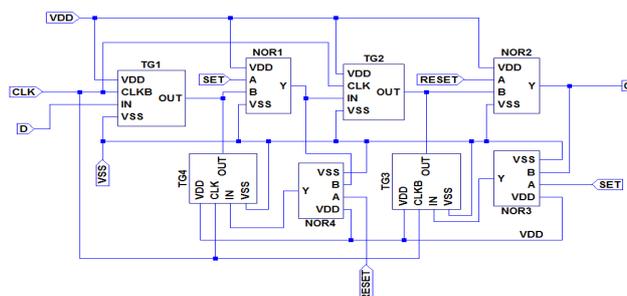


Fig.10 Implemented schematic diagram of D Flip-Flop

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5. Analog value Computation Block

Function of Analog Value Computation Block is to convert the stream of bits generated by the $\Delta\Sigma$ modulator into a stable analog voltage. Changing a capacitor by using a current source controlled by switch is employed to implement this block. Whenever a constant current source connected to capacitor, the current source will pump the charges on to the top plate of the capacitor in a linear manner. This will build potential across the capacitor. The voltage developed across the capacitor can be treated as a stable analog voltage.

The relation between the current I, voltage V and the Capacitance C is given as

$$I = C \frac{dV}{dt}$$

Where, I is the current, C is the capacitance, dv is the differential voltage

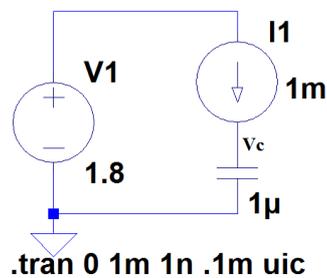


Fig.11 Circuit diagram for charging a capacitor by current source

The differential voltage developed across the capacitor in a specified time period is dV/dt . I is the resultant current because of the voltage potential across the capacitor at time dt. Using this relation, amount of current required to charge this capacitor C up to the voltage values V is calculated. Where V is the final voltage developed across the capacitor after the time period T. Hence dV/dt can be referred as small change in the voltage in a small time period. After T unit of time, the voltage developed across the capacitor C will be V unit by using a constant current source I A.

Fig.11 shows the schematic diagram for analysing phenomenon of charging the capacitor with a current source. The parameters such as I, dV, dt are assumed as $I=1\mu A$, $dV=0.1V$, $dt= 0.1msec$ and required capacitor is calculated to achieve the final desired voltage across the capacitor. Fig.12 shows the output waveform a capacitor charged by current source. V1 is supply voltage, I1 is the current and v_c is voltage across the capacitor.

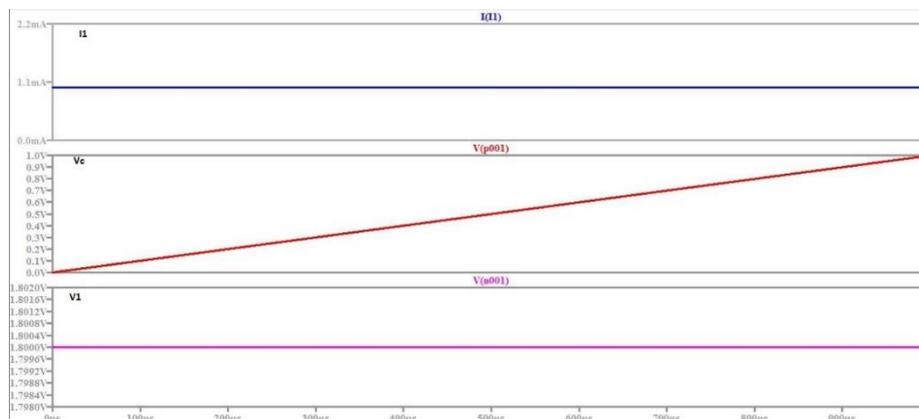


Fig.12 Output waveform of charging a capacitor by current source

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This basic idea of charging a capacitor with current source can be employed to convert the bitstream generated by the $\Delta\Sigma$ modulator into an analog voltage by having PMOS switch connected in between the current source and the capacitor. The gate of this PMOS switch is driven by the bitstream from the $\Delta\Sigma$ modulator.

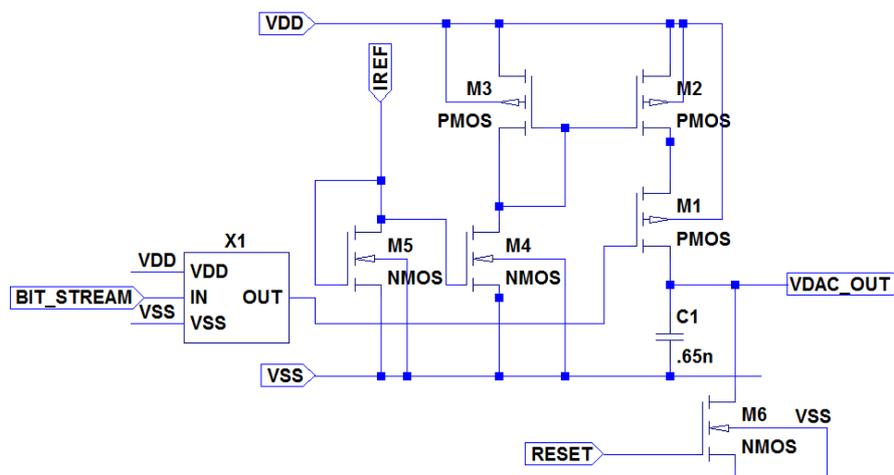


Fig.13 Circuit diagram of Analog value computation block

In the Fig.13 PMOS M1 is a switch which will control the charging of the capacitor by the current source in accordance with its gate voltage. Here the bitstream from the modulator will control the charging of capacitor. M2 and M3 are the PMOS transistors forming a current mirror to mirror the constant current from the current source. Once the bitstream is applied to the gate of PMOS switch which is controlling the charging, whenever there is a high pulse in the bitstream, the PMOS switch will be on and it will allow the charges to accumulate on the plate of the capacitor which will result in a voltage developed across the capacitor. Whenever there is low pulse in the bitstream, PMOS switch will turn off and disconnect the capacitor from the current source. During this time, for an ideal case there will not be any leakage of the charges from the capacitor. Hence for every high pulse in the bitstream, there will be small voltage developed across the capacitor which can be referred as the 1LSB voltage of the DAC. This is the differential voltage developed at each interval time of high pulse in the bitstream

Considering a data input '011' applied to the $\Delta\Sigma$ modulator. As a result the modulator will produce the bit stream can be represented as '01001010'. This bit stream consists of three '1's. Hence as per the $\Delta\Sigma$ logic, corresponding analog voltage of DAC is given as

$$V_{out} = \frac{3FS}{2^N}$$

Where, V_{out} is the output voltage, FS Full scale voltage of DAC and N is the number of bits. Assuming FS as 1.8 V and N as 3, the final analog voltage V_{out} corresponding to digital data '011' would be .675V. In the bitstream corresponding to the data input '011', there are three 1s. Hence there will be three high pulse in the bitstream and the capacitor will be charged for three unit of time. This can be represented as 3dv. Hence dv can be calculated using the full scale value of DAC and the resolution of DAC as,

$$dv = \frac{FS}{2^N}$$

For a particular FS, N and the dt, capacitor and the required current can be chosen to implement the Analog value computation block to convert the bitstream into a stable analog voltage.

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IV. TESTS AND RESULTS

In order to analyse the functionality of $\Delta\Sigma$ DAC, its divided into two major blocks namely $\Delta\Sigma$ Modulator and the Analog Value Computation Block. These two blocks are designed, tested individually and then they are integrated to have the complete working model of $\Delta\Sigma$ DAC.

1. 3-bit $\Delta\Sigma$ Modulator



Fig.14 Block diagram for 3-bit $\Delta\Sigma$ Modulator

Fig.14 shows the block diagram of $\Delta\Sigma$ Modulator used to decide the ports in developing Verilog model of $\Delta\Sigma$ Modulator which is simulated by giving the input data as '011'. In the first clock cycle, bits of the Σ Register are initialized as '10000'. After the second clock pulse, the MSB of the Σ Register will be taken as the individual bit of the bitstream. Hence for DIN='011' expected output bit stream would be '010010'. Fig.15 shows the simulation result of modulator with input '011'.

Table.4 is tabulated with different input and output ports used in $\Delta\Sigma$ Modulator. DIN<2:0> is the data input port with 3-bit, CLK is the clock signal and BITSTREAM is the output of the modulator.

Table.4 IN/OUT Signal details of $\Delta\Sigma$ Modulator

SIGNAL	MODE	DESCRIPTION
DIN<2:0>	INPUT	DATA input
CLK	INPUT	Clock signal for Modulator
COUNT	OUTPUT	Indicates the end of process
BITSTREAM	OUTPUT	Stream of output bits

Fig.15 shows the simulation result of 3-bit $\Delta\Sigma$ Modulator with DIN as '011'. It is observed that the first two clock pulses are used to initialise the content of Σ register and after third clock pulse, the MSB of the Σ register is taken out as the stream of bits. For the given test case the input applied is '011' and the output bitstream is observed as '0100101'.

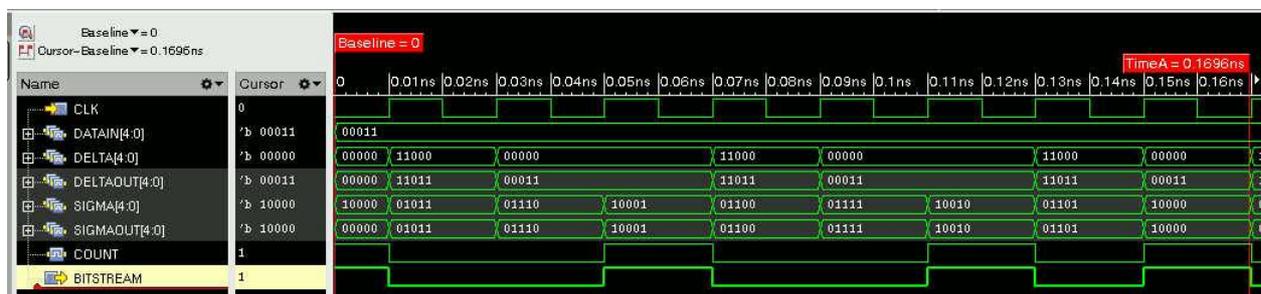


Fig.15 Output waveform of $\Delta\Sigma$ modulator for input '011'

The logic for $\Delta\Sigma$ Modulator is implemented and verified using Verilog modelling is implemented in SPICE level using LTspice tool. Fig.16 shows the testbench used for testing the functionality of the circuit designed in SPICE level. DIN<2:0> is the 3-bit input data. RESET is the signal used to initialize the content of shift register. CLK is the clock signal, LATCH is the signal used to latch out the stream bits at the output port BIT_STREAM after two clock cycles.

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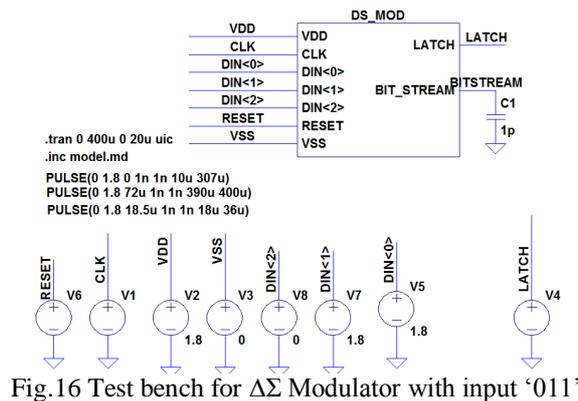


Fig.16 Test bench for $\Delta\Sigma$ Modulator with input '011'

Input data applied for the modulator DIN<0:2> is '011'. RESET is the input signal used to initialize the content of registers. LATCH is the signal to take out the bitstream from the modulator. Output bitstream '0100101' is observed in the output waveform and its matching with the desired bitstream.

Fig.17 shows the simulation result of $\Delta\Sigma$ Modulator for the testbench with input '011'. CLK is the clock signal used to operate the Σ register, RESET is the signal used for initialization of the content of Σ register, and bitstream is the output of the $\Delta\Sigma$ Modulator.

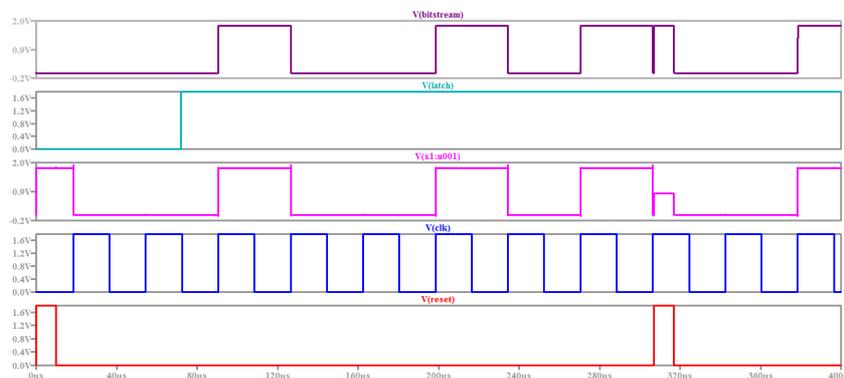


Fig.17 Output waveform of $\Delta\Sigma$ Modulator with input '011'

2. Δ Sequence Generator

Fig.18 shows the test bench for Δ sequence generator. DELTA0 and DELTA1 are the output pins. For input '1', output expected is '11'. For the input '0', the out expected is '00'. VDD and VSS are the power and ground pins respectively.

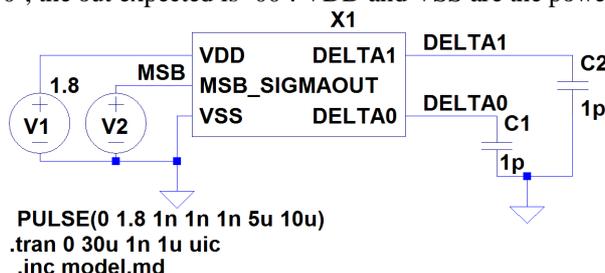


Fig.18 Testbench for Δ Sequence generator

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Fig.19 shows the simulation result of Δ Sequence generator. Input applied to MSB SIGMAOUT pin is logic high. Hence the output observed is '11'.

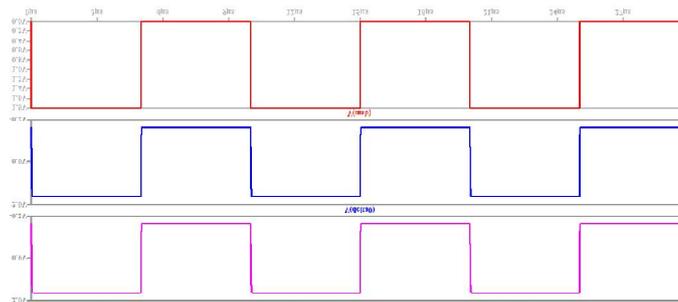


Fig.19 Simulation result of Δ Sequence generator

3. Analog Value Computation Block

Fig.20 shows the test bench for Analog value computation block which is the sub block of $\Delta\Sigma$ DAC block. Function of this block is to take the bitstream produced by the $\Delta\Sigma$ Modulator and charge the capacitor with a controlled current source. Voltage developed on its capacitor is the final output voltage of DAC.

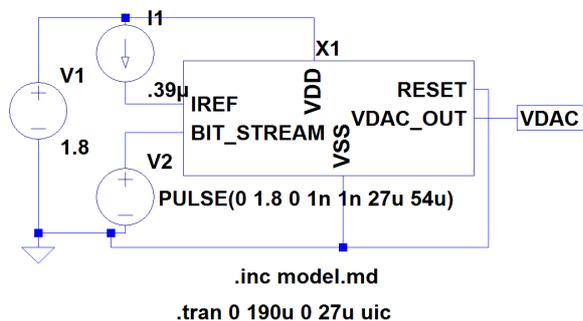


Fig.20 Testbench for Analog Value computation block

Fig.21 shows the simulation result of analog value computation block for the testbench with input bitstream '10101010'. Since there are four '1's in the bitstream, it is observed that the capacitor in the analog value computation block is charged four times with the differential voltage dv . Hence the final analog voltage built across the capacitor is 0.9v.

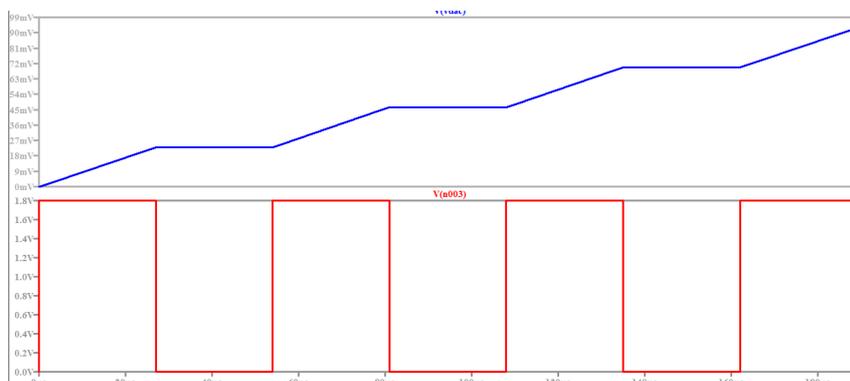


Fig.21 Simulation result of Analog Value Computation Block with bit stream '10101010'

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4. 3-bit $\Delta\Sigma$ DAC

Fig.22 shows the schematic diagram of 3-bit $\Delta\Sigma$ DAC which has two components namely $\Delta\Sigma$ modulator and the analog value computation block integrated together. The $\Delta\Sigma$ modulator produces the bitstream for the given set of digital input of 3-bits. The bitstream produced by the modulator is used by the analog value computation block to produce the stable analog output voltage VDAC.

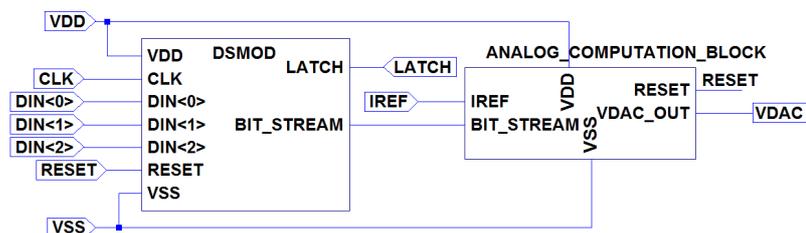


Fig.22 Schematic diagram of 3-bit $\Delta\Sigma$ DAC

Fig.23 shows the testbench used to test the functionality of the $\Delta\Sigma$ DAC. LATCH is the signal used to latch out the bitstream from the modulator after two clock pulses to estimate analog voltage by the analog value computation block. RESET is the signal used to initialize the content of register and the output capacitor of the analog computation block. CLK is the clock signal for register, IREF is the reference current used to charge the capacitor in the computation block as per the bitstream. Input bits applied for the DAC is '111' as shown in Fig.23.

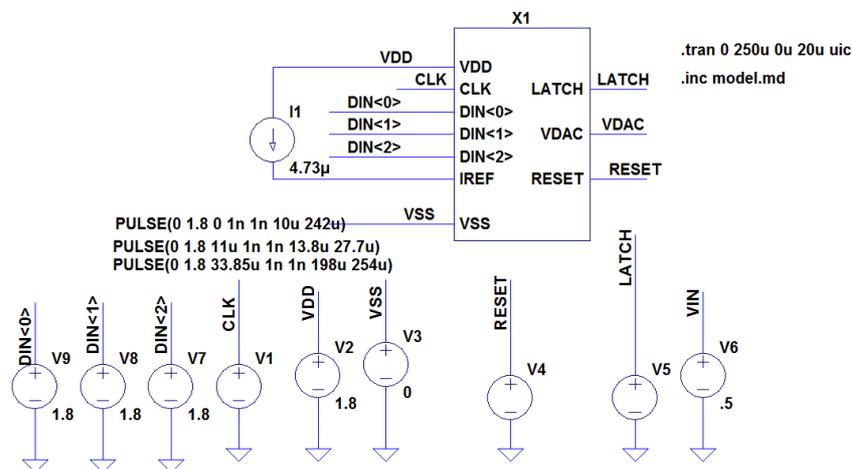


Fig.23 Test bench for $\Delta\Sigma$ DAC with input '111'

Fig.24 shows the simulation result of $\Delta\Sigma$ DAC for test bench with input data '111'. For $1LSB = 0.225V$, the theoretical output voltage expected is $1.575V$ from the equation $VDAC = 7(1LSB)$.

For the given input '111', bitstream with seven '1' is observed in the output waveform and the corresponding analog output voltage is observed as $1.5V$.

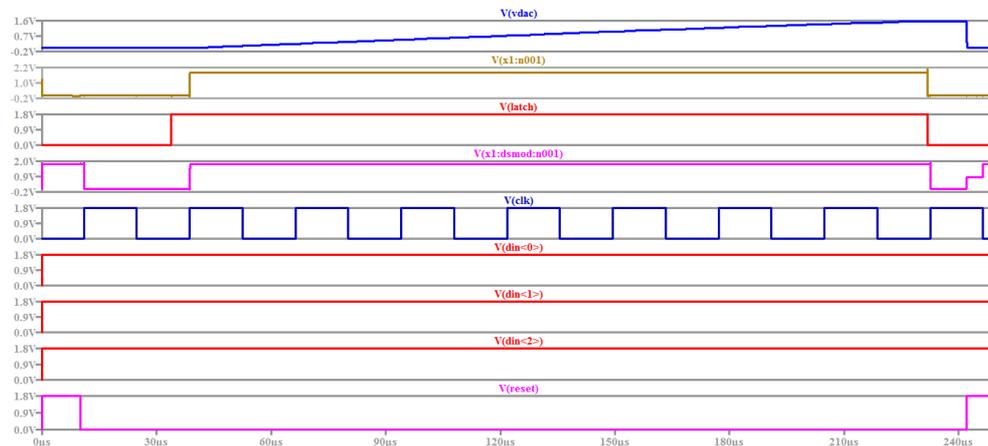


Fig.24 Output waveform of $\Delta\Sigma$ DAC with input '111'

V. CONCLUSION

Resolution is the one of the limiting factor associated with the SAR ADC architecture. This is because of the capacitive DAC employed in the SAR ADC. The DAC used in SAR ADC should have the same resolution as that of ADC. As the resolution of ADC increases, number of capacitors employed in DAC is also increase in direct proportion. This requirement for the increase capacitors in DAC leads to mismatch between the capacitors connected to each of the input bits of DAC and also, this will increase the power consumption of DAC.

In order to overcome this limitation associated with capacitive DAC, we have proposed and implemented a different DAC architecture referred as $\Delta\Sigma$ DAC. Functionality of the $\Delta\Sigma$ DAC is analysed by developing a Verilog model for 3-bit $\Delta\Sigma$ DAC and tested across the different input combination. 3-bit $\Delta\Sigma$ DAC is designed and implemented in SPICE level, tested for functionality and timing for different input conditions successfully and the results are documented. Evaluating the performance parameters of DAC, non-linearity parameters such as INL and DNL will be taken up as future work.

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