

Synthesis and Evaluation of Allocation Algorithms on FPGA Platforms

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ABSTRACT: Network on Chip has attracted lot of attention towards itself in recent years by giving good performance with less cost. Designing an FPGA requires good efforts to achieve high performance and its process of designing also varies based upon the requirements. Some of the FPGA designs require more attention towards area, some require high performance and some designs are to reduce the delay. An FPGA designer cannot randomly choose any arbitration algorithm, it is important to study the characteristics of some of the arbitration algorithm which will help the designers to choose suitable algorithm for their design. The project focuses on four algorithms and their characteristics on FPGA. The obtained results are tabulated for features like on-chip resources, timing parameter and FPGA resources.

KEYWORDS: Arbitration algorithm, FPGA, Network on Chip, resources.

I. INTRODUCTION

Network on Chip refers to a new networking method for on-Chip communication. The on-chip communication undergoes problems like latency. Routing technique used in a Network on Chip helps to achieve maximum performance so it is important to choose a best suitable scheduling algorithm. Arbiter present in a Network on Chip (NoC) determines the arbitration process. An arbiter decides when and which task needs attention based upon the priority assigned. In some cases when there is no priority assigned to the ports, then the arbiter works in a round robin fashion based upon its code. Network on Chips aim to provide efficient communication fabric with scalability. There are various topologies used for arrangement of the Network on Chip routers like mesh, linear, torrous and 2D, 3D type of topologies. The control path of on-chip communication routers are composed of arbiters and allocators while the data path of the on-chip routers consists of virtual channels, buffers and switching fabric.

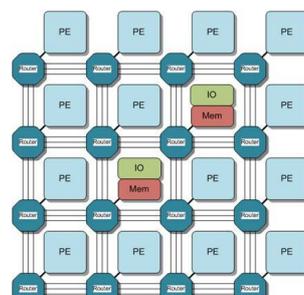


Figure 1: Block Diagram of NoC

The alignment of the paper is as follows. Section 1 describes the brief introduction of Network on Chip, arbiter and arbitration algorithm. Section 2 refers to some of the related work in arbiter and scheduling algorithm. Section 3 is about description of various algorithm and their principal of working. Section 4 describes about the synthesis and

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implementation of these allocation algorithms. Section 5 shows the experimental results obtained and the data is tabulated. Section 6 includes conclusion and finally references.

II. RELATED WORK

There are various scheduling algorithms in past which achieve high performance but also have disadvantages like deadlock and starving. The author [1] Zhongai lu has proposed a scheduling algorithm for large data to be transmitted. This algorithm is referred as Wormhole allocation algorithm where the large data is divided into smaller units called Flits and instead of transferring large data smaller packets of data called flits are transmitted which helps in faster transmission. The router in the network involved in flit ejection and flit transmission use acknowledgement process before transmission.

In [2] the author has introduced a scheduling algorithm called iSLIP which is a round robin based scheduling algorithm but is having an extra feature of giving priority. The arbitration algorithm is capable to reach highest of 100% throughput.

In [3] the author describes about themodeling communication between a pair of processors as tasks known as "Comtasks". The network is generated by "scheduling" these comtasks onto a set of routers so as to obtain a network with minimum area which fills up the available slack. Moreover, the set of overlapping comtasks are identified and generate a minimal network to allow the maximum set of overlapping comtasks to execute concurrently. The compared approach with a greedy network generation is obtained and the results show 80% benefit in the router area.

In [4] the author states that the system-on-chip (SoC) solutions based on state-of-the art FPGA have successfully demonstrated flexibility and reliability for scientific space applications like the Venus Express mission. Future high end payload applications (e.g. Solar Orbiter) demand high-performance on-board processing because of the discrepancy between extreme high data volume and low downlink channel capacity. Furthermore, in-flight reconfiguration ability enhances the system with re-programmable hardware and thus a maintenance potential. To achieve these advanced design goals a reconfigurable system-on-chip (RSoC) architecture is proposed supported by a flexible communication architecture. The flexibility for on-chip communication is covered by a dedicated network-on-chip (NoC) approach. The configurable system-on-chip solution is introduced and the advantages are outlined. A newly developed NoC approach is presented along with system-on-chip wire (SoCWire) and its performance and the applicability for in-flight reconfigurable systems is done.

• III. iSLIP Allocator

iSLIP is a separable allocation method that uses round-robin arbiters and updates the priority of each arbiter only when that arbiter generates a winning grant. iSLIP can be used either in a single pass, or as an iterative matching algorithm. By rotating the winning arbiters, iSLIP acts to stagger the priority of the input arbiters, resulting in fewer conflicts at the output stage. The update of a priority only occurs when an arbitration results in a grant and, as in a round-robin arbiter, priorities are updated so that a winning request has the lowest priority in the next round. The rotating priority aids the algorithm in assigning bandwidth equally and more fairly among requesting connections.

• Lonely Output Allocator

Single-pass separable allocators often give poor matching because many input arbiters choose the same popular output while the few requests for lonely outputs are less likely to be chosen by the input stage. The lonely output allocator, shown in figure 2, overcomes this problem by adding an additional stage before the input arbiters that counts the number of requests for each output. The input arbiters then give priority to requests for outputs that have low request counts the lonely outputs. This reduces the number of conflicts at the output stage, resulting in a better matching. As the request vector is taken by first stage the number of requests competing for the requested output is determined. The input arbiters are allowed to select 'o' request per sub-stage of first stage of the allocator with the priority given to lower numbered requests. Giving priority to low-count requests causes intermediate stage to present fewer conflicts for the output stage. The output stage then finally generates the final grant matrix.

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(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

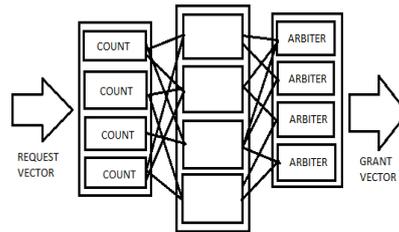


Figure 2: Block Diagram of Lonely Output Allocator

- **Wavefront Allocator**

The wavefront allocator, unlike the separable allocators arbitrates among requests for inputs and outputs simultaneously. The wavefront allocator cell is shown in figure 3 the wavefront allocator works by granting row and column tokens to a diagonal group of cells, in effect giving this group priority. A cell with a row (column) token that is unable to use the token passes the token to the right (down), wrapping around at the end of the array. These tokens propagate in a wavefront from the priority diagonal group, hence the name of the allocator. If a cell with a request receives both a row and a column token, either because it was part of the original priority group or because the tokens were passed around the array, it grants the request and stops the propagation of tokens. To improve fairness, the diagonal group receiving tokens is rotated each cycle. However, this only ensures fairness. In an $n \times n$ arbiter, diagonal group k contains cells x_{ij} such that $(i+j) \bmod n = k$. A non-square wavefront allocator can be realized, however, by adding dummy rows or columns to square off the array. The priority groups in an allocator need not be diagonals as long as they each contain one element of each row and column. When the cell is a member of the priority group, signal pri is asserted, which generates both a row token x_{pri} and a column token y_{pri} via a set of OR gates. If the cell is not a member of the priority group, row tokens are received via signal x_{in} and column tokens via y_{in} .

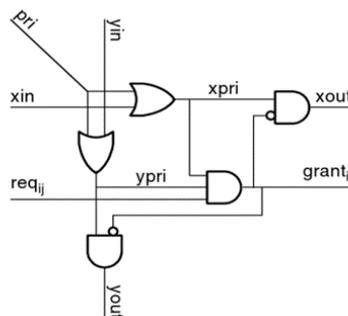


Figure 3: Wavefront Allocator cell

- **Wormhole Allocator**

Wormhole flow control, also called wormhole switching or wormhole routing is a system of simple flow control in computer networking based on known fixed links. It is a subset of flow control methods called Flit-Buffer Flow Control. Switching is a more appropriate term than routing, as "routing" defines the route or path taken to reach the destination. The wormhole technique does not dictate the route to the destination but decides when the packet moves forward from a router. Wormhole Allocation algorithm is a scheduling algorithm which is used to transfer large data packets faster and easily by breaking the data packets into smaller units. These smallest unit of data packet is known as FLITS. These flits are transmitted based upon the destination address, they can be divided into head flit, data and tail flit. The routers which transmit these flits uses an acknowledgement process before transmission. Transmission of data through Flits results in faster transmission and routers communicate each other before transmission of data. Figure 4 shows data packet being divided into smaller unit called Flit containing the head and tail flit and data to be delivered. Wormhole has virtual channels to transmit the data to the flit buffers.

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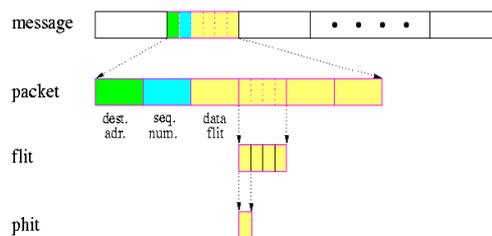


Figure 4: Data Encapsulation

IV. SYNTHESIS AND IMPLEMENTATION

The parameters considered are resource utilization, timing and average power dissipation. Resource utilization is considered in terms of on chip FPGA components used. Timing refers to the clock speed of the design and is limited by the setup time of the input and output registers, clock to the output time associated with the flip flops, propagation and routing delay associated with critical paths, skew between the launch and capture register. Timing analysis is carried out by providing appropriate timing constraints. The average power dissipation mainly composes of dynamic power dissipation besides negligible static power dissipation. In order to provide a fair comparison of the results obtained the test bench is provided with same clock period and same input statistics in all the topologies implemented. The constraints related to the period and offset are duly provided in order to ensure complete timing closure. The design synthesis, implementation and mapping have been carried out in Xilinx ISE 14.5. Power metrics are measured using Xpower analyser. The simulator data base is observed to obtain clock period and operating frequency of the implemented design.

V. EXPERIMENTAL RESULTS

Table 1: Comparison of Utilization of Resources

On-Chip Resources	iSLIP	Wavefront	Lonely Output	Wormhole
No. of Slice Regs	12	60	36	51
No. of Slice LUT's	12	36	51	36

Table 1 shows the comparison results of various scheduling algorithm based upon the resources utilized as the tabulated data indicates iSLIP scheduling algorithm uses less number of slice registers compared to others. If area is major concern about the design then then iSLIP is best suitable.

Table 2: Comparison of Timing of Various Allocation Algorithms

Timing Parameter	iSLIP	Wavefront	Lonely Output	Wormhole
Max Frequency (Mhz)	352.2	750.9	219.15	337.26

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Table 2 shows the timing parameters as listed above highest maximum frequency is 750.9 for Wavefront allocator. Global interconnect design problems in Network on Chip is delay. Delay directly depends on the performance so it is necessary to reduce delay and choose suitable allocation algorithm.

Table 3: Comparison in Power Dissipation between Allocation Algorithms

FPGA Resources	iSLIP	Wavefront	Lonely Output	Wormhole
Dynamic	6.63	37.25	6.63	5.64
Quiescent	3458.5	3460.17	3458.59	3460.14
Total	3465.2	3497.4	3465.22	3465.78

Table 3 shows tabulated results of scheduling algorithm for dynamic and quiescent power. Different types of energy requirements of a routing table are static and dynamic power. Static power also known as quiescent power depends on the required chip resources. Dynamic power is determined by the switching activity. Each of these powers for various scheduling algorithm is tabulated.

VI. CONCLUSION

The performance analysis of various scheduling algorithms is verified. The resulting structures showed differences in the way of using resources available in the target FPGA device. The Lonely allocation algorithm uses the resources extensively and has more power delay product and largest area delay product metric. On the other hand the iSlip based allocation algorithm uses lesser resources than any other algorithm considered and also shows relatively least power delay product and lesser area delay product metric. To sum up, a judicious trade-off between area, power and throughput parameters, and the intended application will determine the correct approach for implementing the allocation algorithms of an On-chip router. Since the area delay product and the power delay product of the design targeted for FPGA platforms are considered as important parameters. Hence implementation of above allocation algorithms for on-chip communication architectures, for FPGA based platforms revealed that iSlip based allocation algorithm as reasonably appropriate among the ones considered, for Network-on-chip (NoC) communication architectures.

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