

Design of Low Power and High CMRR Two Stage CMOS Operational Amplifier in 180nm Technology

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ABSTRACT: In this paper a CMOS two stage operational amplifier is presented which operates with 2.5 V power supply at 0.18 micron (i.e., 180 nm) technology, whose input is depending on Bias Current. To reduce overall power consumption of the system the supply voltage has been scaled down. The main aim is to decrease power dissipation. There is a trade-off among speed, power and gain at large supply voltages. Performance of any circuit depends upon speed, power and gain. Designed op-amp has very low standby power consumption with a large driving capability and operates at low voltage so that the circuit operates at low power. The two stage CMOS op-amp provides a gain of 52.80dB and a -3db bandwidth of 21.01kHz and a unity gain bandwidth of 9.20 MHz for a load considered of 3 pF compensation capacitor & 10pF load Capacitor. It has a PSRR (+) of 111.66dB, with a high CMRR of 117.10 dB and an output slew rate of 22.82 v/ μ s. The power consumption for the op-amp is 0.775mW.

KEYWORDS: CMOS, Two stage Op amp, CMRR, PSRR

I. INTRODUCTION

The trend towards low power low voltage silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications including telecommunications, medical, computers and consumer electronics. The operational amplifier is one of the most useful devices in analog electronic circuitry. Operational amplifiers are built with different complexity levels to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. Only with the presence of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, scientific devices, and industrial. Operational Amplifiers are the most widely used building blocks in analog electronic circuits more commonly known as Op-amps. They are linear devices which has nearly all the properties required for ideal DC amplification and is used extensively for signal conditioning, filtering and for performing mathematical operations such as integration, addition, differentiation, subtraction etc. Generally an Operational Amplifier is a 3 terminal device.

As shown in figure 1, the first block is of input differential amplifier, which is designed to provide very high input impedance, a large CMRR and PSRR, a low offset voltage, high gain and low noise. The second stage performs Level shifting, added gain and differential to a single-ended converter. The third block is the output buffer, which may sometimes be omitted to form a high output resistance. An Un-buffered op-amp is often referred to as Operational transconductance amplifier or an OTA. Those logics which have the final output buffer stage have a low output resistance (called as Voltage operational amplifiers).

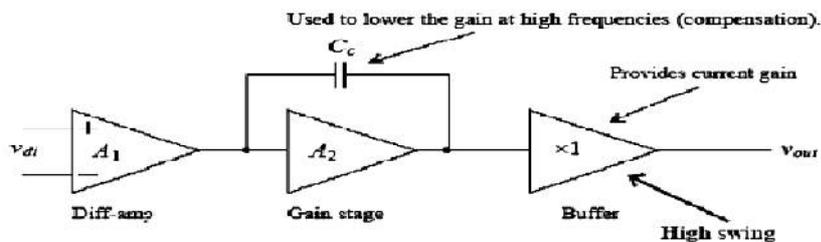


Fig. 1 Functional Block Diagram of two stage operational amplifier

II. RELATED WORK

CMOS Op-Amp is one of the most versatile and important building blocks in analog circuit design. Depending upon the value of their output resistance they are being classified into two categories:

a. Un-buffered Op-Amp:

These are Operational Transconductance Amplifiers (OTA), which have high output resistance as shown in figure 3 and Illustration of the design relationship and the circuit for a two stage OPAMP is as shown figure 4.

b. Buffered Op-Amp:

These are Voltage Operational Amplifiers, having low output resistance. These Operational amplifiers are controlled sources that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of the gain of the op-amp. One of the primary requirements of such an op-amp is to have an open-loop gain that is sufficiently large to implement negative feedback concept.

CMOS op-amps are similar in architecture to their bipolar counterparts.

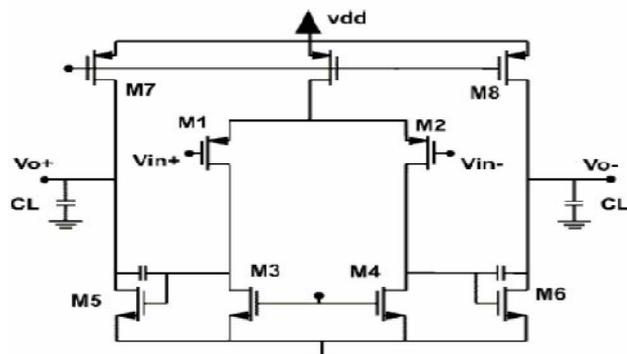


Fig 2 Two Stage Op-Amp

The Two Stage op-amp is shown in figure 2 which is widely used because of its simple structure and robustness.

The design process involves two major steps; the first is the conception of design. The conception of the design has been accomplished by proposing architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the intuitive view point necessary for choices that must be made. Second step is optimization of design, is to take the "first-cut" design and verify and optimize it. It is normally done by using Computer simulation and can include influences such as environmental or process variations.

Our aim is physical design of an Op-amp with low power. An ideal op-amp with a single-ended out is characterized by a differential input, zero output resistance, infinite input resistance and infinite voltage gain. In a real op-amp however these characteristics cannot be generated but their performance has to be efficiently good for the circuit behaviour to closely relate the characteristics of an ideal op-amp in most applications. With the introduction of

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each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths are scaling down.

III. DESIGNING OF TWO STAGE CMOS OPAMP

The designed op-amp has been simulated to find the different characteristics listed below. The total design is performed in available Cadence tool. Different test benches have been created to verify the design and extracted design along with the parasitic values has been simulated and compared with the schematic. Later we have also compared the obtained parameters of the device through simulation with the specifications for the device.

Design Issues

Typical specs	Design factors
DC Gain (A_v), ICMR, AND CMRR	Frequency Response
Power Dissipation	Load Capacitance
Slew Rate & PSRR	Compensation
Input Offset Voltage & Output Voltage Swing	Device Dimensions

Steps in designing a CMOS OP AMP:

- Creating the basic structure of the op amp.
- Decide a suitable configuration of the type of compensation needed for meeting the specification
- Selection of the dc currents
- Opting transistor sizes.

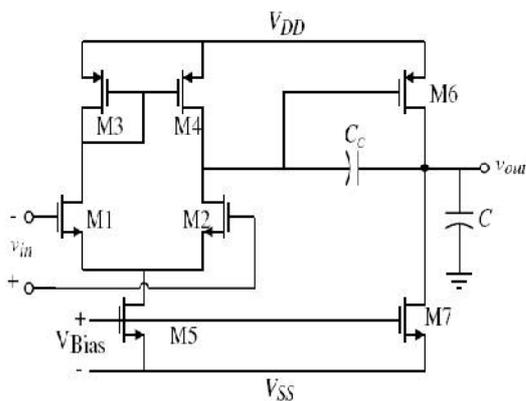


Fig.3 Unbuffered two stage CMOS OPAMP

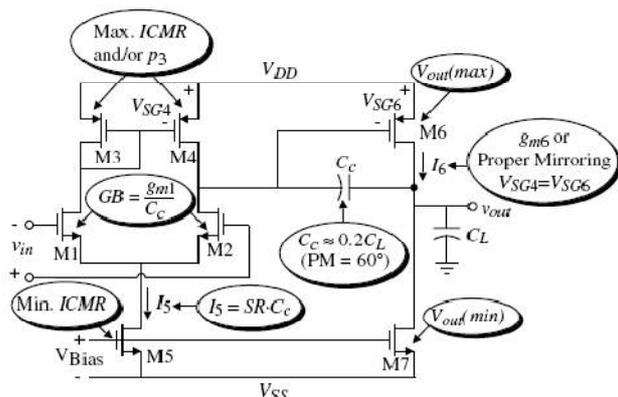


Fig. 4 Illustration of the design relationship and the circuit for a two stage OPAMP

This design procedure assumes that the unity gain bandwidth (GB), gain at dc (A_v), input common mode range ($V_{in(min)}$ and $V_{in(max)}$), slew rate (SR), load capacitance (C_L), settling time (T_s), power dissipation (P_{diss}) and output voltage swing ($V_{out(max)}$ and $V_{out(min)}$) are given. Choose the smallest device length so that the channel modulation parameter will be constant and give good matching for current mirrors.

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1. From the desired phase margin, choose the minimum value for Cc, i.e. for a 60° phase margin use the following relationship. This assumes that $z \gg 10GB$.

$$C_c \geq 0.22C_L \quad (1)$$

2. Determine the minimum value for the “tail current” (I_5) from

$$I_5 = SR \cdot C_c \quad (2)$$

3. The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ is

$$S_3 = (W/L)_3 = \frac{I_5}{(K'_3)[V_{DD} - V_{\square}(max) - [V_3(max) + V_{T1}(min)]]^2} \quad (3)$$

4. Requirements for the Trans conductance of the input transistors can be determined from knowledge of Cc and GB. The Trans conductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GB(C_c) \quad (4)$$

5. The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below:

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{(K'_1)(I_5)} \quad (5)$$

6. Using the negative ICMR equation, calculate the saturation voltage of M5 (V_{DS5}) by the following relationship:

$$V_{DS5} = V(min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(max) \quad (6)$$

7. With V_{DS5} determined $(W/L)_5$ can be calculated by the following equation:

$$S_5 = (W/L)_5 = \frac{2(I_5)}{K'_5(V_{DS5})^2} \quad (7)$$

At this stage the design of first stage op amp is complete.

8. Next the transconductance g_{m6} can be determined by the following relationship:

$$g_{m6} = 2.2(g_{m2})(C_L/C_c) \quad (8)$$

9. Then to design of M6 we can write $V_{SG4} = V_{SG6}$

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} \quad (9)$$

Knowing g_{m6} and S_6 will define the dc current I_6 using the following equation

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6} \quad (10)$$

10. Design S_7 to achieve the desired current ratios between I_5 and I_6

$$S_7 = S_5(I_6/I_5) \quad (11)$$

11. Check gain and power dissipation specifications

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)(\lambda_6 + \lambda_7)} \quad (12)$$

$$P_{diss} = (I_6 + I_5)(V_{DD} + |V_{SS}|) \quad (13)$$

Two stage OPAMP is designed for 180 nm technology for the following specifications:

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TABLE I DESIGN SPECIFICATIONS

Open loop Gain	100 V/V (40 dB)
Gain B/W at -3 db gain ,(f _{3db})	5 MHz
Load Capacitance (CL)	10 pf
Slew Rate	10 V/μs
Mirror Pole kept at	>=10GB
Maximum Power Dissipation	≤ 2mw
Channel Length	180nm
CMRR	≥ 60
PSRR	≥ 60
Power Supply	2.5V

IV .EXPERIMENTAL RESULTS

Schematic configuration of two stage OPAMP with 180nm technology is shown in figure 5 and aspect ratio's of 180 nm technology opamp their channel width for mos transistor are tabulated below.

TABLE II
CHANNEL WIDTH FOR MOS
TRANSISTORDESIGNED FOR 180 nm
TECHNOLOGY OPAMP

MOS Transistor	Aspect Ratio (W/L)
M1	3
M2	3
M3	15
M4	15
M5	4.5
M6	94
M7	14
M8	4.5

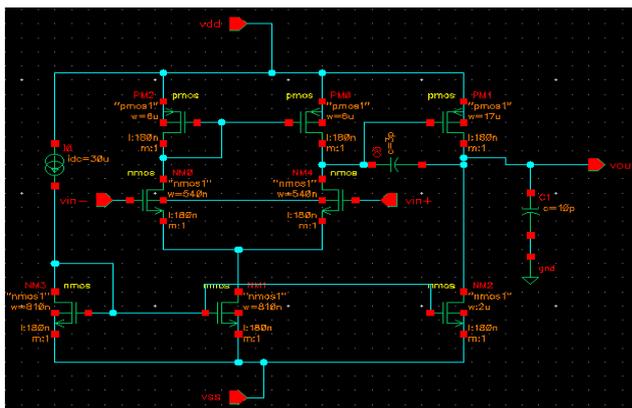


Fig. 5 Schematic configuration of two stage OPAMP

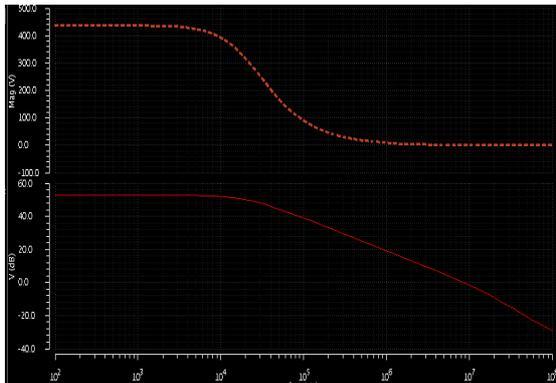


Fig.6 Frequency response simulation result

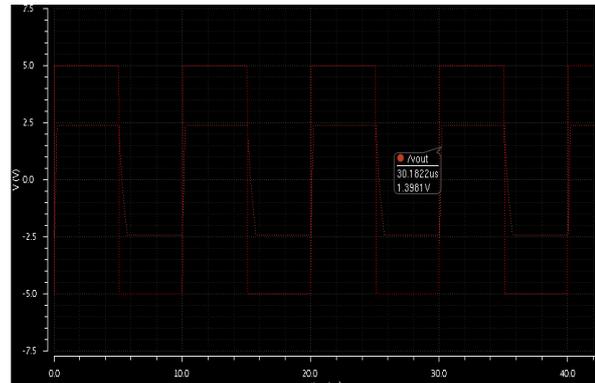


Fig 7 Slew rate simulation result

Frequency response and slew rate of 180 nm opamp technology simulation results are shown in figure 6 and figure 7.

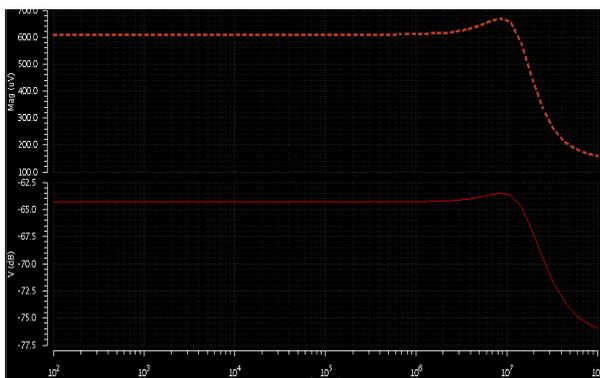


Fig 8 CMRR Simulation result

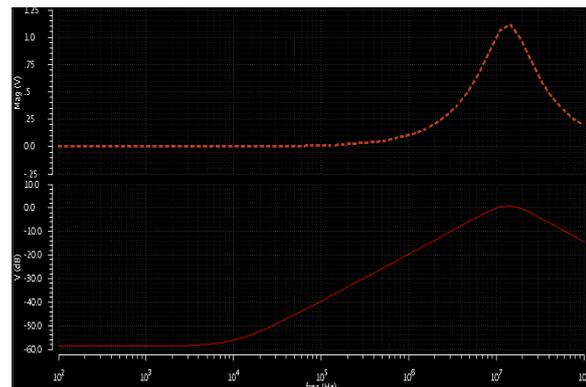


Fig.9 PSRR Simulation result

CMRR and PSRR of 180 nm opamp technology simulation results are shown in figure 8 and figure 9.

Slew rate (SR) = $V_2 - V_1 / T_2 - T_1$. From figure we can find the value is 22.82V/ μ S

The CMRR can be calculated as $CMRR = 20 \log_{10} \frac{A_d}{A_{cm}}$

From simulation CMRR can be calculated as, $20 \log_{10} \frac{436.83 V}{609.719 \mu V} = 117.103dB$

$PSRR = 20 \log_{10} \frac{A_d}{A_{ps}} = 20 \log_{10} \frac{436.83 V}{1.14 mV} = 111.66dB$

Power dissipation:

The power dissipation of designed Op-Amp is calculated as 0.775 mW using the SPECTRE simulator; have to set up a DC analysis. The power is calculated as the power dissipated by the V_{DD} source. To calculate the power in cadence, simulate the circuit and save the DC operating points and calculate the power as the product of the total current drawn from the V_{DD} DC voltage source and the total DC potential across the circuit. ($V_{DD} + |V_{SS}|$) Here we have taken the parameters as $V_{DD} = 2.5V$, $V_{PULSE} = 0$ to 2.5V, pulse width=5us, period = 10us. For the same W/L ratios as table II represents when V_{DD} is applied as 1.8V the power dissipation decreases to 0.441mW.

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TABLE III COMPARISON BETWEEN THEORITICAL AND SIMULATION RESULT

Specification	Actual value	Simulation value
open loop gain	40dB	52.80dB
Gain bandwidth	>5MHz	9.20MHz
Slew rate	>10 V/ μ S	22.82 V/ μ S
CMRR	>60dB	117.10dB
PSRR	>60dB	111.66dB
Power Dissipation	<2mW	0.775mW
Compensation capacitance	2.2pF	3pF

IV. CONCLUSION

The objective of this work was to implement the full custom design of low voltage and low power operational amplifier. In this paper a well-defined method for the design of a two-stage CMOS operational amplifier has been presented. The design has been made through the scaling of device parameters, as it is known that, by maintaining the scaling factor to a minimum value can reduce the current, power consumption and area as well. Now an OPAMP has been described in its negative feedback Configuration, as it can provide a moderate gain as compare to the open loop, but the problem is this case is the stability, which can be reduced by using the compensation techniques. In this thesis Miller Compensation technique is implemented, where this simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage.

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