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Low Transient to Exploit Same Tag Bits to Improve Error Protection in the Caches Using ETA

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ABSTRACT: Caches are most vulnerable to the transient errors. It is important to prevent transient errors and provide a correction mechanism for hardware circuits. To prevent transient errors, cache memories employ error protection mechanisms, such as parity codes and single-bit error correction and double-bit error detection codes. The existing schemes are not efficient in terms of error protection coverage. So another method is proposed to exploit same tag bits to improve error protection capability of the tag bits in the caches. When an error is detected in the tag bits, the same tag bit information is used to recover from the error. The proposed scheme has small area, energy, and efficient error protection. A new cache design technique, referred to as early tag access (ETA) cache is designed to improve the energy efficiency of data caches in embedded processors. Before the actual cache accesses it performs to determine the destination ways of memory instructions. It, thus, enables only the destination way to be accessed if a hit occurs during the ETA. Compared with the existing cache design techniques, the ETA cache is more effective in reduction of energy and maintaining better performance.

KEYWORDS: ETA(Early Tag Access) , Cache memory , Tag bits

I. INTRODUCTION

Due to the continued technology scaling to the nanometer regime, computer systems are becoming vulnerable to transient errors. With the trend of increasing transient error rate, it is becoming important to prevent transient errors and provide a correction mechanism for SRAM cache memories. Caches are the largest structures in microprocessors and vulnerable to the transient errors. Tag bits in cache memories are also exposed to transient errors and to reduce their vulnerability a few efforts have been made. Considerable efforts have been made to reduce vulnerability of data bits, but errors in tag bits are also critical for data integrity. For example, transient errors in tag bits can incur false misses in dirty cache lines, and consequently, stale data can be consumed. However, a complex protection mechanism for tag bits can degrade performance due to their long latency. Clearly, providing high reliability with a low-cost mechanism to tag bits is necessary to guarantee system integrity and maintain system performance. This paper presents a new technique, same tag bit similarity The same tag bits is used to improve error protection in the caches.

II. PROPOSED APPROACH

Most of the techniques consider only data bits without considering tag bits corruption. To improve tag bits reliability, it exploits tag bits similarity. Most of the tag bits in the data caches have their replica in adjacent cache sets due to spatial locality of programs. Hence, when an error is detected using the conventional parity check bits, the error can be corrected if the same tag bits were present in adjacent cache sets. Faulty tag bits are simply replaced with correct tag bits from the adjacent cache sets for error correction.

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A. DETAIL OPERATION

Detailed operation of the technique with an example. Four-bit STI is attached into each entry of tag array in a four-way set associative cache. When data (a) are fetched from the main memory, upper and lower sets are referred to find the same tag bits. In this example, the upper set has the same tag bits as newly fetched tag bits. After checking the lower and upper cache sets, STI bits of data (a) are filled with a proper STI code. At this time, STI bit of existing lines, whose tag value is the same with the new tag bits, is also filled with a proper STI code. STI codes of the upper right side set were originally 0000, no same tag, and thus corresponding tag bits were vulnerable to errors. After data (a) are loaded, however, the STI bits are encoded to 1001 due to the same tag bits in the lower left side set, and the corresponding tag bits are protected by exploiting the same tag bits. Therefore, both tag bits whose values are the same can be recovered from errors by fetching other intact tag bits. One more thing that have to be considered is to invalidate STI bits that are pointing evicted tag bits. The tag bits of the evicted cache line may have been pointed by STI bits of other lines in adjacent sets. If this situation is not handled appropriately, the STI bits will point to wrong tag bits. When this kind of STI bits is detected, they are invalidated and newly generated if possible.

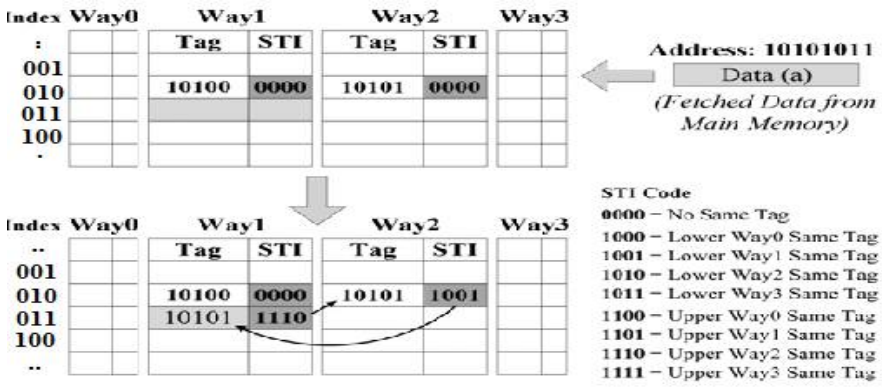

Fig (1) Detailed operation in a four way set associative cache

B. ARCHITECTURE

To implement SimTag, first, a shifter is added to access a lower or upper cache set. However, since this component may increase the critical path of cache access, we also devise an alternative counter-based technique. Second, STI Encoder is needed to generate STI bits. Third, STI replacement handler is required to modify STI bits in an upper or lower cache set on replacements. Finally, an error correction unit is built for error recovery.

i) SHIFTER*:* By changing the output signals of the cache decoder, cache lines in a lower or upper set can be accessed. Thus, our proposed architecture needs a shifter. On cache misses, the shifter shifts the output signals of the decoder to the left and to the right sequentially so as to generate STI bits. For error recovery, it also shifts the decoder output signals but shift direction is determined by the STI set location bit

ii) COUNTER: Fig.3 shows the alternative counter-based technique, which does not affect critical path. Similar to shifter, basic operation of the counter is increasing or decreasing a set index value on a cache miss. However, the difference is that it increases or decreases the set index value in the memory access stage. In case of a cache miss or occurrence of an error, the pregenerated set index value is selected by a multiplexer during the execution stage.

iii) STI ENCODER: To generate STI bits, the STI encoder compares the tag bits of cache missed data with other tag bits located in lower and upper sets while pipelines are stalled due to cache misses

iv) STI REPLACEMENT HANDLER*:* STI bits in a lower or upper set must be updated on cache replacements. The STI replacement handler checks all STI bits in the adjacent sets. If certain STI bits point to

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the tag bits of the replaced cache line, then we simply invalidate their STI valid bits and generate new STI bits by finding other same tag bits.

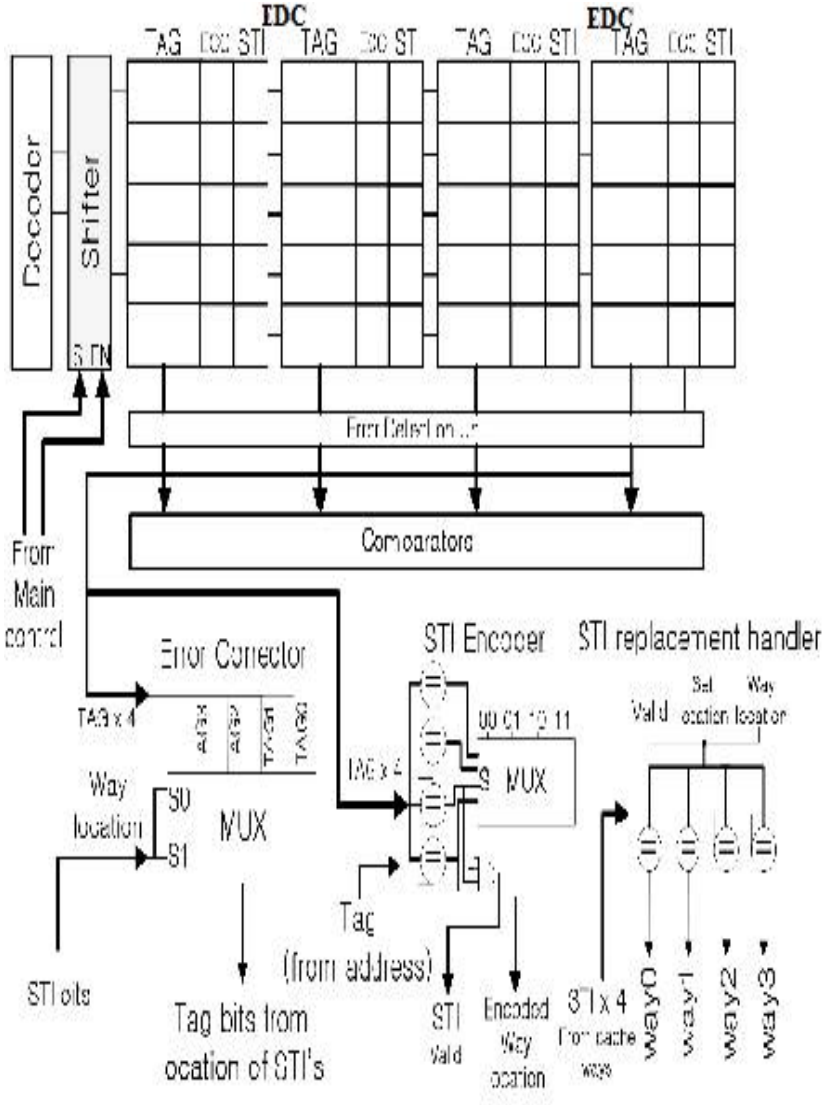

Fig (2) Detailed architecture

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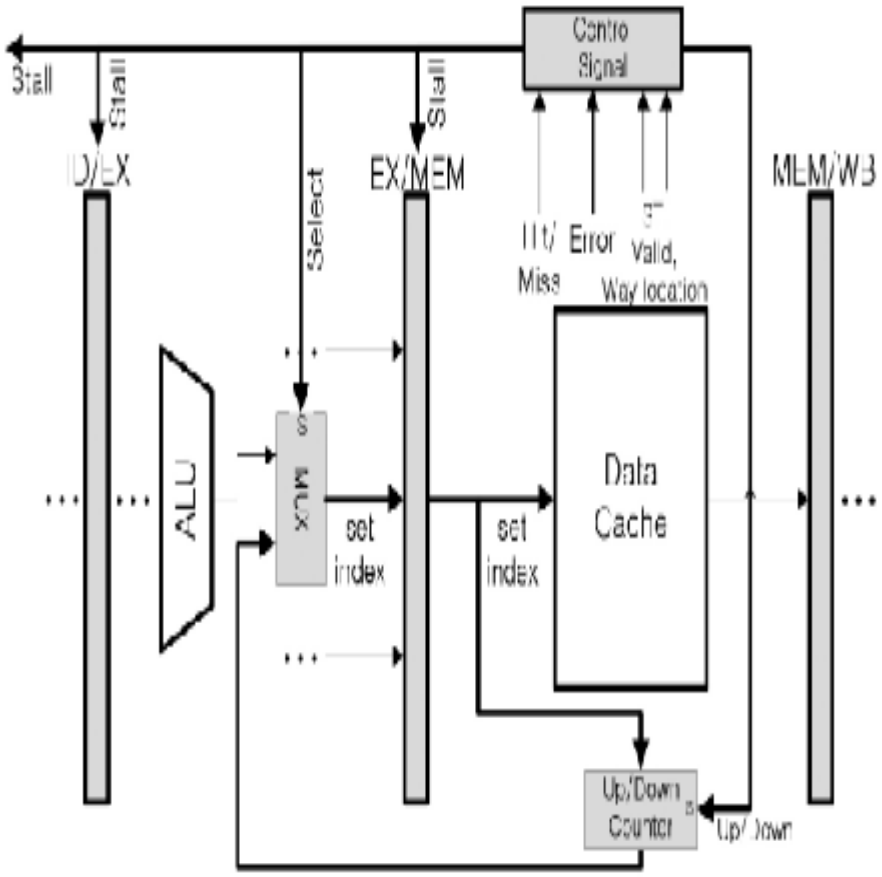

Fig (3) counter based technique

v) ERROR CORRECTOR: To recover tag bits from errors, uncorrupted tag bits should be obtained from an adjacent cache set using STI bits (if the same tag bits exist). With STI way location bits, the exact location having the same tag bits can be obtained. After fetching right tag bits, the corrupted tag bits are replaced with them.

vi) MAIN CONTROLLER: To support extra components, the main controller is slightly modified to generate necessary control signals. On cache misses or tag bits errors, the pipelines are stalled and, at the same time, the main controller signals the additional shifter (or counter) to access adjacent sets.

III. ETA ARCHITECTURE

All ways in the tag and data arrays are accessed simultaneously in a conventional set-associative cache. Under a cache hit the requested data, however, only resides in one way. The extra way accesses incur unnecessary energy consumption. In this section, cache architecture referred to as ETA cache will be developed. By reducing cache energy consumption the ETA cache reduces the number of unnecessary way accesses. To accommodate different energy and performance requirements in embedded processors, the ETA cache can be operated under two different modes: the basic mode and the advanced mode.

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(i) BASIC MODE:
In the basic mode of the ETA cache, each time a memory instruction is sent into the LSQ, an access to a new set of tag arrays and TLB .This new set of LSQ tag arrays and LSQ TLB are implemented as a copy of the tag arrays and TLB of the L1 data cache, respectively, to avoid the data contention with the L1 data cache. If there is a hit during the LSQ lookup operation, the matched way in the LSQ tag arrays will be used as the destination way of this instruction when it accesses the L1 data cache subsequently

(ii) ADVANCED MODE:
There are some memory instructions whose early destination ways cannot be determined due to either early tag misses or
early TLB misses when a memory instruction with either an early tag miss or an early TLB miss accesses the L1 data cache, the tag arrays of the L1 data cache are accessed first. In most cases this will be a real cache miss, and thus the L1
cache access is completed without the need to access the data arrays of the L1 data cache, thereby saving energy.

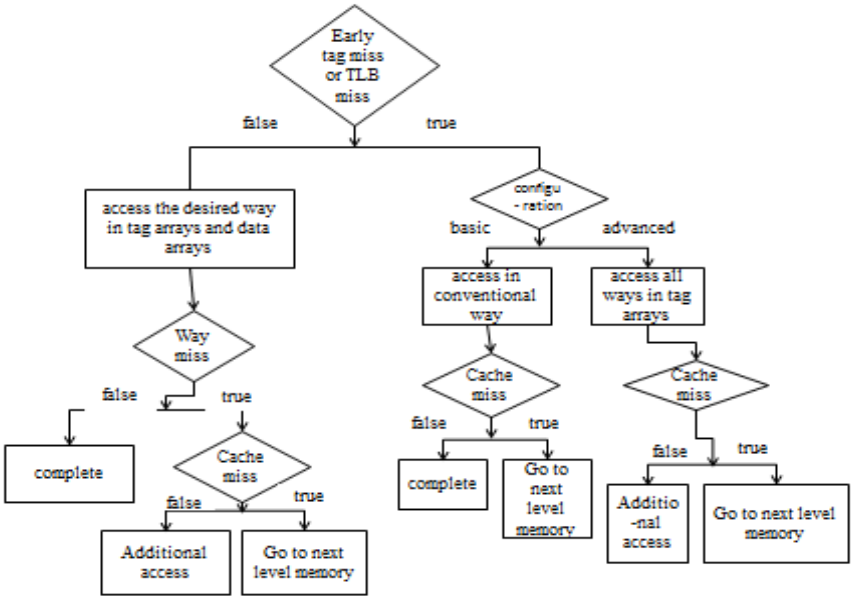

Fig (4) Operation flow of the proposed ETA cache under two modes.

IV. CONCLUSION

With the trend of increasing transient error rates, it is becoming important to provide error detection and correction. Traditionally, parity or SEC–DED code has been widely used for caches against transient errors. Many techniques are proposed to reduce performance, energy, and area overheads of the conventional error protection mechanism. To improve tag bits reliability, tag bits similarity is used. Most of the tag bits in the data caches have their replica in adjacent cache sets due to spatial locality of programs. Hence, when an error is detected using the conventional parity check bits, the error can be corrected if the same tag bits were present in adjacent cache sets. Faulty tag bits are simply replaced with correct tag bits from the adjacent cache sets for error correction. A new energyefficient cache design technique, ETA for low-power embedded processors. The proposed technique predicts the destination way of a memory instruction at the early LSQ stage. Thus, only one

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way needed to be accessed during the cache access stage if the prediction is correct, thereby reducing the energy consumption significantly.

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