

Design and Performance Comparison of High Speed Parallel BCD Multiplier

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ABSTRACT: Multiplication is the one of the most important and more power and time consuming operation in all the arithmetic and logical unit operations. Now-a-days decimal computations are needed in financial and banking and other applications with speed efficiency. Hence there is a demand to design multipliers with high speed by reducing the delay. This paper delivers the implementation of decimal multiplier which is arranged in parallel fashion. Multiplication process involves repeated additions. Two different adders are used in this methodology to decrease the delay. By using Reduced delay BCD adder rather than CLA adder there is a 16.27% reduction in delay. These modules are designed in Verilog HDL, simulated and synthesised using Xilinx 14.7.

KEYWORDS: Multiplication, Partial products (PP), BCD adder, delay, CLA adder, Recoding.

I. INTRODUCTION

Every user desires high speed operation for computing results. So many researchers are maximum focusing towards efforts in designing the digital circuits with the idea of reducing the delay. Multiplication is performed either in parallel or in sequential manner. This paper describes the delay comparison of parallel decimal multiplier by using CLA and Reduced delay BCD adders. This idea can be implemented by decrementing the number of partial products which leads to speed up the multiplication process. Multipliers are designed by using analog & digital circuits. In digital multipliers the two inputs are multiplied in similar manner as it is done in mathematics i.e., shifting of partial products followed by addition.

In Unsigned numbers, multiplication can be done by using AND gates and full adders. The partial products are generated by AND gates. Full adders are used for addition of generated partial products. For signed digit multiplication, the positive numbers are considered as usual but negative numbers are converted to 2's complement form. This gives all the partial products in positive. By using signed radix-10 method, the multiplier digits are recoded as -5 to 5 from 0 to 9 along with a sign bit. Most of the commercial databases use decimal format to store data rather than data in binary format. Representation of fractional decimal numbers in binary format will not be exact and hence, the approximate representations of fractional numbers are used in binary arithmetic operations.

II. LITERATURE SURVEY

There are several approaches for decimal multiplication. Decimal multiplication is considered as one of the most complicated operations, which requires high-cost hardware implementation. Therefore, the processor industry has opted to use sequential decimal multipliers to reduce the high cost of parallel architectures as given by Liu han et al. [1]. A fixed-point decimal multiplication is proposed that utilizes a simple recoding scheme to produce signed-magnitude representations of the operands thereby greatly simplifying the process of generating partial products for each multiplier digit. The fixed-point decimal multiplication utilizes decimal carrysave addition to reduce the critical path

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 6, Issue 4, April 2017

delay [2]. The carry look ahead adder permits the design of a parallel decimal arithmetic unit which is competitive to a binary arithmetic unit in terms of performance [3]. In [4], the delay is shown to be less in parallel multiplication rather than sequential method. Introduced and analysed are three different techniques for performing fast decimal addition on multiple binary coded decimal (BCD) operands by R.D Kenney [5] and the problem of Multioperand Parallel Decimal Addition with an approach that uses binary arithmetic and suggested adoption of binary-coded decimal (BCD) numbers by L.Dadda [6].

III. SYSTEM MODEL

The system model shows the block diagram for the efficient parallel decimal multiplication. Multiplication is done by using two adders to produce less delay. Decimal multiplication hardware requirement is mainly due to the reason that most of the commercial databases use decimal format to store data rather than data in binary format. Also all financial applications use decimal software in order to get the exact results. As a result decimal representation becomes hardware oriented. This model deals with simple calculation of partial products and their addition for the final product.

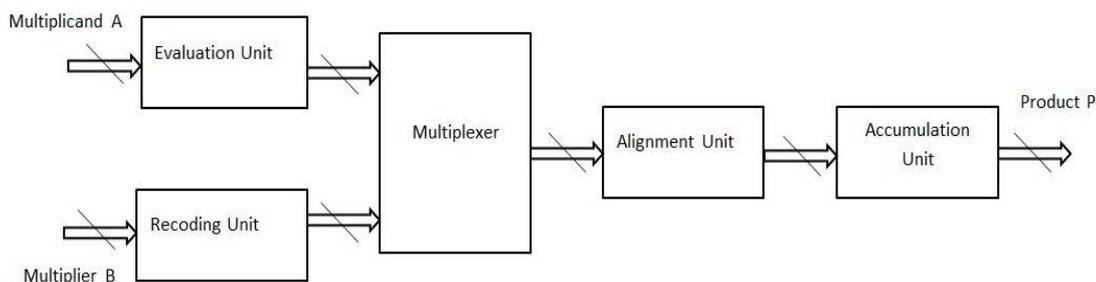


Fig 1: Block Diagram of Parallel Multiplier

A. Evaluation Unit

This unit calculates the multiplicand multiples as 1A, 2A, 3A, 4A and 5A for the input A. For computing the final multiplication product, the essential requirement is to calculate the multiplicand multiples. Inputs and outputs of these unit are in BCD form. BY using CLA adder and Reduced delay BCD adders these multiples are produced. Adder sections are used in both the Evaluation Unit and Accumulation Unit.

The Carry Look Ahead Adder (CLA) has less delay path than ripple carry adder. In CLA the post-correction utilization is eliminated but a pre-correction unit is required instead of post-correction stage. In pre-correction stage, both the inputs A and B are added up if the result is greater than or equal to eight an addition of 0110 is done for correcting the sum. If the result is 1110 or 1111 (invalid combinations), they are further represented as 8 and 9 respectively. The Reduced delay BCD Adder has three stages, viz., Pre Processing, Carry Look Ahead networking and Post Processing. Every adder has a Route delay and Logical delay. Route delay is the path delay from source to destination and logical delay is the time required for the entire operation. Route delay is minimum for Kogge stone adder so it produces less delay as compared to other adders.

B. Recoding Unit

The decimal digits {0 to 9} are recoded as {-5 to 5} by using the Multiplier Recoding Unit. The numbers -4 to -1 are recoded from 6 to 9. Every digit in BCD numbers is considered by 4-bits so this can be recoded as 6-bits by hot one encoding method. In 6-bits, MSB represents sign bit, and the other 5-bits represent the digit. If the BCD number is equal to or greater than five then the sign bit becomes negative otherwise it is positive. Another five digits at the output of the recoding unit are treated as selection bits.

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 6, Issue 4, April 2017

C. Multiplexer

It is a data selector which selects the multiplicand multiples {1A, 2A, 3A, 4A, 5A} by using the selection bits from recoding unit. It chooses the positive multiples if the sign bit is positive otherwise it selects negative multiples if the sign bit is negative.

D. Alignment and Accumulation Unit

The partial products are aligned accordingly which means the final result is obtained by left shifting and adding those partial products as same as in mathematics multiplication. Finally the result is obtained from Accumulation unit. If the input digit is of size n then the partial products length is of n+1 and the final product length may be maximum of 2n length.

IV. SIMULATION RESULTS

A 16-bit multiplier is designed using Verilog HDL and simulated using ISIM simulator. Figure 2 shows the simulated waveforms which are generated from Evaluation unit, intermediate partial products and the final result. It is designed in Verilog HDL, synthesized and implemented using Xilinx 14.7 design suite with specifications of spartan6(XC6SLX45-CSG324).



Figure 2: Simulation Results of 16X16-bit BCD Multiplication

In figure 2, A is 4 digit decimal value whose multiplicand multiples are calculated. M1, M2, M3, M4, M5 represents multiplicand multiples. A and B represents the multiplicand and multiplier respectively. P1, P2, P3, P4, PP1, PP2, PP3 and PP4 represents partial products and P represents final product. Table 1 and Table 2 represents the device utilization summary for CLA adder and Reduced delay BCD adder respectively.

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 6, Issue 4, April 2017

Table 1: Multiplication using CLA adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	75	54576	0%
Number of Slice LUTs	758	27288	2%
Number of fully used LUT-FF pairs	75	758	9%
Number of bonded IOBs	64	218	29%

The Device Utilization Summary allows us to quickly access design overview information, number of LUTs and Slice Register. Maximum Combinational path delay observed is 30.764ns for CLA adder.

Table 2: Multiplication using Reduced delay BCD adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	75	54576	0%
Number of Slice LUTs	729	27288	2%
Number of fully used LUT-FF pairs	75	729	10%
Number of bonded IOBs	324	218	148%

Maximum Combinational path delay observed is 25.744ns for Reduced delay BCD adder. Table 3 shows the Performance analysis of parallel decimal multiplier in terms of maximum combinational path delay and number of LUTs. By comparing the multiplication delays Reduced delay BCD adder has given the minimum path delay.

Table 3: Performance analysis of 16X16 bit multiplier

Parameters	CLA Adder	Reduced delay BCD adder
Maximum Combinational path delays(in ns)	30.746	25.744
Device Utilization summary(number of LUTs)	758	729

V. CONCLUSION

We have implemented the parallel decimal multiplication by two adders. The reduced delay BCD adder gives less delay as compared to CLA adder. The delay produced for CLA is 30.746ns and for reduced delay BCD adder is 25.744ns. Synthesis results show 16.27% reduction of maximum combinational path delay.

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ISSN(Online) : 2319-8753
ISSN (Print) : 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Website: www.ijirset.com

Vol. 6, Issue 4, April 2017

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