

# Performance Investigation of Asymmetrical Cascaded H-Bridge Multilevel Inverter Based DSTATCOM in Distribution Network

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**ABSTRACT:** This paper presents the performance analysis of asymmetrical cascaded H-bridge multilevel inverter based DSTATCOM in the distribution network. For this, seven level asymmetrical cascaded inverter based DSTATCOM is proposed for the compensation of 11 kV distribution network. The paper also presents the comparative analysis for different asymmetric inverters. For this, 7,9,11 and 13 levels with unequal dc voltage sources are realized. Level shifted based multicarrier alternate phase disposition (APOD) PWM control strategy is selected for the utilization of asymmetric cascaded H-bridge inverter. CHB multilevel inverters can be used for high power and medium voltage networks, it gives sufficiently less T.H.D. when compared with the conventional two level inverter. Asymmetrical inverters use decreased number of switching devices. Since distribution systems are believable to be subjected by power quality problems, so DSTATCOM is used in the network which mitigates the harmonics generated by nonlinear loads. The control algorithm for DSTATCOM for the production of reference compensating currents is based on the park's transformation (D-Q) theory. The results are achieved through simulation in MATLAB software.

**KEYWORDS:** DSTATCOM, asymmetric cascaded h bridge multilevel inverter (ACHBMLI), level shifted multicarrier sinusoidal pulse with modulation (LS-MSPWM), alternate phase opposition disposition (APOD), synchronous reference frame theory (SRF).

## I. INTRODUCTION

In present day's power quality improvement has become a major responsibility for the power quality engineers. The distribution network uses nonlinear reactive loads that are responsible for the birth of harmonics, instability of voltages which are the sources for poor power quality. The trendy load devices are also responsible for the negative effects of power quality. The power quality issues refer to the complications of voltage sag, swell, lagging power factor, high harmonic distortion contents, voltage flicker, load unbalancing etc. [1]. These all are responsible for the involution or complexities of the output waveforms. In order to meet the above problems, some preventive methods are proposed which are collectively known as custom power devices (N.G. Hingorani, 1995). This work mainly focusses on the performance of the three phase four – wire system with DSTATCOM. The device effectively compensates the load current harmonics that are given to the supply side. As, a result load gets compensated and the sinusoidal waveforms are achieved and compensation of reactive power is also achieved through DSTATCOM. It is a shunt connected device which improves the power quality of the system.

In the current years, multilevel inverters have attained much consideration because of its so many advantages of capability of reducing switching losses, voltage stresses very low harmonics [2]. The main benefit of using multilevel inverters is that higher number of voltages are achieved when the number of levels are increased. More the number of levels, lesser will be the harmonic distortions. Multilevel inverters are used in the high power and voltage applications [3]. Conventional two level voltage source converters are not effective to be used in low switching frequency applications while multilevel inverters can be used for the applications which use high or low switching frequencies. We achieve three levels of voltages or more in the form of staircase output by multilevel inverters whereas two level

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inverter produces two output voltages. We can get high power quality through multilevel inverters. There are three topologies for multilevel inverter. These are: Diode clamped, flying capacitor and cascaded h bridge multilevel inverter. Cascaded H-bridge inverters are considered to be the most profitable than other two topologies and are more widely used. CHB inverters use less number of switching components and are cost effective. They do not require clamping diodes and balancing capacitors. We get comparatively low harmonics and less losses and high efficiency. CHB multilevel inverters use separate dc sources and with these dc sources many inverters can be formed for producing higher number of voltage levels. CHB inverters are flexible and uncomplicated. There are two types of CHB MLI based on the dc sources which are Symmetrical CHB MLI which uses equal magnitude of dc voltage sources and another one is Asymmetrical CHB MLI that uses unequal magnitude of dc source voltages. Asymmetrical inverters are proven to be more advantageous than symmetric inverters. Asymmetrical inverters use less number of devices. We can achieve high number of levels by using less number of switching components and separate dc sources in asymmetric inverters. For the implementation of 7 level, we need only two h bridges in asymmetric inverters while three h bridges are needed to generate 7 levels in symmetric inverters. There is one main limitation of cascaded h bridge inverters that if we increase the number of levels, complexity of the device increases. This limitation is overcome by asymmetrical multilevel inverters with reduced number of switching components. Harmonic profile is better improved in asymmetric cascaded h bridge inverters.

This work mainly emphasizes on asymmetrical cascaded H-bridge multilevel inverters. The work in this paper is partitioned in different sections. Section-I presents brief introduction. Section-II represents the brief literature review of the related work. Section-III represents the analysis of different asymmetrical cascaded h bridge inverters in which 7,9,11 and 13 levels are realized and after that harmonic contents of each level are investigated and compared and also presents the results from this work. Section-IV describes DSTATCOM along with its control scheme. Section-V shows the work carried out for the performance of proposed 7 level asymmetric cascaded H-bridge inverter based DSATCOM for power quality improvement in the distribution network that reduces the output current harmonics and balance the load through simulation. The selection of asymmetrical cascaded H bridge inverter for DSTATCOM for the application of distribution networks successfully decreases the harmonics caused by nonlinear loads by increasing the number of levels. The results of the performance of DSTATCOM are justified through the simulation in MATLAB. Final conclusion of the work is presented in section-VI.

## II. RELATED WORK

The work already published in the literature is as follows:

The multilevel inverters are first defined by Nabae et al. [4]. Multilevel inverters start with three or more than 3 levels. Multilevel inverters have overcome the disadvantages of a 2-level inverter.

The term cascaded H-bridge was introduced by Marchesoni M. et al. [5]. In order to vanquish the limitations of other topologies of multilevel inverter, the researcher defined this new topology of multilevel inverter. The idea of cascaded H-bridge multilevel inverter was followed by the conception of connection of connection of series inverter by R.H. Baker et al. [6].

The realization of symmetrical 7-level and 15-level cascaded H-bridge multilevel inverters were first done by Zhong et al. [7].

Asymmetrical multilevel inverter was realized by FaridKhoucha et al. [8] in order to overcome the limitations of symmetrical multilevel inverters.

There are different methods in asymmetrical cascaded H-bridge multilevel inverter through which magnitudes of dc voltage are generated. These were proposed by JavadEbrahimi[9].

Multicarrier PWM strategy is also known as sub-harmonic PWM strategy. The term sub-harmonic was given by Guiseppe Carrara et al. [10] for conquering the limitations of a pulse generator. Sub-harmonic method effectively reduces the total harmonic contents.

Three phase 7-level asymmetrical CHB MLI is analysed in the paper [11] by varying modulation index in order to achieve minimum harmonic content.

Reduced switch topology of 13-level asymmetrical multilevel inverter is proposed in paper [12]. The topology used 10 switches with unequal voltage magnitudes.

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The term custom power device was given by N.G. Hingorani [13] for the improvement of power quality. Custom power devices are used in the distribution network. There are different types of custom power devices [14]; UPQC, DVR and DSTATCOM.

For calculation of reference source currents of DSTATCOM, there are three methods [15]. These are synchronous reference frame, instantaneous reactive power and adaline control theory.

5-level cascaded H-bridge multilevel inverter is used as a DSTATCOM for reducing harmonic content in the distribution network [16].

IEEE-519 1992 standards give guidelines for the control over harmonics in the power system. [17].

### III. ASYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded H-bridge inverter having unequal values of dc source voltages are said to be asymmetrical inverters. These use different algorithms of calculating the magnitudes of dc source voltages. In this work binary method of selecting magnitudes for dc source voltages are used for realizing 7 level and 11 level. In the case of 9 level and 13 level, two voltages of h bridge are taken as identical while the other bridge is having unequal magnitude of dc voltage. In binary based 7 level inverter, two h bridges of unequal dc source voltages are used with eight switches while in the case of 11 level, three h bridges are used with 12 switches. For implementation of 9 and 13 levels, three h bridges are used having two voltages similar and third one different with 12 switches.

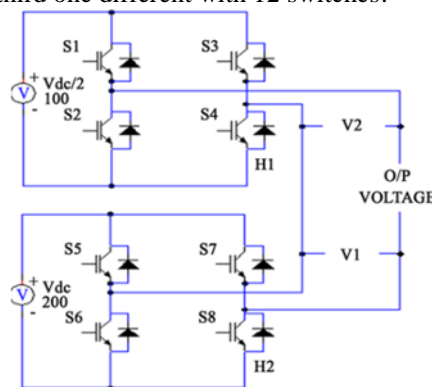


Figure 1: Binary based asymmetrical CHB MLI

In the binary method, the ratio of separate dc sources is 1:2:4:8... Binary means a component of two. This method of selecting values of source voltages is based on the geometric progression by a component of 2. Very sufficient number of components are used even for higher level also in this method thus offering compatible results. It overtures suppleness to the multilevel inverter. Figure 1 shows an example of binary based asymmetrical inverter having two unequal dc source voltages. With the two h bridges it will generate 7 levels of output voltages with four switches in each H-bridge and if add extra h bridge it will generate 11 levels by using the 10 carriers in the logic circuit of PWM.

The output voltage is the summation of all the h bridges voltage;

$$V_0 = V_1 + V_2 \quad (1)$$

The magnitude of SDCSs in binary method is evaluated according to the equation written below:

$$V_i = 2^{(i-1)} V_{dc} \quad (2)$$

Where  $i=1, 2, \dots, N$ ; N is the number of H-bridges.

In the other method of arranging the dc voltages, the number of h bridges are taken as three in both the levels. The arrangement is such that voltage of first h bridge and third h bridge unit are kept identical and second h bridge voltage is taken unequal. For realizing nine levels, magnitude of dc sources are taken as 100, 200 and 100 volts respectively for all the h bridges. The magnitude of dc voltages for the three bridges are 100, 400 and 100 volts respectively. Figure 2 shows the h-bridge inverter having three bridges of single phase inverter. The dc voltage sources are connected with the h-bridges which are in series in a single phase.

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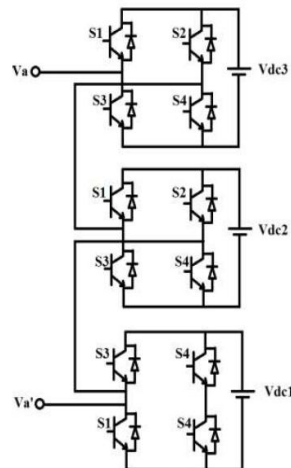


Figure 2: Asymmetrical arrangement of three h bridge

Here  $V_{dc1}$  and  $V_{dc3}$  having equal magnitude of voltages while  $V_{dc2}$  is having unequal dc source voltage with 12 switching devices and twelve feedback diodes. The output voltage of this inverter is the sum total of all voltages of all H-bridges;

$$V_0 = V_{dc1} + V_{dc2} + V_{dc3} \quad (3)$$

The magnitude of selecting SDCS's can be penned according to the following equation:

$$V_1 = V_{i+2} \neq V_{i+1} \quad ; i = 1(4)$$

Table 1. Component requirement in different arrangements of dc sources of asymmetrical inverter

Type of dc source arrangement	Output phase voltage	DC sources	Switches	Main diodes	$V_0(\max)$	Line to line voltages	Ratio of dc sources
Binary	$2^{(N+1)} - 1$	N	4N	4N	$2^N - 1$	2m-1	1:2:4...
Two equal with one unequal dc voltage	m	N	4N	4N	$\frac{m-1}{2}$	2m-1	1:2:1...

In the above table, 'm' is the number of levels of voltages and 'N' is the number of h-bridges. The table shows the number of switching components, number of bridge cells along with main diodes required in the different methods of dc voltage magnitude. The table also shows the number of phase to phase voltages and phase to ground voltages in each method. Number of dc voltage sources depend upon the number of h-bridge cells.

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## A. CONTROL STRATEGY FOR ACHBMLI

The control strategy of asymmetric multilevel inverters refers to the different pulse width modulation methods used for generating the switching pulses for synthesizing the ac staircase waveforms. The desired ac output is all controlled by these techniques. The switches of the converter are made to set in the motion by these methods. The ON and OFF states of the switch combinations of the inverter are controlled by the logic circuit of these strategies. The main objective of the control strategy is to remove nonessential signals. There are various control strategies. In this work, for generating the different ac output voltages for every level, multicarrier based level shifted Alternate Phase Opposition disposition strategy is used.

Multicarrier sinusoidal PWM uses more than one triangular carriers. These strategies are widely used as these are simple in structure, it gives less harmonic contents by eliminating the unwanted signals in comparison to the other techniques of PWM. The main advantage of this strategy is that it is suitable for the use in high power applications. A comparison of reference signal with carrier signal is done. If sinusoidal signal comes to be greater than carrier signal, pulses will be spawned in the upward cycle that is the carriers will be produced in the positive half. If reference signal comes to be lesser than the sinusoidal signal, pulses will be triggered in the lowermost cycle and carriers will be arranged in the negative half.  $\frac{m-1}{2}$  Carriers are set off in the upper half of the cycle and remaining  $\frac{m-1}{2}$  carrier waves are triggered in the lower half.

Level shifted alternate phase opposition disposition is the popular technique of multicarrier PWM in which (m-1) carriers are inclined such that each carrier is 180° out of phase to its adjoining carriers. The technique is based on the identical switching frequency. After the comparison of sinusoidal signal with the carrier waves, the gate signals are produced. Reference frequency is 50 Hz and carrier frequency is taken to be 5 kHz for each level. The modulation index which is the ratio of amplitude of reference signal ( $A_m$ ) to the carrier signal ( $A_c$ ) is calculated for each level according to the equation given below:

$$m_a = \frac{2A_m}{A_c} \quad (5)$$

Frequency ratio is the ratio of carrier frequency ( $f_c$ ) to the reference frequency ( $f_m$ ) and is calculated using the below formula:

$$m_f = \frac{f_c}{f_m} \quad (6)$$

Frequency ratio for each level is coming to be 100 Hz.

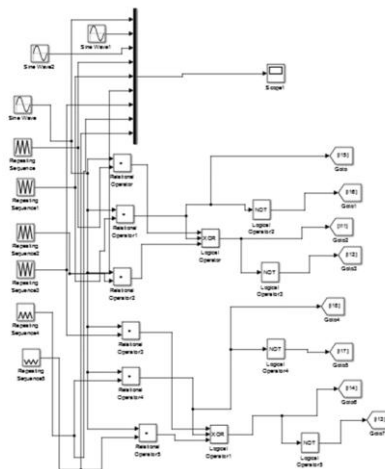


Figure 3: Logic circuit of APOD for 7 level asymmetric cascaded h bridge inverter

The switching or gate pulses which we achieve are generated by the logic circuit of APOD PWM strategy. Figure 3 shows the logic control circuit of APOD for 7 level asymmetric cascaded h bridge inverter. Here six carriers are employed having 8 switches. From these six carriers, first three carriers demonstrate positive switches of two h bridges

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and rest three carriers are revealing for the negative switches of the two h-bridges. The first three carriers are mingled with one XOR gate and the next three carriers are submerged with another XOR gates. This creates seven levels in the output voltages for particular one phase. Different pulses are gathered with these two XOR gates for the development of accurate signals. So, similar agenda follow for other levels also. The only difference occurs in the number of carriers and switches used. NOT gate is personifying the revert mode for the complementary switches. Relational operator is used for comparison between sine signal and carrier signal. (m-1) relational operators are used for m levels.

## IV. DSTATCOM

DSTATCOM is a shunt connected custom power device connected in the distribution network to resituate current harmonics presented by nonlinear loads. DSTATCOM improves the voltage figure. It upgrades the power quality. Since nonlinear loads cause drowns the whole entire system of the distribution system. DSTATCOM improves the power factor of the load and balances the load. It protects the source side from the harmonics that are provided by load side. DSTATCOM deeds like a shunt active filter that balances the load. DSTATCOM effectively resolves the problems in the distribution networks. It also reduces voltage distortion problems. It relocates active and reactive power with the distribution network. DSTATCOM is connected between the source and load side known as point of common coupling known as point of common coupling.

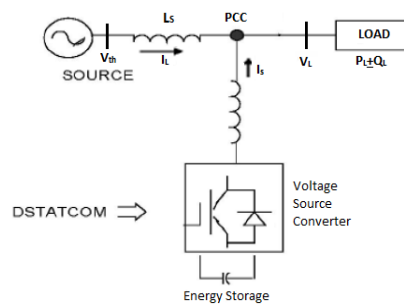


Figure 4: Basic configuration of DSTATCOM

Figure 7 shows the DSTATCOM in the distribution system. It consists of a voltage source converter, energy storage unit which provides the dc voltages to the inverter. PCC is the point of common coupling through which DSTATCOM is connected between source and load. The configuration also consists coupling inductor.

## B. SYNCHRONOUS REFERENCE FRAME THEORY

SRF theory also known as d-q theory based on the conversion of currents in synchronously rotating d-q frame. D-Q theory refers to the conversion of three axis into two axis. The purpose of this theory is to obtain the reference currents for the DSTATCOM. The three phase voltage signals are developed by the phase locked loop (PLL). The load currents and these voltages are considered to be the inputs which are first fed to the controller. PLL provides the sine and cosine signals. The load currents are converted to  $\alpha$  and  $\beta$  frame from stationary (a-b-c-) frame. This transformation is known as Clark's transformation. The transformation in MATRIX form is shown below. PLL provides the angle to the Clark's transformation and Park's transformation.

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (7)$$

Using Park's transformation this two axis  $\alpha - \beta$  frame is now transformed into rotating d-q frame. Equation of Park's transformation is as follows:

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$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta & 0 \\ -\sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (8)$$

Where  $\theta$  is the transformation angle given by:

$$\theta = \tan^{-1} \frac{\alpha}{\beta} \quad (9)$$

These currents converted into the Park's transformation are filtered after the occurrence of fault. The reference source currents are generated which are converted back to a-b-c frame which is known as inverse Park's transformation.

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & -\sin \theta & \frac{1}{\sqrt{2}} \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & \frac{1}{\sqrt{2}} \\ \cos(\theta - \frac{4\pi}{3}) & -\sin(\theta - \frac{4\pi}{3}) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \quad (10)$$

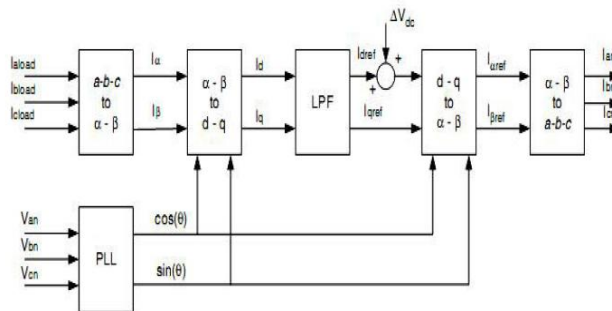


Figure 5: Block Diagram of SRF method

These currents are sent to the PWM signals of the converter for generating the switching pulses to produce the required current. The PWM in this case is used as level shifted carrier based APOD technique. PI controller is used to maintain the dc voltage constant. The injected current is the difference between the reference current and source current. The reference source currents obtained here are the filter currents obtained from the above procedure. The dc quantities are disparate after filtering into a-b-c quantities. This theorem is valid only to the three phase systems. The main function of the PLL is to exercise the voltage signals and to provide transformation angle to the  $\alpha - \beta$  to d-q conversion block. The block diagram of the control scheme used for DSTATCOM for the estimation of reference currents is shown below.

## V.RESULTS

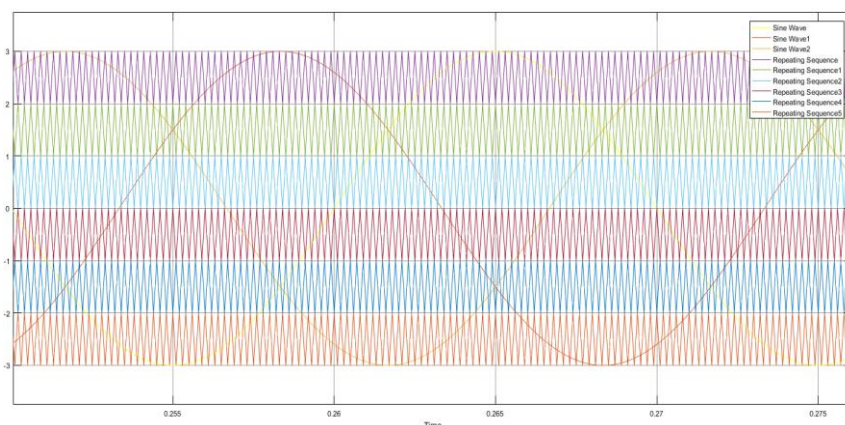


Figure 6: Reference and carrier waveforms for 7-level asymmetrical multilevel inverter

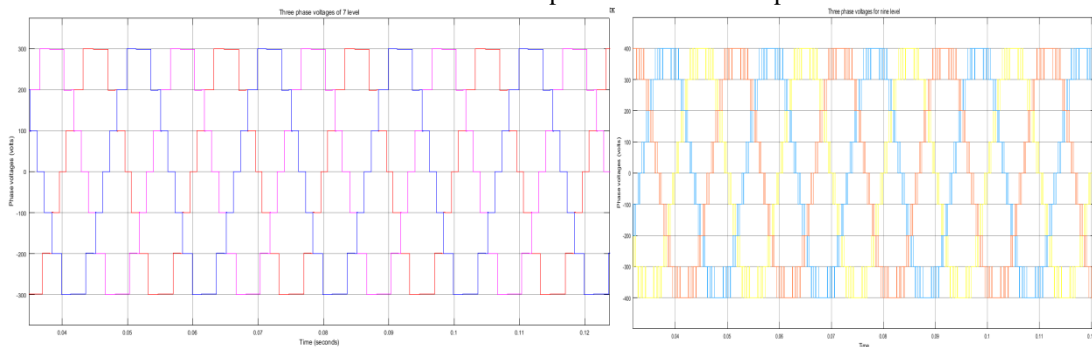
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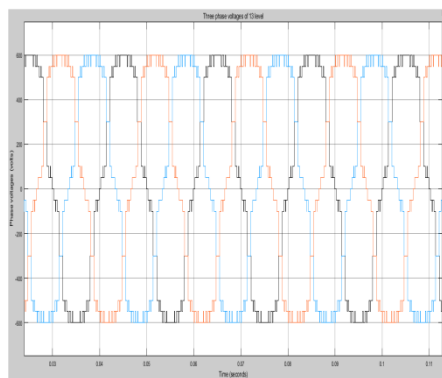
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The above figure shows 6 carriers for seven level multilevel inverter. There are three sine waves for each phase. The sine waves also known as reference signals. These signals are compared with the carrier signals for generating the positive group as well negative group in the arrangement. For generating the reference-carrier arrangement for 7-level, three carriers for all the three positive levels and rest three for the negative levels. In the same fashion, we achieve the arrangement for the other three levels also. Y-axis is the amplitude and X-axis represents time.

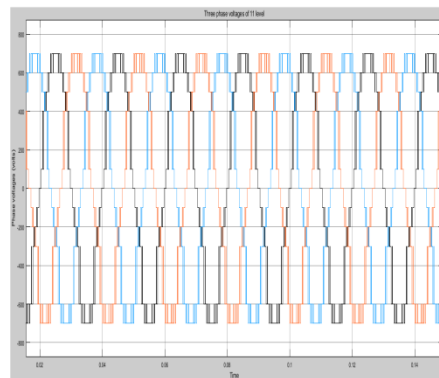


(a) 7 level

(b) 9 level



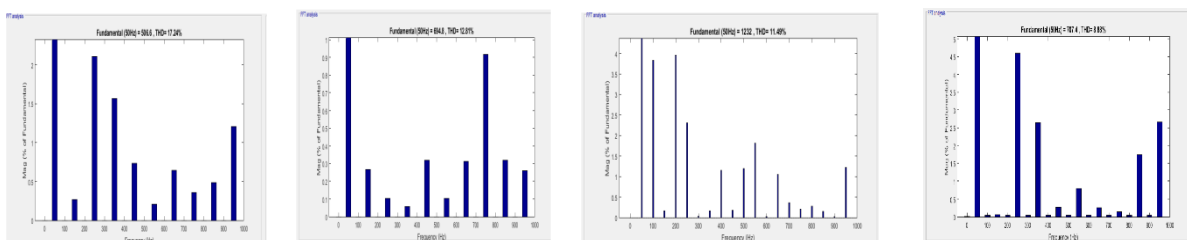
(c) 11level



(d) 13 level

Figure 7: Three phase output voltage waveforms of asymmetrical cascaded inverter (a) Seven level (b) Nine level (c) Eleven level (d) Thirteen level

The above figure shows the waveforms for 7, 9, 11 and 13 levels of asymmetrical inverter. For 7 levels, 3 positive voltage levels are generated in the upper half while 3 in the lower half. In 9 level asymmetrical cascaded H-bridge inverter, four positive voltage levels are generated during upper half cycle and negative voltage levels are in the lower half. For getting 11 levels of asymmetrical inverter, five levels are achieved during upper half cycle and rest five levels are for negative voltages. For generating 13 levels, there 6 positive levels of voltage and 6 for negative voltage levels. As the number of voltage levels increase, waveforms occupy near sinusoidal shape.



(a) 7 level

(b) 9 level

(c) 11 level

(d) 13 level

Figure 8: THD analysis (a) 7 level (b) 9 level (c) 11 level (d) 13 level



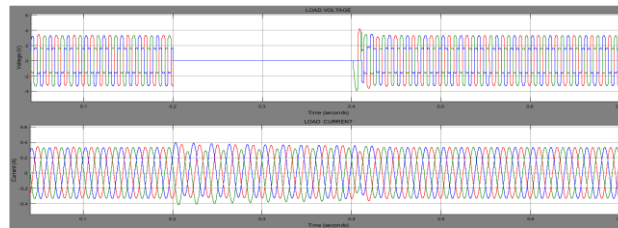
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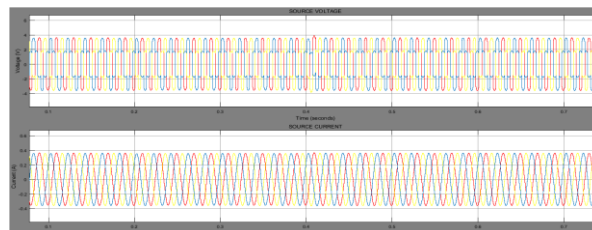
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This can be seen from the above figure showing reduced harmonic contents as the number of levels get increased. THD from 7-level inverter comes to be 17.24%. 12.81% harmonic content is achieved through 9-level inverter. Using 11-level, 11.49% THD is coming and with 13-level asymmetrical inverter, 11.49% harmonic content is reduced to 8.88%. Balanced waveforms are achieved when the number of levels are increased.



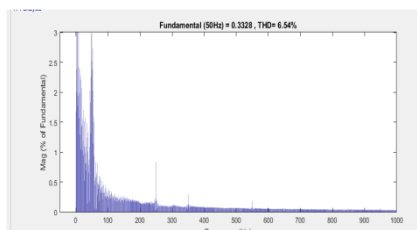
(a) Load Voltage and Load Current



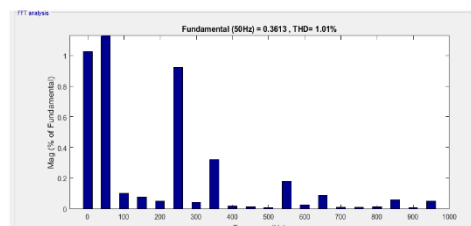
(b) Source Voltage and Source Current

Figure 9: Waveform analysis for source voltage, source current, load voltage and load current

A three phase to ground fault is created between the duration of 0.2, 0.3 and 0.4 seconds. During this, load voltage gets short circuited and load currents suddenly increases which results in the load unbalancing as shown in figure 9 (a). In figure 9 (b) we can see that DSTATCOM effectively compensates the harmonics of the load current which are eliminated in the source side resulting in balanced supply. We can observe the unbalanced voltage and current waveforms in the load side which are compensated through DSTATCOM in source side.



(a) LOAD CURRENT



(b) SOURCE CURRENT

Figure 10: FFT analysis of load current and source current

Due to the effect of non-linearity in the distribution system, total harmonic distortion comes to be 6.54% in the load current but DSTATCOM has compensated the harmonic content to 1.01%. DSTATCOM mitigates the effect of non-linearity to the source side. The reduced THD has a great impact on the power quality improvement as the current and voltage waveforms are balanced that are supplied to the consumers.

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## VI. CONCLUSION

In this paper, performance of DSTATCOM in 11 kV distribution system with asymmetrical cascaded h bridge multilevel inverter is evaluated in the distribution network. It is found that DSTATCOM effectively compensates the harmonics presented due to the non-linear loads. It has compensated the harmonics from 6.54% to 1.01% which is below than 5% according to IEEE-519 standards. It has reduced the unbalancing of the load. Binary based 7 level asymmetrical multilevel inverter using APOD technique is implemented in DSTATCOM. For this, seven level is first realized in MATLAB/SIMULINK model. A comparative analysis between 7,9,11 and 13 levels of asymmetrical cascaded h bridge inverters is done using different algorithms for dc source arrangement is made. It is observed that as the number of levels increases, T.H.D. reduces and waveform becomes smooth and near to the sinusoidal. It can be concluded that with multilevel inverters, performance of DSTATCOM becomes effective for improving the power quality in the distribution networks.

## REFERENCES

- [1] H. Mehta, "Custom power: an opportunity for energy conversion", IEEE International conference on electricity Distribution, pp. 5.23/1-5.23/6, 1993.
- [2] I.D. Pkarne, Y.N. Bhosale, "A review on multilevel converter topology", International conference on power energy and control, pp. 700-703, 2013.
- [3] R Anjali Krishna, "A brief review on multilevel inverter topologies", IEEE Conference on Power and computing technologies (ICCPCT), pp.1-6, 2016.
- [4] A. Nabae and H. Akagi, "A new neutral point clamped PWM inverter", IEEE Transactions on Industrial Electronics, Vol.17, pp. 518-523, 1981.
- [5] M. Marchesoni, M. Mazzucchelli and S. Tenconi, "A non conventional power converter for the stabilization of plasma", IEEE Transactions on Industrial Electronics, Vol. 5, No. 2, DOI: 10.1109/63.53158, pp.212-219, 1990.
- [6] R.H. Baker and L.H. Banister, "Electric Power Converter". U.S. Patent, 1975.
- [7] Zhong Du, Leon M. Tolbert, Joh N. Chiasson and BurakOzpineci, "A cascaded multilevel inverter using a single DC source", Applied Power Electronics Conference and Exposition, APEC, 21<sup>st</sup> Annual IEEE, pp. 426-430, 2006.
- [8] FaridKhoucha and MounaSoumiaLagaun, "A comparison of symmetrical and asymmetrical three phase H-bridge multilevel inverter for DTC induction motor drives", IEEE Transactions on Energy Conversion, DOI: 10.1109/TEC.2010.2077296, pp. 64-72, 2010.
- [9] JavadEbrahimi, "A novel switching technique for three phase asymmetrical multilevel inverter", IEEE first conference, pp.1-1, 2010.
- [10] GuiseppeCarrara, S.Gardella M. Marchesoni and R.Salutari, "A theoretical analysis of a new multilevel inverter based PWM methods", IEEE Transactions on Power Electronics, Vol. 7, No. 3, pp. 497-505, 1992.
- [11] NeerajSeth, VanyaGoel, and R.D. Kulkarni, "Performance analysis of 7-level three phase asymmetrical multilevel inverter at various modulation indices", IEEE Conference on Power Electronics, Drives and Energy Systems, PP. 1-6, 2016.
- [12] EmadSamadaei, AbdalrezaSheikholeslami and JafarAdabi, "A square T-Type module for asymmetrical multilevel inverters", IEEE Transactions on Power Electronics, Vol. 99, No. 1, 2017.
- [13] N.G. Hingorani, "Introducing Custom Power Devices", IEEE publications, Vol. 32, No. 6, pp. 41-48, 1995.
- [14] M.L. Crow, "Power Quality enhancement using custom power devices"
- [15] Bhim Singh and Jitendra Solanki, "A comparison of control algorithms for DSTATCOM", IEEE Transactions on Industrial Electronics, Vol. 56, No. 7, pp. 2738-2745, 2009.
- [16] AkulaRajasekhar and Mamidi Naveen, "Mitigation of flicker sources and power quality improvement by using cascaded H-bridge multilevel inverter based DSTATCOM", IEEE International Conference on Electrical, Electronics and Optimization Techniques, pp. 3125-3128, 2016.
- [17] IEEE- 519-1992 Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems", IEEE Standards, pp. 1-112, 1993.