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ECG Signal Processing by a Convolutional Neural Network with a Processing Element

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ABSTRACT: Cardiovascular diseases (CVDs) are the leading cause of death today. The current identification method of the diseases is by analysing the Electrocardiogram (ECG), which is medical monitoring technology recording cardiac activity. Unfortunately, looking for experts to analyze a large amount of ECG data consumes too many resources. Therefore, the method of identifying ECG characteristics based on machine learning has gradually become prevalent. Using a convolutional neural network (CNN), quick and accurate species identification is a way to ensure the modularity and scalability of the efficient processing element (PE) units, activation function modules, and circuits designed. The TSMC 0.18 μm CMOS technology was used to implement the planned CNN, and it had a 60 MHz operating frequency and 1.42mm² chip area, and maximum power dissipation of 4.4 mW. Furthermore, six types of ECG signals drawn from the MIT-BIH arrhythmia database were used for performance evaluation. Results produced by the proposed hardware showed that the discrimination rate was 96.3% with high efficiency in the calculation,

KEYWORDS: Convolution neural network(CNN), Processing Element(PE)

I. INTRODUCTION

In the top 10 global causes of mortality, heart disease has risen to the top spot. An early warning system for cardiac illness could be required to successfully minimize mortality from sudden cardiac death. Artificial intelligence-based medical electronic equipment technology, including wearable devices, has been extensively and continually investigated and improved in recent years concerning the noninvasive diagnostically valuable tools for detecting patients at high risk of sudden cardiac death. Since electrocardiography (ECG) examination delivers electrophysiological signals released from the heart muscle, it has been regarded throughout many elements of such applications as a mature and well-established monitoring approach. The ECG signals may be used to identify several aberrant heartbeats, for instance.

Earlier research has demonstrated in the literature that ECG can be lethal arrhythmias like ventricular tachycardia and ventricular defibrillation, among others, have been accurately detected by noninvasive algorithms developed by some researchers using system-on-chip (SoC) platforms. Other researchers have focused on circuit-design-based studies aiming at the detection of abnormal ECG signals. A cardiac sensor SoC (CS-SoC) with machine learning support was created for mobile health care applications. According to the findings of this study, the CS-SoC managed to identify arrhythmias based on an ECG in real-time with an accuracy of 95.8% while using just 48.6 W of power.

The SoC essentially comprises three modules: a high-pass sigma-delta modulator-based biosignal processor, a switch key control transceiver, and a digital signal processor. In, a low-power biological signal collection and classification system for human sensor networks is described. Also constructed in FPGA is another illustration of a wearable cardiac arrhythmia early detection device as suggested by. The MIT-BIH ECG arrhythmia database's numerical detection results demonstrate that the suggested method may reach a sensitivity and specificity of 94.64% and 99.41%, respectively. Additionally, a premature ventricular complex (PVC) detecting device based on convolution neural networks (CNN) is suggested.

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The CNN, which consists of two convolutional layers and one fully connected layer, enables quick training, successfully establishing the identification model. This research aims the creation of a CNN-based real-time ECG signal identification circuit to produce an efficient and accurate abnormal heartbeat classification/detection due to the growing interest in medical wearable monitoring devices nowadays. In general, the suggested circuit classifies six various types of ECG heartbeats, including the typical one, using three convolution layers and two fully linked layers. It should be emphasized that for network training and testing, the MIT-BIH arrhythmia database is used in this case. To obtain a compact area and high-speed design that may be highly compatible with worn ECG electrodes and is therefore particularly appropriate for portable and wearable devices, the suggested CNN chip was constructed in a TSMC 0.18 μm complementary metaloxide-semiconductor (CMOS) process. It should be mentioned as well that motion artifact is a significant difficulty for wearable ECG monitoring. In this regard, several earlier research in the literature has shown that deep learning models, such as CNN, are effective in removing motion artifacts. Therefore, we think that the suggested CNN chip may be further used for the job of ECG heartbeat detection for wearable medical devices with certain suitable arrangements. As a consequence, the application-specific integrated circuit (ASIC), with a chip size of 1.4 mm^2 , wastes power by 4.4 mW at the operating frequency of 60 MHz. The CNN algorithm's general structure and the specifics of the suggested circuit's architectural design are presented in this paper's following sections:

II. METHODOLOGY

2.1 Proposed Method

In general, a typical ECG signal consists of five characteristic points, denoted as P, Q, R, S, and T, respectively. Different diseases manifest themselves by components formed by a variety of combinations of these characteristic points, such as the QRS complex, PR interval, ST segment, and so on. In addition, the variability of interbeat intervals (i.e., RR intervals), alternatively known as the heart rate variability, can be diagnostically useful for serving as a predictor of mortality after myocardial infarction. When an abnormality is detected at an early stage, patients can be treated on a timely basis. The database used in this research was drawn from the MIT-BIH Arrhythmia Database. It contains 48 two-channel ambulatory ECG recordings obtained from 47 subjects studied by the BIH Arrhythmia Laboratory between 1975 and 1979, and each recording is 30- min long. The recordings were sampled by 360 Hz with 11-bit resolution over a 10mV range. For each ECG recording, the database also includes computer-readable reference annotations for each beat, thus being very suitable for applications in the task of ECG classification. Our study aims to design and realize a CNN-based abnormal heartbeat detection ASIC, and the chip is capable of identifying six different types of ECG signals drawn from the MIT-BIH arrhythmia database: normal, left bundle branch block (LBBB), right bundle branch block (RBBB), premature ventricular contraction (PVC), atrial premature beat (APB), and paced beat, as tabulated in Table 2.1.1.

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Table 2.1.1. Listing of different types of ECG heartbeats drawn from the MIT-BIH arrhythmia database to be detected.

Layer	Name	Number of Parameters
1	Convolution ($3 \times 1 \times 7$)	21
2	MaxPooling ($3 \times 1 \times 2$)	0
3	Convolution ($1 \times 1 \times 1$)	3
4	Convolution ($3 \times 1 \times 7$)	21
5	MaxPooling ($3 \times 1 \times 3$)	0
6	Flatten	0
7	Fully Connected (6×21)	126
8	Fully Connected (21×6)	126
	Total	297

Figure 2.1.1 provides a schematic block diagram illustrating the entire flow of the proposed CNN algorithm for ECG heartbeat classification. To reduce the circuit area, here we only included two convolutional layers to perform the main calculations and inserted an extra convolutional layer between both layers in the design of the CNN architecture, as shown in Figure 2.1.1.

Since the kernel size of the extra convolutional layer is 1×1 , this design would result in a significant reduction in the number of parameters, meaning the implementation of the circuit becomes much simpler while the overall training accuracy would still maintain at an adequately high level.

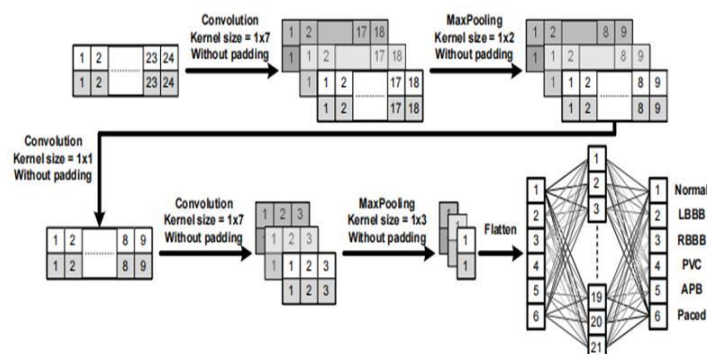


Figure 2.1.2 The schematic block diagram of the entire flow of the proposed CNN algorithm for ECG signal.

To have a better idea about how the proposed CNN algorithm works, we here just take the third convolution layer as an example to illustrate how the convolution calculation performs and explain why it would produce three 2×3 blocks after the convolution. First, it should be noted that there are three 1×7 kernel filters at this layer. In addition, note that the input is a 2D array of size 2×9 .

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The convolution is performed as follows. We slide each 1×7 kernel filter column-wise first and then advance along the rows over the input. Since each input row consists of only 9 data points and the filter length is 7, without zero padding, it would result in a 2D output of size 2×3 after the filtering process.

As a result, because there are three 1×7 kernel filters, it would finally produce three 2×3 blocks as outputs after the convolution calculation at this layer is completed.

Moreover, to achieve re-usability in circuit design, we further analyzed all the calculations required by the convolutional layers as well as the fully connected (FC) layer and then determined the total number of filter coefficients for the entire network structure. As a result, the total number of filter coefficients or parameters required for each layer of the proposed CNN structure are as listed in Table 2.1.2. Note that here in Table 2.1.2 “ $3 \times 1 \times 7$ ” in the first convolution layer means that there are three kernel filters of size 1×7 in this layer.

Table 2.1.2 Several parameters in each layer

Layer	Name	Number of Parameters
1	Normal Beat	N
2	Left Bundle Branch Block Beat	(LBBB) L
3	Right Bundle Branch Block Beat	(RBBB) R
4	Premature Ventricular Contraction	(PVC) V
5	Atrial Premature Beat	(APB) A

2.2 Proposed Architecture

As described in the previous subsection, when an ECG signal is input into the neural network, two-dimensional convolution calculations of three 1×7 filters in the first layer are performed and then followed by the 1×2 max pooling process. Note that a max pooling operation simply reduces the feature dimension by replacing the corresponding local patch in the convolutional layer of the same stage with its maximum value. Next, a 1×1 filtering process in the second layer is then performed. Afterward, similar to the first layer, in the third layer, the convolution calculations of three 1×7 filters are performed and then followed by a 1×3 max pooling. Finally, the learned feature maps are flattened and then fed into a fully connected neural network with an input layer of 21 nodes and an output layer of 6 nodes (i.e., six types of different ECG heartbeats) obtained after the SoftMax calculation. Figure 2.1.2 shows the schematic diagram of the proposed CNN algorithm. It should be noted that the main problem in implementing neural networks is that the detection accuracy, number of neurons, and the circuit area affect one another. For example, to enhance the detection accuracy, the number of neurons is unavoidably bound to increase, and thus, the original circuit area would undesirably increase. Therefore, the proposed research aims to design and implement a very large-scale integration (VLSI) circuit of the proposed CNN algorithm which can be used for ECG heartbeat classification.

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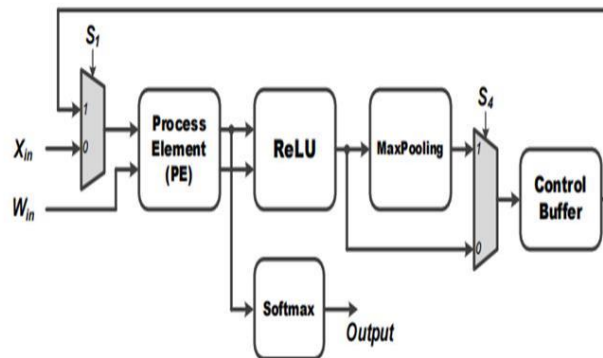


Figure 2.2.1 The architecture of the main CNN core

To substantially reduce the circuit area, here a modular design is adopted. Figure 2.1.2 shows the overall hardware architecture of the proposed main CNN core. It executes all the operations such as multiplication, addition, activation function, maximum pooling, and SoftMax calculations, as required by Figure 2.1.1. As depicted in Figure 2.1.2, the proposed CNN circuit mainly consists of process element (PE), ReLU, SoftMax, MaxPooling, and Control Buffer modules. The PE module is essentially used for all multiplication-accumulation (MAC) operations. The activation function employs ReLU and SoftMax modules. In addition, after each layer of CNN, the max pooling layer is generally applied. Finally, temporary storage space is designed for storing the intermediate values produced by each layer. Consequently, under a constraint of a small area, the modules mentioned above are all designed to be repeatedly used so that the circuit may effectively and efficiently achieve utilization maximization and the chip area may be thus substantially reduced. The details in these five modules are discussed as follows.

Process Element (PE) :

The PE module is employed for all the multiplication and addition (MAC) operations of the proposed CNN circuit. As shown in Figure 3.2.2, the proposed PE module executes the CNN filter size of 1×7 and 1×1 , and the fully connected layer operation of 6 to 21 and 21 to 6. It should be noted that the proposed PE module includes seven multipliers and six adders and thus, a complete fully connected operation would include three executions of the PE module for finishing doing the 21 MAC operations. Moreover, W , where $W = [W_0, W_1, W_2, W_3, W_4, W_5, W_6]^T$, can be either a set of filter coefficients or a set of weights; W is a set of filter coefficients when the PE performs the convolution calculations while it is a set of weights when the PE performs the MAC calculations at the fully connected layer.

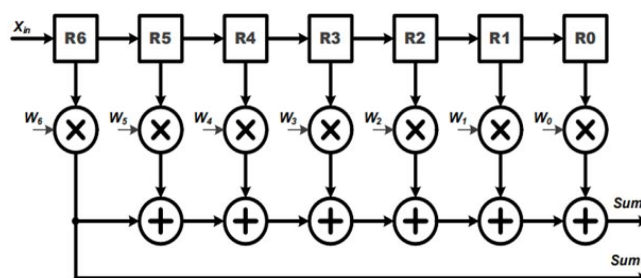


Figure 2.2.2. The architecture of the proposed PE module

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ReLU:

The activation function of ReLU outputs the positive number after the CNN operations. As shown in Figure 2.2.3 the proposed ReLU module uses the S2 signal to select the results from 1×7 or 1×1 CNN operations and send them into the ReLU operation. We utilize an adder and register (Reg) to implement the operation of 1×1 CNN

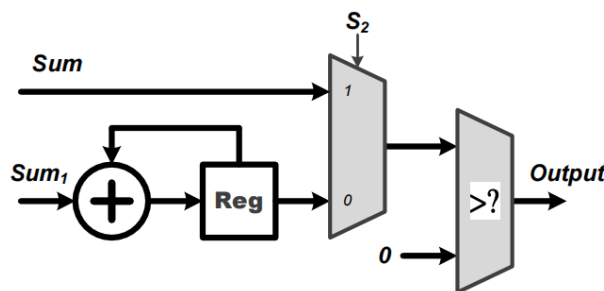


Figure 2.2.3. The architecture of the proposed MaxPooling module

Control Buffer:

The proposed control buffer is the value temporary storage area which consists of 54 registers as shown in Figure 2.2.4. The S5 signal is used to control data feeding into the PE to calculate 1×1 CNN operation, and the selection signal S6 switches the data sending into PE to calculate 6×21 FC, 1×7 CNN, 21×6 FC, and 1×1 CNN operations.

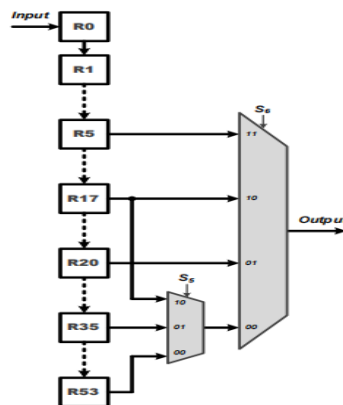


Figure 2.2.4. The architecture of the proposed Control Buffer module

SoftMax:

The proposed SoftMax module calculates the maximum value as the detection output. An adder and a register (Reg) accumulate three results from the PE module to calculate the final layer of the 21×6 FC operations, as shown in Figure 2.2.5. In addition, note that the calculation of the final FC layer is executed by the PE and SoftMax modules, as shown in Figures 2.2.1 and 2.2.5, respectively. Since this final FC layer is in a neural network structure of size 21×6 , there are 21 MAC operations required for producing the numerical result of each of the six output nodes before SoftMax operation.

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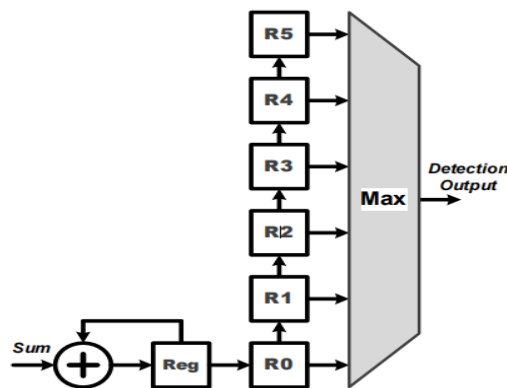
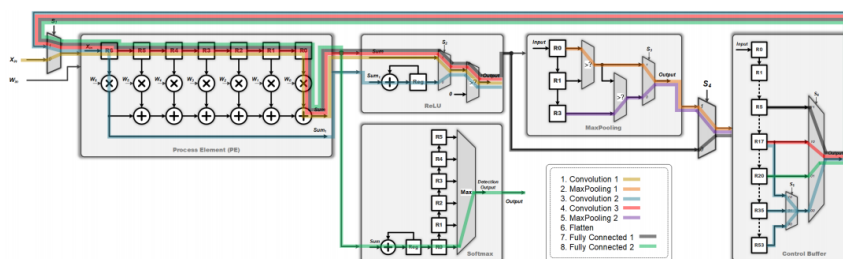


Figure 2.2.5. The architecture of the proposed SoftMax module.

Considering our design in Figure 2.2.2, one may see that the proposed PE module has seven multipliers and six adders. Therefore, to produce the numerical result of each output node, the PE module should execute exactly three times, thus resulting in the required 21 MAC operations in total; each time when the result of one of the three PE executions is obtained, it is immediately sent to the SoftMax module, as indicated by “sum” in Figure 2.2.6. Further observing Figure 2.2.6, one may see that there are a register and an adder in the proposed SoftMax module. The register and adder are used to accumulate the results of the three PE executions to obtain the final numerical result of each output node at the final 21×6 FC layer. Once the weighted sums of all the six output nodes are obtained, the numerical results of all the six output nodes are stored in the registers R0, R1, R2, R3, R4, and R5, respectively. Next, the maximum value of all these weighted sums stored in the register array is then found so the final ECG heartbeat classification result as the detection output is finally determined. In the proposed circuit, there are six multiplexers (MUXs) to control each layer’s operations as tabulated in Table 2.1.1. Table 2.1.2 shows the designated values of the select input(s) of each multiplexer when operating at different layers. Taking the convolution operation of the first layer as an example, we only need to set the values of S1 and S2 to 0 and 1, respectively, and the other multiplexers can be ignored. In this way, the PE module can be used to calculate 1×7 convolution operations of the first convolution layer. The rest of the calculations can be also completed by the settings in Table 2.1.2 using the proposed circuit. By obtaining this, the hardware resources of the proposed circuit can be shared. Figure



2.2.6 illustrates the data flow of each operation in the proposed circuit.

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III. RESULTS AND DISCUSSION

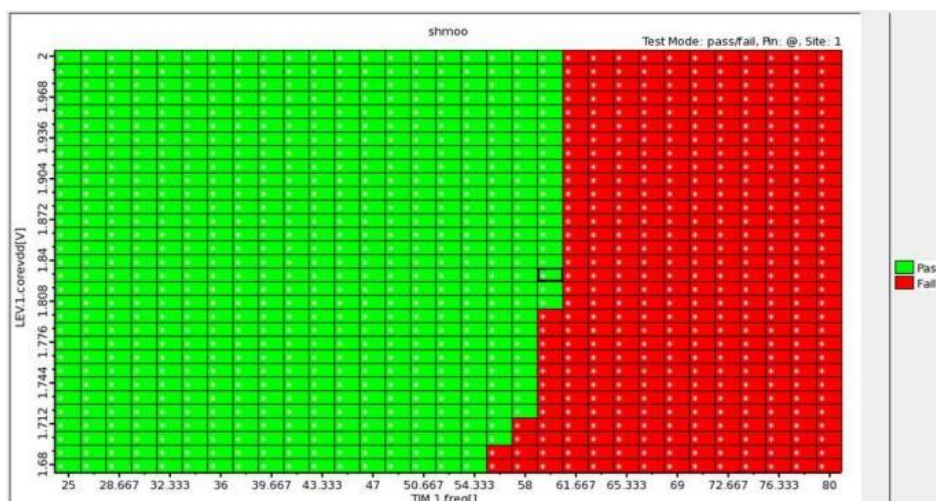
3.1 VLSI Chip Implementation

Taiwan Semiconductor Research Institute (TSRI), which uses the 1.8-V TSMC 0.18- m 1P6M CMOS process technology, was entrusted with the task of turning out the device for the planned CNN accelerator. With a power consumption of 4.4 mW, the suggested core ran at a frequency of 60 MHz. 1.42 mm² made up the chip area.. A frequency of 60 MHz and 4.4mW of electricity were used to run the suggested core. 1.42 mm² was the size of the chip

Table 3.1 chip characteristics of the proposed CNN accelerator

Process Technology	TSMC CMOS 0.18- μ m
Supply Voltage	1.8 V
Clock Frequency	60 MHz
Core Area	1.187 \times 1.196 mm ²
Power Consumption	4.4 mW @ 60 MHz
Latency	13.94 μ s

After the RTL code had been created using the Synopsys Design Compiler, placement and routing had been accomplished using the Cadence Innovus. Advantest V93000 (Scalable SoC Test Platform) device is used testing chip functionality. The testing procedures are as follows: First, the Advantest V93000 equipment was loaded with ECG data taken from the MIT-BIH Arrhythmia Database and measured the device's output data.A shmoo plot(response of a system) of the chip's measurement findings is shown in Figure 3.1. A green "pass" square in the shmoo plot denotes that both the hardware and software findings were satisfactory. According to the measurement results, as shown in Figure3.1, one may see that under a core voltage of 1.8 V, the maximal operating frequency that the chip can achieve is 60MHz.



3.2 Comparison with the Existing Works

Table 3.2 provides a performance comparison among a number of existing works, including the proposed one. First, it can be seen from the table that under the same manufacturing process, had the highest detection accuracy, their system can only detect three types of ECG heartbeats: normal, atrial premature beat, and premature ventricular contraction; moreover, their chip area is also the largest of all works. In addition,the operating frequency of the circuit as proposed by is the highest, but they could not achieve an adequately high accuracy (less than 95%). On the other hand, we may see from Table 3.2 that while the area of the chip as proposed in our study is much smaller than (1.42 mm² vs. 2.47

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mm²), our chip is capable of identifying six types of ECG heartbeats with an adequately high accuracy of 96.83%, indicating that our work may achieve a better chip design than may other works. However, the weakness in our design is the proposed chip has higher power consumption than do the other ones. Note that the power dissipation can be substantially reduced simply by reducing the operating frequency.

Table 3.2 performance comparison of the proposed circuit and a number of existing works

Method	[6]	[7]	[8]	[9]	Proposed
Database	MIT-PTB	MIT-BIH	MIT-BIH	MIT-BIH	MIT-BIH
# of Diseases	1	1	2	1	5
Accuracy	95.8%	97.25%	97.02%	94.94%	96.3%
Technology	90 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Voltage	0.5 V	1.2 V	1.0 V	1.8 V	1.8 V
Frequency	25 MHz	120 Hz	1 KHz	66.6 MHz	60 MHz
Area	4.90 mm ²	2.47 mm ²	N/A	0.73 mm ²	1.42 mm ²
Power	48.06 μW	5.97 μW	5.04 μW	3.1 mW	4.4 mW

3.3 Performance Evaluation for ECG Classification

To demonstrate the performance of the proposed CNN chip, twelve thousand ECG segments in total were utilized for training process to obtain the CNN weights, and three thousand ECG segments were used for testing process. The testing result in terms of detection accuracy was then used to verify the function of the circuit. As a result, the detection results produced by the proposed CNN chip showed that it can achieve 96.3% in overall detection accuracy for the task of ECG heartbeat classification. Table 3.3.1, provides the numbers of ECG segments used for training and testing processes, respectively, for each type of ECG heartbeat. In order to evaluate the performance of the proposed chip for ECG classification, a 6 × 6 confusion matrix, as shown in Table 3.3.2, was further adopted.

Table 3.3.1 number of ECG segments used for training & testing process for each type of ECG.

Item	Diseases	Codename	# of Train	# of Test	Total
1	Normal Beat	N	2000	500	2500
2	Left Bundle Branch Block Beat	L	2000	500	2500
3	Right Bundle Branch Block Beat	R	2000	500	2500
4	Premature Ventricular Contraction	V	2000	500	2500
5	Atrial Premature Beat	A	2000	500	2500
6	Paced Beat	/	2000	500	2500
			12,000	3000	15,000

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Table 3.3.2 Detection results for all six labeled ECG heartbeats.

Labels \ Predict	Predict						
	N	L	R	V	A	/	
N	496	0	0	1	2	1	
L	0	492	0	7	1	0	
R	1	0	488	7	4	0	
V	2	1	2	486	7	2	
A	4	0	16	16	464	0	
/	1	0	0	3	1	495	
Accuracy	99%	98%	98%	97%	93%	99%	

In general, the confusion matrix compares the actual labeled values with those predicted by the proposed CNN model, and each row consists of the predicted values of the labeled heartbeat corresponding to that row. Table 3.3.2 provides the detection results obtained from the chip for all six labeled ECG heartbeats. One may see from Table 3.3.2 that the detection results obtained from the proposed chip for all the ECG events might achieve more than 90% in accuracy, indicating that the proposed CNN chip may be suitably applied for wearable healthcare monitoring devices.

IV. CONCLUSION

In this study, a VLSI chip of the proposed CNN accelerator with applications in ECG heartbeat detection was implemented using a TSMC 0.18 μm COMS technology. The CNN circuit mainly consists of PE, ReLU, SoftMax, MaxPooling, and Control Buffer modules, and all the modules can meet the requirement of repeated use so that utilization may be maximized. As a result, it is revealed from the chip characteristics that the proposed CNN chip achieved a substantially small-area and high-speed design, in comparison to several previous works. Furthermore, the experimental results also demonstrated that the proposed chip can achieve 96.3% overall detection accuracy for identifying six types of ECG heartbeats, and this would represent a significant benefit of this study. We may speculate that the proposed CNN chip may apply to the development and demand for wearable healthcare monitoring devices.

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