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Design and Implementation Low Power High Speed Multiplier using Urdhva Tiryagbhyam Sutra

Ankita Kumara, Shashi Kant Ray, Gajendra Sujediya

Research Scholar, M. Tech (VLSI), RIET JAIPUR, Rajasthan, India

Assistant Professor, RIET JAIPUR, Rajasthan, India

Assistant Professor, RIET JAIPUR, Rajasthan, India

ABSTRACT : Multiplication is one of the basic operations for any high speed digital logic system design, digital signal processors or communication system. Primary issues in design of multiplier are area, delay, and power dissipation. There are many algorithms like booth multiplier, array multiplier, vedic multiplier, compressor based Vedic multiplier for overcoming this problems.

We analyze delay and power of proposed 16x16 CMOS vedic multiplier. It is clear that delay is reduced $\approx 71.85\%$ and power is also reduced $\approx 68.79\%$ as compared to existing vedic multiplier. 20479 transistors is used for the design of this vedic multiplier.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit [1]. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption.

The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n^2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay

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of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

II. BASIC OF VEDIC MULTIPLIER AND ALGORITHM

Early Indian Mathematics

The early Indian mathematicians of the Indus Valley Civilization used a variety of spontaneous tricks perform multiplication. Most calculations were performed on small slate hand tablets, using chalk tables. One technique was of lattice multiplication. Here a table was drawn up with the rows and columns labeled by the multiplicands. Each box of the table is divided diagonally into two, as a triangular lattice. The entries of the table held the partial products, written as decimal numbers. The product could then be formed by summing down the diagonals of the lattice. This is shown below:

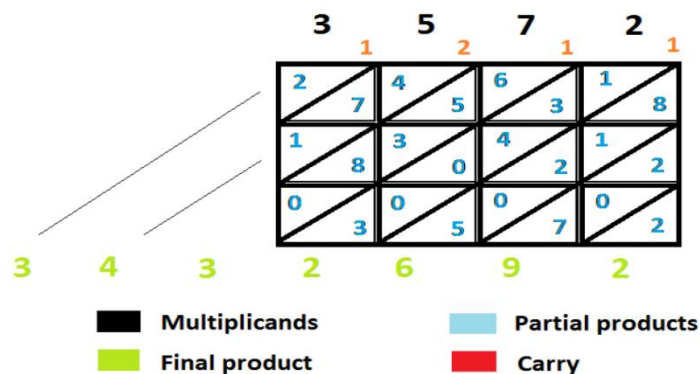


Figure 1 : Example of Early Mathematician Technique

History of Vedic Mathematics

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swahiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why VM has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristic, VM has already crossed the boundaries of India and has become a leading topic of research abroad. VM deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

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- 1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
- 2) Chalana-Kalanabyham – Differences and Similarities.
- 3) Ekadhikina Purvena – By one more than the previous One.
- 4) Ekanyunena Purvena – By one less than the previous one.
- 5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
- 6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
- 7) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
- 8) Paraavartya Yojayet – Transpose and adjust.
- 9) Puranapuranyam – By the completion or non completion.
- 10) Sankalana- vyavakalanabhyam – By addition and by subtraction.
- 11) Shesanyankena Charamena – The remainders by the last digit.
- 12) Shunyam SaamyaSamuccaye – When the sum is the same that sum is zero.
- 13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
- 14) Urdhva-tiryakbhyam – Vertically and crosswise.
- 15) Vyashtisamanstih – Part and Whole.
- 16) Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here.

III. URDHVA TIRYAKBHYAM SUTRA

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in fig 2.1. The algorithm can be generalized for $n \times n$ bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed [10, 4].

Implementation of Vedic Multiplier

The designing of Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Where small blocks are used to design the bigger one. The functionality of each block is verified using simulation software, Tanner EDA 13.00v.

Multiplication of two decimal numbers- 325*738

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.2.2. The digits on the both sides of the line are multiplied and added with

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the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero. To make the methodology more clear, an alternate illustration is given with the help of line diagrams in figure 2.2 where the dots represent bit '0' or '1'.

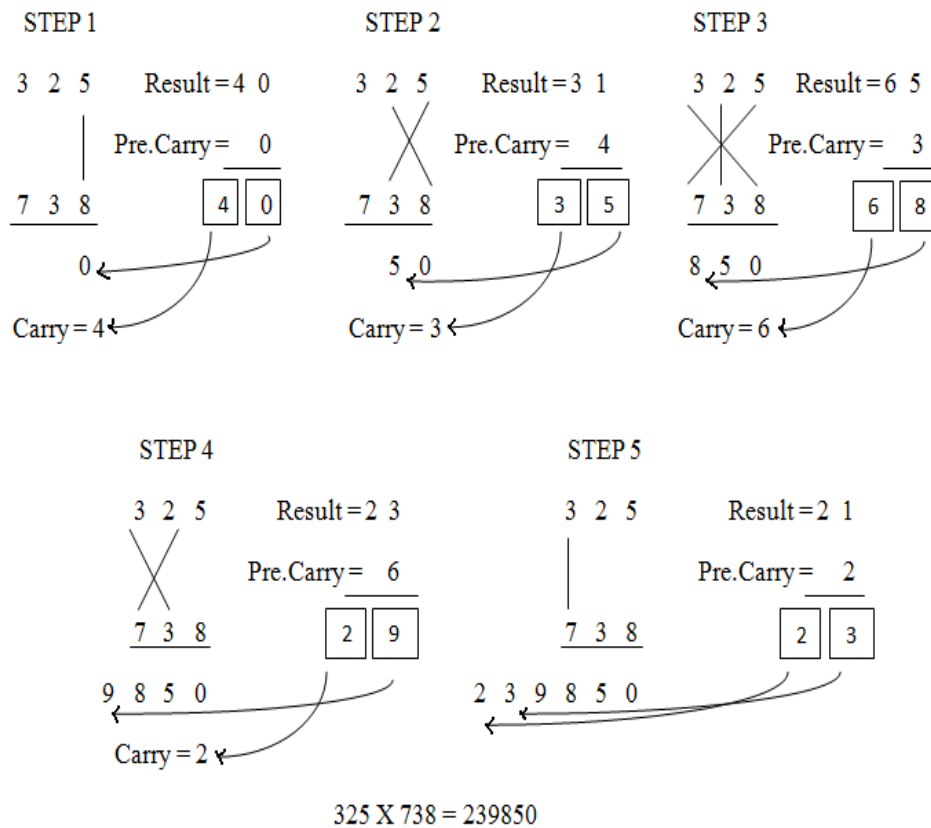


Figure 2: Multiplication of two decimal numbers by Urdhva Tiryakbhyam.

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Implementation of 16 x 16 Bits Vedic Multiplier

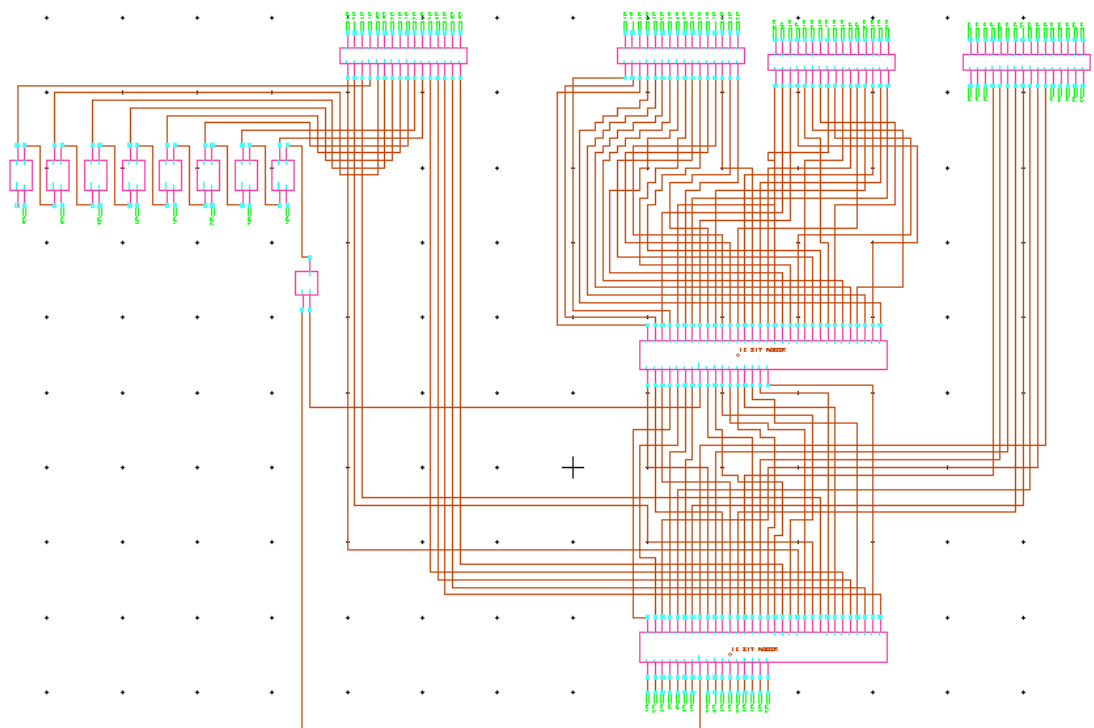


Figure 3 Block diagram of 16 x 16 Vedic Multiplier

The 16X16 bit multiplier structured using 8X8 bits blocks as shown in Figure 3. In this Figure 4.4.2 the 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 8X8 bit multipliers are added accordingly to obtain the 32 bits final product. Thus, in the final stage two adders are also required. Similarly, we have extended same for input bits 32, 64.
RESULT = (Q31- Q16) & (Q15- Q8) & (Q7- Q0)

IV. RESULTS

1.7 Simulation Results of 16 x 16 CMOS Vedic Multiplier

When the given input bit A=a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0 &

B = b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0

A=65,535 (1111 1111 1111 1111)

B=65,535(1111 1111 1111 1111)

Then output its S = 65,025 (1111 1111 1111 1110 0000 0000 0000 0001)

which is shown in given below:

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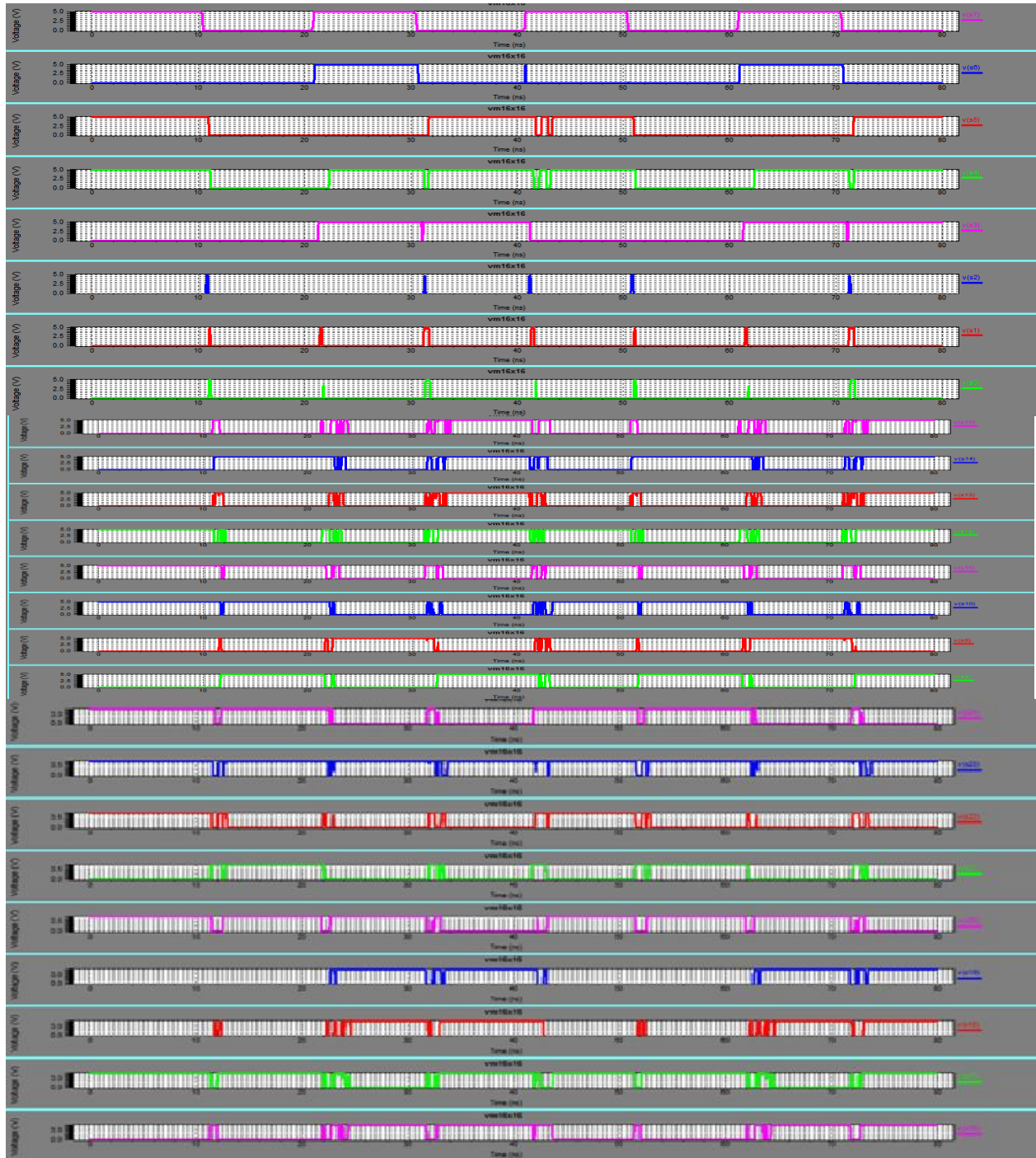


Fig 4 : Output waveform of 16x16 vedic multiplier

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Table 1 : Delay and power dissipation of 16x16 Vedic Multiplier

S. No.	V _{dd} (V)	Delay (ns)	Power (mW)	Transistor count
1.	1.8	20.856	2.878	20479
2.	2	17.580	3.524	
3.	3	16.158	4.441	
4.	4	12.020	7.856	
5.	5	9.087	9.587	

V. CONCLUSION

The design of 16x16 CMOS Vedic multiplier has been implemented on Tanner EDA tool 13.00v. The computation delay for 8x8 bits Vedic multiplier is 9.203 ns at 5V and for 16x16 CMOS Vedic multiplier is 20.856ns at 5V. Since power and delay of proposed Vedic multiplier is reduced as compared to existing multiplier. Thus, it is more efficient for fast multiplication.

REFERENCES

1. Arpita S. Likhitkar , M. N. Thakare , S. R. Vaidya “A Hierarchical Design of 16 -bitn Vedic Multiplier ” Research Scholar, SDCOE, Wardha, India ISSN (Online): 2319-7064.
2. Akshata R , Prof. V.P. Gejji, Prof. B.R. Pandurangi,” ANALYSIS OF VEDIC MULTIPLIER” International conference on computing, communication and energy systems, Dept. of Electronics and Communication Gogte Institute of Technology Belagavi, India.
3. D.Muthulakshmi1, S.Durgadevi2, B.Iyyappan, “High Speed and Reduced Area 16 bit Vedic Multiplier Using Carry Select Adder” International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. II, Issue III, March 2015.
4. Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H, “ Implementation of Multiplier using Vedic Algorithm” International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.
5. Sainadh chintha, Ch. Tirupathi Rao, “ FPGA Implementation of Fast and Power Efficient 4 Bit Vedic Multiplier (Urdhva Tiryakbhayam) using Reversible Logical Gate”, International Journal of IT, Engineering and Applied Sciences Research (IJIEASR) ISSN: 2319-4413 Volume 3, No. 10, October 2014.
6. Shashidhar Shivanagi, Dr. A.B.Kalpana, Kumaraswamy KV, “Do-254 Implementation of High Speed Vedic Multiplier” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization)Vol. 5, Issue 5, May 2016.