

Carbon Nanotube Transistor Based Novel 2:4 Decoder with Minimum Power Consumption at 32 nm Technology Node

Rajbeer Singh¹, Manoj Kumar Bandil²PG Scholar, Department of Electronics & Communication, ITM Gwalior, India ¹Assoc Professor, Department of Electronics & Communication, ITM Gwalior, India²

ABSTRACT: As silicon base technology has reached its bounds by breaking sub micron range and reaching threshold of nanometer range. Semiconductor industry based on silicon technology is looking for an economical and efficient alternative to get into the atomic range which is provided by Carbon Nanotube Field Effect Transistor (CNTFET). In this paper we have designed a novel CNTFET based 2:4 decoder at 32 nm technology by using single walled carbon nanotube and carried out comparative analysis of critical parameters with its CMOS counterpart at 32 nm technology .We have conducted the design analysis by using Spice simulation tools. The comparative study of the design on the basis of leakage power and propagation delay shows that CNTFET outperforms the CMOS based technology.

KEYWORDS: Carbon Nanotube, power consumption, leakage current, propagation delay, silicon, decoder, etc.

I. INTRODUCTION

The pursuit of Moore's Law as prescribed by International Technology Roadmap for Semiconductors (ITRS) has predicted significant intrinsic device hurdles (such as leakage, interconnect, power, quantum effects) to the capabilities as required by the future designs based on CMOS technology. In the future, power efficiency and propagation delay are the main scaling goal for chips used both in small hand held devices and in large data centers [1]. The International Technology Roadmap for Semiconductors (ITRS) has identified Carbon based nanotechnology is one among seven "Beyond CMOS" for accelerated development in future innovations [2]. As with the current trend the line between digital and non digital parts will diminish and only scaling silicon based CMOS (Si-CMOS) will not benefit the market. Hence, there is a call of industry to look for alternative transistor materials for scaling down non digital parts in line with digital parts and pursue more than Moore space [3]. Carbon Nanotube Field Effect Transistor (CNFET) has the ability to do justice to both digital and non digital world.

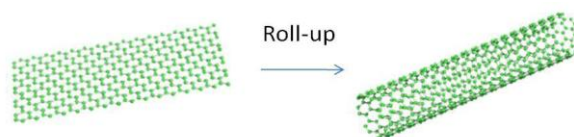


Fig.1. Single carbon nanotube

II. CARBON NANOTUBE FET

In 1991, Sumio Iijima discovered long thin cylinders of carbon known as carbon nanotubes which are nothing but rolled up sheets of graphene [4] as shown in Fig. 1. Due to its unique electrical properties such as higher speed, higher conductivity it is used in CNTFET [5]. Carbon nano tube is used by CNTFET between source and drain instead of silicon channel as used by CMOS [6] as shown in Fig. 2.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

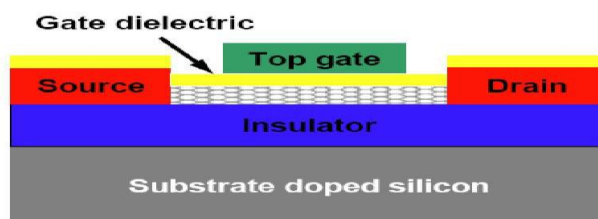


Fig.2. Structure of CNTFET

Basically there are two types of CNTFET structures 1. Multi Wall CNT (MWCNT) which has two structural models, one is Russian Doll model in which a carbon nanotube contains another nanotube inside it and another is Parchment model in which a single graphene sheet is rolled around itself multiple times. 2. Single Walled CNT (SWCNT) in which only a single sheet of graphene is rolled into a cylinder [7]. SWCNT can be formed into three designs depending upon two factors one of which is how graphene is rolled into cylinder which is characterized by wrapping vector also known as chiral vector.

$$c = na_1 + ma_2 \quad (1)$$

Where a_1 and a_2 are lattice unit vectors and the indices (n, m) known as chiral vectors are positive integers of the unit vectors along the graphene structure. While other factor is at which angle graphene sheet is rolled to form a carbon nanotube characterized by chiral angle θ described by

$$\theta = \tan^{-1} \left(\frac{\sqrt{3}m}{m+2n} \right) \quad (2)$$

where n and m are chiral vectors. Chiral vector c and Chiral angle θ decides the chirality of CNT which gives SWCNT three different structures [8], [9] as shown in Fig. 3:

- (a) Zig-Zag ($\theta = 0, m = 0$)
- (b) Arm Chair ($\theta = 30^\circ, n = m$)
- (c) Chiral ($0 < \theta < 30^\circ, n \neq m$)

The SWCNT behaves as metallic when n and m integers are multiple of 3 otherwise as semiconductors with small band energy gap of 0.1eV to 2eV. In this design we have used Stanford 32nm model with chirality $(19, 0)$ [10]

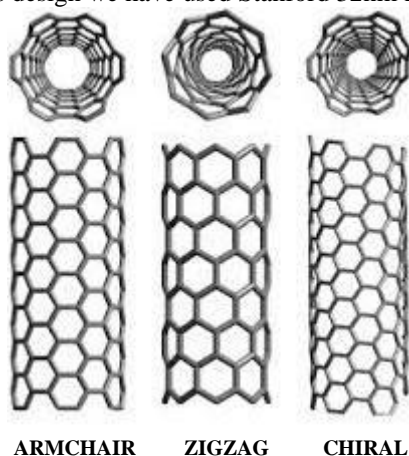


Fig.3. Structure of SWCNT [11]

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

III. PROPOSED 2:4 DECODER CIRCUIT

Decoders are used in many applications in digital world as they are the part of addressing in memory systems and instructional decoder in processors. Decoders are also used for various logic data implementation and multiplexing I/O ports. As speed of modern day processors has increased resulting in high frequency of memory access and large number of instructions which results in high power consumption[11],[12]. Basically, Decoder is a combinational logic circuit that converts code into a set of signals [13]. The name decoder means translating of coded information from one format into another. It is a logic circuit that has 'n' input lines and maximum of 2^n output lines. For each of the combinations of input line only one of the output lines is activated.

As 2:4 decoder has 2 inputs and has 4 outputs along with an Enable input [14] as shown in its general block diagram in Fig. 4 and its truth table is shown in table 1

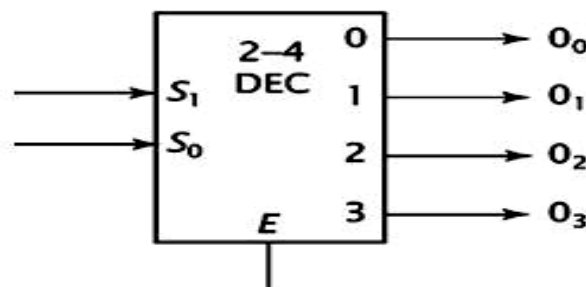


Fig.4. Block Diagram of 2:4 Decoder

A	B	E	D0	D1	D2	D3
X	X	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Table 1: Truth Table of 2:4 Decoder

The Boolean expressions for the output of 2:4 Decoder are as:-

$$D0 = E\bar{A}\bar{B} \quad (3)$$

$$D1 = E\bar{A}B \quad (4)$$

$$D2 = EA\bar{B} \quad (5)$$

$$D3 = EAB \quad (6)$$

The 2:4 decoder can be implemented by two NOT gates and four AND gates [15]. In this paper we have proposed a 2:4 decoder based on the CNTFET as shown in the Fig. 5. As 2:4 decoder is the basic decoder which can be used to build 3 to 8 and other higher decoders. Hence results got by simulation of 2:4 decoders can be used for the designing of higher decoders.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

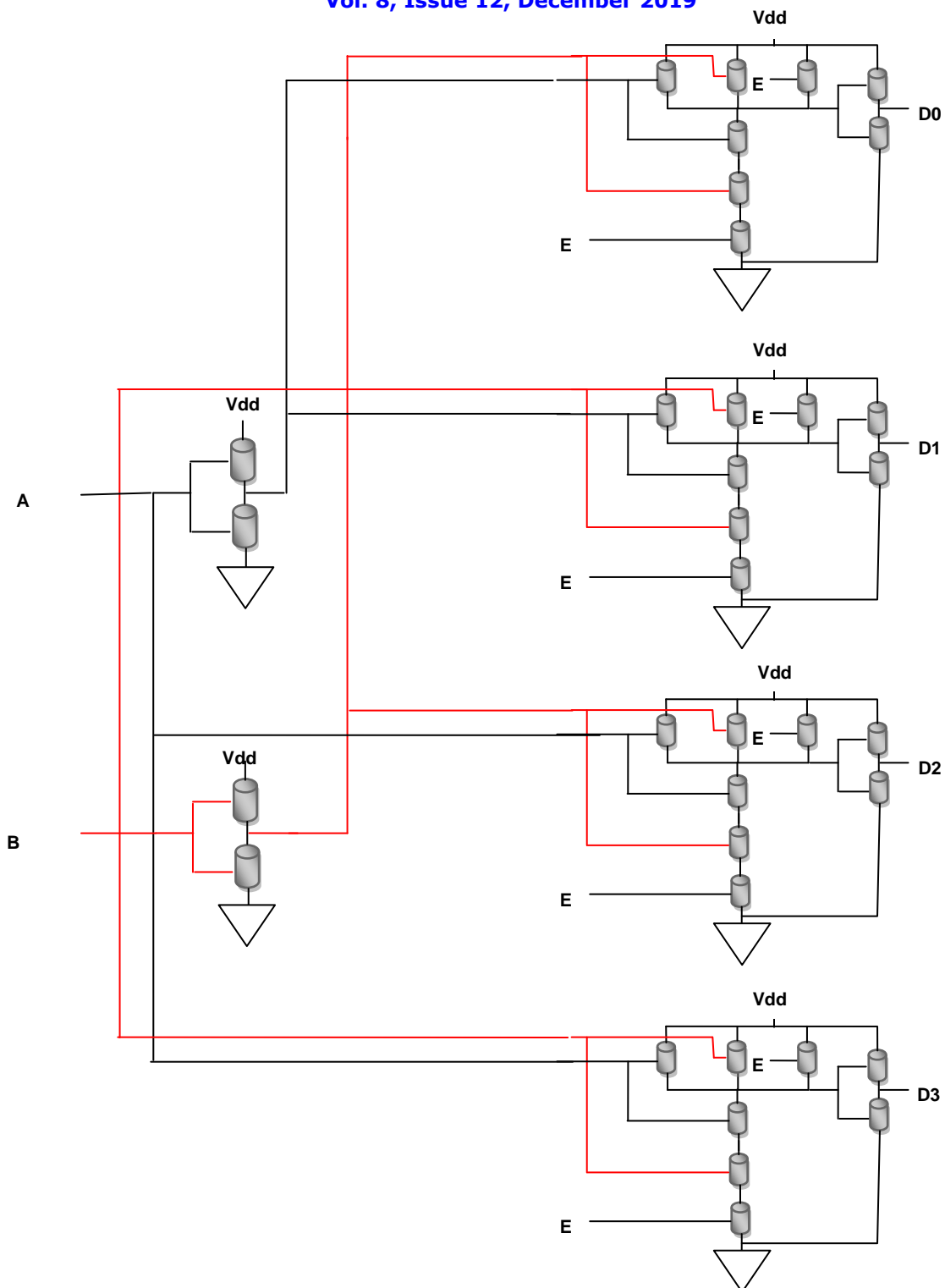


Fig.5. CNTFET based 2:4 Decoder

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

IV. SIMULATED RESULTS

CNTFET based 2:4 Decoder simulated by using SPICE Tool at 32 nm scale and its resulted waveform is shown in Fig. 6. Output spice file showing power consumption is shown in Fig. 7. The comparison of CMOS based 2:4 Decoder, LECTOR based 2:4 Decoder and CNTFET based

2:4 Decoder at operating voltage of 0.7V is shown in Table 2 along with graphical representation in Fig. 8. Results clearly show the improvement in power consumption and propagation delay of CNTFET based 2:4 Decoder as compared to CMOS technology.



Fig. 6 Output waveform of CNTFET based 2:4 Decoder

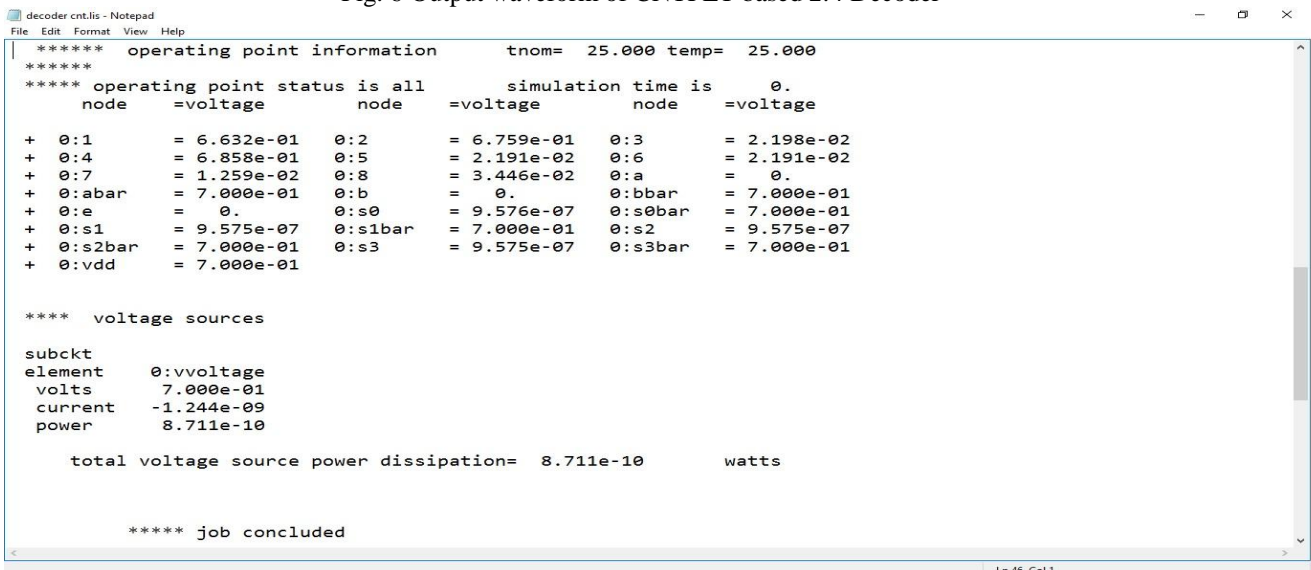


Fig.7. Output File of spice tool

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

Table 2: Simulated results of CNTFET based 2:4 Decoder

Parameters	CMOS based 2:4 Decoder 32nm	LECTOR Technique based 2:4 Decoder 32nm	CNTFET based 2:4 Decoder 32nm
Voltage	0.7v	0.7v	0.7v
Power Consumption	331.0987nW	115.0931nW	0.8711nW
Leakage current	472.9981nA	164.4188nA	1.244nA
Propagation Delay	20.390ps	50.120ps	4.4380ps

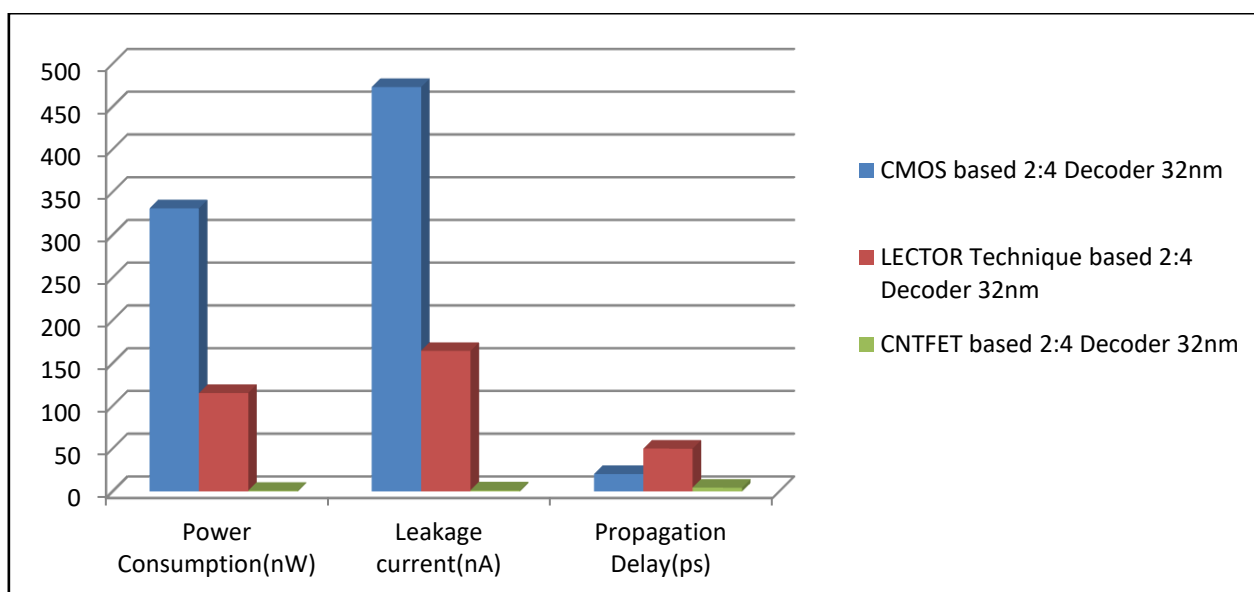


Fig.8. Graph showing reduction in Power Consumption, Leakage Current and Propagation Delay

V. CONCLUSION

As the simulation results show that the CNTFET based Decoder is far better than its CMOS based counterpart. We have carried out simulation on 32nm scale and compared the power consumption leakage current and propagation delay at operating voltage of 0.7v using SPICE tools. From the simulation results we can conclude that CNTFET consumes about 99.74 percent less power and leakage current than CMOS based Decoder along with 78.23% improvement in propagation delay. This improvement is due to the absence of power leakage mechanisms in CNTFET which are dominant in CMOS. The major factor of leakage due to threshold voltage has been eradicated in CNTFET as its threshold voltage increases as we go for further scaling which is contrary to CMOS. Besides, this CNTFET has better transconductance and mobility than CMOS. In future various power saving and delay reducing techniques can be used in CNTFET circuits to further improve its performance and CNTFET can be used for building various digital circuits .

REFERENCES

- [1] Snehlata Murotiya, Aravind Matta, Anu Gupta, "Performance Evaluation of CNTFET-based SRAM cell design," International Journal of Electrical and Electronics Engineering, vol. 2,no. 1,pp. 78-83,2012.
- [2] Semiconductor Industry Association, "The International Technology Roadmap for Semiconductors: MORE MOORE," 2015.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 12, December 2019

- [3] G. Q. Zhang, M. Graef, F. van Roosmalen, "The rationale and paradigm of more than Moore," Electronic Components and Technology Conference 2006, Proceedings.56th, 2006.
- [4] Iijima, S., "Helical microtubules of graphitic carbon," Nature, vol. 354, pp.56-58. (1991)
- [5] J.Guo, Lundstrom and S. Datta, "Performance projections for ballistic carbon nanotube field-effect transistors," Applied Physics Letters, vol. 80, pp. 3192-3194, 2002.
- [6] Adrian Bachtold, Peter Hadley, Takeshi Nakanishi, Cees Dekker, "Logic Circuits with Carbon Nanotube Transistors," Science vol.294, pp. 1317-1320, 9 Nov. 2001.
- [7] J. Appenzeller, "Carbon nanotubes for high performance electronics progress and prospect," Proceedings of the IEEE, pp. 201-211, 2008.
- [8] P. Avouris, J. Appenzeller, R. Martel and A. J. Wind, "Carbon nano tube electronics," Proceedings of the IEEE, vol. 91, pp. 1772-1784, 2003.
- [9] A Zaidi, T.A.Khan, M.Nizamuddin and A.Zaidi, "Design & Simulation of Carbon Nano Tube Based Logic Circuit (Inverter) For Advance Applications," VSRD International Journal of Electrical, Electronics & Communication Engineering, vol.2, no.10, Oct.2012.
- [10] CNTFET Models (2011) [Online] Available: <http://nano.stanford.edu/models>.
- [11] Johnson RR. About carbon/boron nitride nanostructures builder plugin [Internet]. Available from:<http://www.ks.uiuc.edu/Research/vmd/plugins/nanotube/>.
- [12] Ashwin JS, Praveen JS, Manoharan N., "Optimization of SRAM array structure for energy efficiency improvement in advanced CMOS Technology," Indian Journal of Science and Technology.2014; 7(S6):35-9.
- [13] Saikiran Sudhakar, K. Hari Haran and V. Vaithiyathan, "A New approach for low power decoder for memory array," Indian Journal of Science and Technology, August 2016.
- [14] A. Anand Kumar, "Fundamentals of Digital Circuits," Second Edition, Prentice Hall of India, pp.337-340, 2006.
- [15] Pranay Kumar Rahi, Shashi Dewangan, Shital Bhagel, "Design and Simulation of 2-TO-4 Decoder using 32nm, 45nm AND 65nm CMOS Technology," International Journal of Scientific Research Engineering & Technology (IJSRET), vol 4, Issue 3, pp. 270-273, March 2015.