

Review of Built in Self Test Technique in Various Digital Circuit Applications

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ABSTRACT: On-line testing is fast becoming a basic feature of digital systems, not only for critical applications, but also for highly-available applications. To achieve the goals of high error coverage and low error latency, advanced hardware features for testing and monitoring must be included. One such hardware feature is built-in self-test (BIST), a technique widely applied in manufacturing testing. We present a practical on-line periodic BIST method for the detection of operational faults in digital systems. The method applies a near-minimal deterministic test sequence periodically to the circuit under test (CUT) and checks the CUT responses to detect the existence of operational faults. To reduce the testing time, the test sequence may be partitioned into small sequences that are applied separately—this is especially useful for real-time digital systems. Several analytical and experimental results show that the proposed method is characterized by full error coverage, bounded error latency, moderate space and time redundancy.

KEYWORDS: BIST, LFSR, SRAM, CUT, Controller, Latency, Verilog.

I. INTRODUCTION

The field of digital systems has undergone a major revolution in recent decades. Circuits are shrinking in physical size while growing both in speed and range of capabilities. This rapid advancement is not without serious problems, however. Especially worrisome are verification and testing, which become more important as the system complexity increases and time-to-market decreases. The inadequacy of existing verification methods is illustrated by the 1994 Pentium microprocessor's FDIV design error, which cost its manufacturer (Intel) an estimated \$500 million. The inadequacy of existing testing methods is also illustrated by the 1990 breakdown of AT&T's long distance network, which cost AT&T around \$75 million. Due to the high cost of failure, verification and testing now account for more than half of the total lifetime cost of an integrated circuit (IC). Increasing emphasis needs to be placed on finding design errors and physical faults as early as possible in the life of a digital system, new algorithms need to be devised to create tests for logic circuits, and more attention should be paid to synthesis for test and on-line testing. On-line testing requires embedding logic that continuously checks the system for correct operation. Built-in self-test (BIST) is a technique that modifies the IC by embedding test mechanisms directly into it. BIST is often used to detect faults before the system is shipped and is potentially a very efficient way to implement on-line testing.

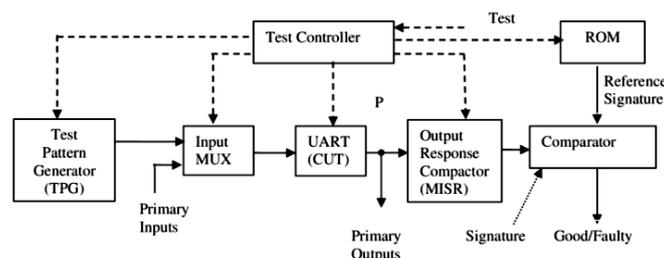


Figure 1: Basic BIST architecture block diagram

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II. LITERATURE REVIEW

W. T. Hale et al.,[2018] A method is proposed to improve system reliability in terms of self-detection and isolation of discrete faults. The application of this method on the design of built-in tests for maintenance is presented using the case of aircraft environmental control system maintenance testing. Built-in testing during aircraft on-ground maintenance allows for wider system input variability due to the absence of operational constraints and requirements. This provides an opportunity to optimally design tests that improve the fault detection and isolation capabilities for operators and maintenance crews. A general mathematical framework for built-in test design is shown using a model-based active fault detection and isolation technique. The motivation for this work is first illustrated through a case study showing the inability to detect and isolate faults at different conditions, demonstrating how system states contribute to these issues. The success of the proposed framework is demonstrated by designing built-in tests that are capable of fully detecting and isolating a multiplicity of faults common to aircraft environmental control systems. It is concluded by presenting the value of the proposed method of detecting and isolating faults, as a solution to a constrained optimization problem with the admissible system inputs as manipulated variables. [1]

K. Akhila, et al.,[2018] Due to ever increasing number of transistors on chip and decrease in feature size have posed challenges in manufacturing and have risen defects due to them. Thus, testing has become vital for any Very Large Scale Integrated (VLSI) design. The design engineers concentrate more on design development and test techniques used to test those designs are neglected due to design cycle time. Any design will not be passed unless it is 100% fault free and Design For Testability (DFT) technique facilitates to detect the faults. Multiple standards are developed to test different parts of Integrated circuits. In this work power efficient & high fault coverage Built In Self-Test (BIST) is designed and implemented to test combinational logic. The developed technique is tested on standard combinational circuits and has given promising results. The conventional Linear Feedback Shift Register (LFSR) is modified to generate all the states, hence improving fault coverage. Compared to conventional method, 100% fault coverage & 12.25% reduction in power is achieved by the proposed design. The design is coded in Verilog, verified for functionality using Xilinx ISIM simulator, synthesized by targeting the design to slow_vdd1v0 1.0 library for 45nm technology using Cadence genus tool and validated on FPGA Spartan 6 boards. [2]

A. K. S. Pundir et al.,[2017] This Work presents an exhaustive review on BIST technique used in different fault tolerant systems and also consider the fault detection methodologies used in these systems. BIST is an alternative method of at-speed testing of high speed ATE that is expensive and having some unavailability issues. With supplement of an external high speed clock, BIST requires on-chip circuitry for vector generation and response analysis. The pseudo-random vectors give a good coverage of stuck-at faults and transition faults even if it is applied at high speed. But in case of robust testing, the Coverage of path-delay faults requires some additional modifications in the combinational logic. BIST also provides the testing feature to test circuits for timing delay. For this a standard BIST architecture with a hybrid pattern generator is required, for replacing LFSR-TPG, which can test both stuck at and delay faults. For test insertion BIST is now universally adopted, this is not only because BIST hardware overheads have come down, particularly for memory BIST (1-3%) [1], [7], [16] but also because it enables partitioning of the testing problem for large hardware systems into small ones so currently memory BIST is preferred [3], [4], [11], [68], [92], [121], and [122]. Most commonly used schemes to provide pattern generation and response compaction for BIST are LFSRs, MISRs and built-in logic block observers. [3]

T. Koshy et al.,[2017] This Major portion of the SoC's are covered by memories. Dense design creates a wide variety of faults leading to the failures in the memory functions. Built-in self-test (BIST) mechanism is a promising method to

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test and diagnose embedded memories like RAMs. The advantages include reduced test cycle duration and fewer complexes. March tests are widely used in production test thanks to their low time complexity and high fault coverage. They were capable of locating and identifying the fault types. Diagnostic data exportation by the BIST is time-consuming since it is exported bit-by-bit. To overcome this, a BIST with March-element-based (MEB) Compression scheme is proposed. MEB Compression scheme can efficiently compress the diagnostic data of a RAM tested by a March test. To optimize the performance of the BIST controller, another design is also proposed here. Detection of different faults in a RAM memory using a single counter based BIST design is advantageous. As a result a fusion of March algorithms like MATS, March C and March X are used for the detection of Stuck-at fault, Coupling fault and Transition fault respectively. Advantages of counter-based BIST architecture includes reduced area overhead and complexity. Compression of the test data is carried out using a decoder module. The implementations are carried out by using Verilog Hardware description language and Xilinx ISE 13.2 design suite. Experimental results shows that the proposed methods reduces the fault detection time, redundant diagnostic data, tester storage requirement, area overhead and complexity in the design. [4]

S. Kostin, et al.,[2014] Two approaches to improve the fault coverage of functional logic BIST in digital circuits are proposed and investigated. The first approach is based on introducing of additional test points. An experimental tool set is developed for fast evaluation of the number of control points that is needed to achieve 100% fault coverage for the given functional test sequence. A novel algorithm is proposed to minimize the number of control points. The second approach is based on complementing the functional test with additional deterministic test patterns. The pros and cons of both approaches are highlighted and discussed. [5]

N. Das, et al.,[2013] The increased circuit complexity of field programmable gate array (FPGA) poses a major challenge in the testing of FPGAs. One of the test challenges is to detect the delay faults in high-speed circuits. Built-in-self-test (BIST) Technique is an ease solution compared with expensive automatic test equipment. In this work, a BIST structure is proposed to detect the delay faults in the various resources of the FPGA such as multiplier, digital signal processing (DSP) block, look-up tables etc. and interconnects of FPGA. The authors have also proposed a full-diagnosable BISTer structure that improves the testing efficiency of the logic BIST. The proposed BISTer structure can diagnose the faulty configurable logic block (CLB), when all the CLBs in the 2×3 BIST are faulty. The proposed scheme has been simulated in Xilinx Vertex FPGA, using ISE tool, Jbits3.0 API and XHWI (Xilinx HardWare Interface) and MATLAB7.0. The result shows significant improvement compared with earlier BIST methods. [6]

M. H. Husin, et al.,[2012] This project emphasized mainly on software analysis. Modelsim-Altera 6.4a is the software that used to generate every single module of the Built-in-Self-Test (BIST) for Random access Memory (RAM) architecture. There are three key things to be concern in the BIST for RAM which is the Test Pattern Generator (TPG), Output Response Analysis (ORA) and RAM. The output of counter which is a type of TPG is analyzed to provide a pattern for March test algorithm. At the mean time, the ORA compare the output from decoder and the RAM output itself which modeled under the theory of numerical autonomy of error vectors from the circuit under test. The output of ORA, the comparator, will show pass or fail for faulty detection of RAM. The system has been successfully developed and vector waveform is used to examine the result of the system. From the result obtained, it showed that the system is working as expected with satisfactory result. [7]

P. Manikandan, et al.,[2010] This work presents SIC based test stimuli with Arithmetic Built in Self-Test (ABIST) concept in order to detect the path delay faults. The presented generator with ABIST stimuli is quite useful for detecting the K-longest path-delay faults of the microprocessor. This work extends the work of Ø. Gjermundnes and

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presents its application and validation to the Intel 8051 microprocessor. The experimental results of this work with the given test case microprocessor allows us to validate the proposed test method is effective by the obtained fault coverage. [8]

Table 1: Summary of literature survey

S No.	Author Name	Year of Publication	Proposed Work	Outcome
1	W. T. Hale	IEEE, 2018	Reliability in terms of self-detection and isolation of discrete faults	A model-based active fault detection and isolation technique
2	K. Akhila,	IEEE, 2018	power efficient & high fault coverage BIST is designed.	100% fault coverage & 12.25% reduction in power.
3	A. K. S. Pundir	IEEE, 2017	BIST fault tolerant systems and also consider the fault detection methodologies	Response compaction for BIST are LFSRs, MISRs and built-in logic block
4	T. Koshy	IEEE, 2016	A BIST with MEB Compression scheme is proposed.	The fault detection time, redundant diagnostic data,
5	S. Kostin	IEEE, 2014	The fault coverage of functional logic BIST in digital.	Functional test sequence. minimize the number of control points
6	N. Das,	IEEE, 2013	A BIST structure the delay faults in the various resources of the FPGA.	Significant improvement compared with earlier BIST methods.
7	M. H. Husin	IEEE, 2012	The BIST for RAM which is the TPG, ORA and RAM.	The system has been successfully developed and vector waveform.
8	P. Manikandan	IEEE, 2010	SIC ABIST concept in order to detect the path delay faults.	Microprocessor allows us to validate obtained fault coverage

III. BIST CHALLENGES

Advantages of implementing BIST include:

- 1) Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated;
- 2) Better fault coverage, since special test structures can be incorporated onto the chips.
- 3) Shorter test times if the BIST can be designed to test more structures in parallel.
- 4) Easier customer support.
- 5) Capability to perform tests outside the production electrical testing environment. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

Disadvantages of implementing BIST include:

- 1) Additional silicon area and Lab processing requirements for the BIST circuits
- 2) Reduced access times.
- 3) Additional pin (and possibly bigger package size) requirements, since the BIST circuitry need a way to interface with the outside world to be effective.
- 4) Possible issues with the correctness of BIST results, since the on-chip testing hardware itself can fail.

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Challenges that need to be considered when implementing BIST are-

- 1) Faults to be covered by the BIST and how these will be tested.
- 2) How much chip area will be occupied by the BIST circuits.
- 3) External supply and excitation requirements of the BIST.
- 4) Test time and effectiveness of the BIST.
- 5) Flexibility and changeability of the BIST.
- 6) How the BIST will impact the production electrical test processes that are already in place.

IV. CONCLUSION

Built in self test is a promising technique to safe and maintain of FPGA and digital circuits. In this paper we review of various built in self test approach for different application and find there are still some parameters constraint, which can be more improved. Area, power, latency and throughput are important concern for high speed digital signal operation. Therefore some need to modify built in self test circuit for advance digital circuit operation.

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