

Joint Channel Estimation and Data Analysing in Large SIMO Wireless Systems

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ABSTRACT: Channel estimation errors have a critical impact on the reliability of wireless communication systems. While virtually all existing wireless receivers separate channel estimation from data detection, it is well known that joint channel estimation and data detection (JED) significantly outperforms conventional methods at the cost of high computational complexity. In this paper, we propose a novel JED algorithm and corresponding VLSI designs for large single-input multiple-output (SIMO) wireless systems that use constant-modulus constellations. The proposed algorithm is referred to as PROjectionOntoconveX hull (PrOX) and relies on biconvex relaxation (BCR), which enables us to efficiently compute an approximate solution of the maximum-likelihood JED problem. Since BCR solves a biconvex problem via alternating optimization, we provide a theoretical convergence analysis for PrOX. We design a scalable, high-throughput VLSI architecture that uses a linear array of processing elements to minimize hardware complexity. We develop corresponding field-programmable gate array (FPGA) and application-specific integrated circuit (ASIC) designs, and we demonstrate that PrOX significantly outperforms the only other existing JED design in terms of throughput, hardware-efficiency, and energy efficiency.

KEYWORDS: FPGA and ASIC designs, joint channel estimation and data detection (JED), large single-input multiple-output (SIMO) wireless systems, biconvex relaxation (BCR).

I. INTRODUCTION

Wireless communication with a large number of antennas at the base-station (BS) will play a major role in fifth-generation (5G) systems. By equipping the BS with hundreds or thousands of antenna elements, large wireless systems enable fine-grained beam forming and, hence, improved spectral-efficiency within each cell compared to traditional communication systems that use a small number of BS antennas. All these advantages come at significantly increased signal-processing complexity at the BS, which necessitates the development of high-performance transceiver algorithms that scale well to large BS array sizes and can be implemented in very-large scale integration (VLSI) circuits at low costs and in an energy-efficient manner.

Existing Method

In the existing system exact ML and GLRT optimal non-coherent detection algorithms in the literature for conventional MIMO systems was used. It was designed a sphere decoder algorithm to achieve the GLRT-optimal non-coherent detection performance for SIMO wireless systems using constant-modulus constellations. The GLRT-optimal non-coherent detection is equivalent to the exact ML non-coherent detection for SIMO systems, when the channel coefficients are independent and identically distributed complex Gaussian random variables and the constellations are constant-modulus. The sphere decoder has a lower expected complexity than the exhaustive search method over a wide range of signal to noise ratio (SNR) and moderate system dimension, for both coherent MIMO detection and non-coherent MIMO detection. However, the sphere decoder approach has two limitations. Firstly, for coherent MIMO detection, at a fixed SNR, the expected complexity of the sphere decoder grows exponentially in system dimension. For non coherent SIMO systems, there is no explicit result on how the complexity of the sphere decoder in grows in the channel coherence time, at a fixed SNR. Secondly, existing GLRT-optimal sphere decoders in only work for constant-modulus constellations in JED. Contrary to sphere decoders which have low expected computational complexity at high SNR, channel state partition approaches can achieve the GLRT-optimal non-coherent detection with worst case computational complexity polynomial in channel coherence time(T). The auxiliary-angle method, one type of channel state partition approach, was first introduced in to perform the ML non-coherent detection. It was considered a

polynomial-complexity Voronoi-cell based approach for solving the low-rank convex quadratic maximization, but in the context of the optimal phase control in wireless MIMO systems with scalar feedback quantization.

Drawbacks of Existing System:

- Approximate separate channel algorithm was used.
- There is a time delay while receiving signals.
- Requires additional antennas to send the signals.
- Errors in the final results.
- The accuracy is low.

PROBLEM IDENTIFICATION IN THE EXISTING METHOD:

- The computational complexity is increased
- Failed to achieve the efficient error rate performance
- Failed to count all the received information
- Hardware complexity is increased

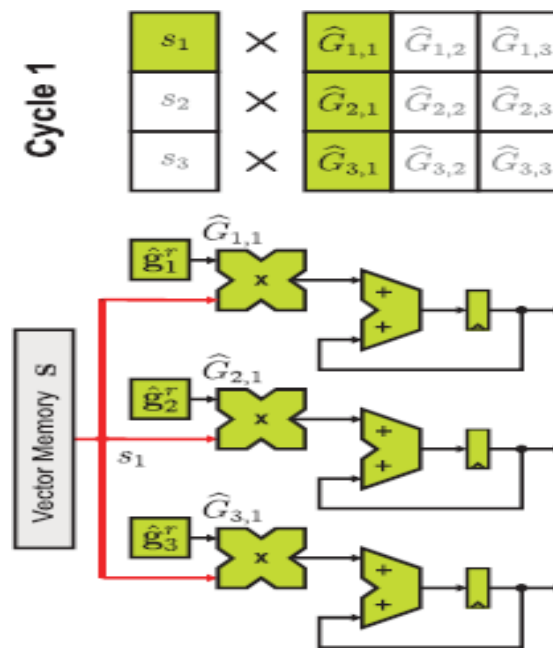


Fig.1. Column by column approach

These problems can be solved by the following considerations:

- By using two memory block the matrix values are stored.
- MAC unit is proposed to reduce the hardware complexity.
- To minimize the area and power the fixed point values are represented.
- Column by column approach is introduced to increase the speed.

II. PROPOSED SYSTEM

In the proposed system, accurate channel state information is not only required in the uplink (to coherently detect data transmitted from the users to the BS), but also required for beam forming or precoding in the downlink (to precisely focus the transmit energy towards the users and to mitigate multi-user interference). The following considerations will be made in the proposed system.

- By using Joint channel estimation and detection algorithm reduce the computational complexity of signal processing.

- To minimize the errors in joint channel wireless communication.
- To Minimize the hardware complexity and increase the speed.

However, the fading nature of wireless channels as well as pilot contamination, i.e., channel training that may be contaminated by pilots or data transmission of users communicating in adjacent cells, render the acquisition of accurate CSI without a significant channel-training overhead a difficult task. Most proposed large wireless systems rely on time-division duplexing (TDD) and perform pilot-based channel training during the uplink phase.



Fig.2 Simple representation of SIMO system

It is, however, well known that the quality of CSI can be improved significantly by joint channel estimation and data detection (JED), which is capable of approaching the performance of idealistic systems with perfect CSI. While a few JED algorithms have been proposed for traditional, small-scale wireless systems their computational complexity is typically high and not much is known about their efficacy for systems with hundreds or thousands of antennas.

Features of existing system:

- BCR Algorithm is used.
- The computational complexity is reduced.
- Preprocessing complexity has been minimized.
- The speed of the architecture has been improved.
- The biconvex problem is eliminated and increase the efficiency.

FUNCTIONAL BLOCK DIAGRAM:

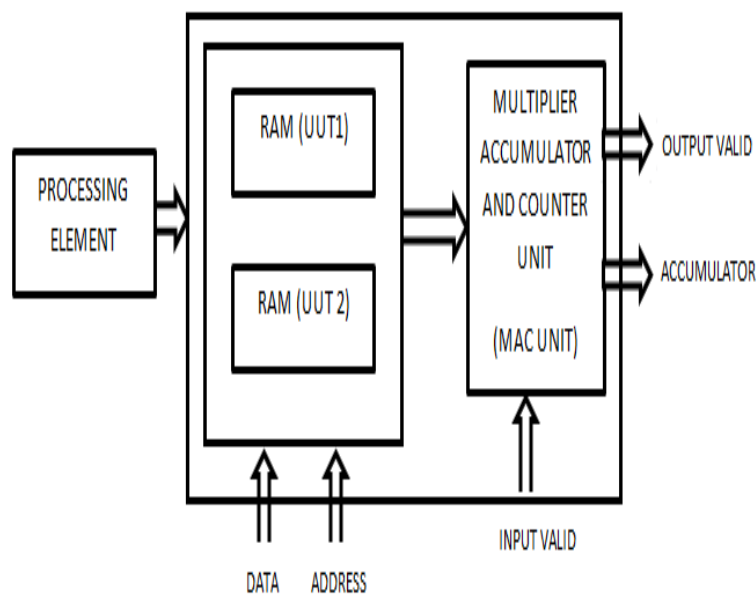


Fig.3 Block diagram of SIMO Wireless Communication systems

The Importance of Accurate Channel State Information

Due to the fine-grained nature of beam forming in such large wireless systems, the acquisition of accurate channel state information (CSI) at the BS is critical for reliable, high-throughput data transmission. In particular, accurate channel state information is not only required in the uplink, but also required for beam forming or precoding in the downlink. However, the fading nature of wireless channels as well as pilot contamination, i.e., channel training that may be contaminated by pilots or data transmission of users communicating in adjacent cells, render the acquisition of accurate CSI without a significant channel-training overhead a difficult task.

Most proposed large wireless systems rely on time-division duplexing (TDD) and perform pilot-based channel training during the uplink phase. It is however, well known that the quality of CSI can be improved significantly by joint channel estimation and data detection (JED), which is capable of approaching the performance of idealistic systems with perfect CSI.

Contributions

In this paper, it propose a novel, computationally efficient and near-optimal JED algorithm for large SIMO wireless systems, and we develop corresponding very-large scale integrated (VLSI) designs. Our contributions are summarized as follows:

- We theoretically analyze the convergence of PrOX, which solves a biconvex problem via alternating optimization.
- We introduce an approximation that significantly reduces the preprocessing complexity of PrOX at virtually no loss in terms of error-rate performance.
- We provide simulation results that showcase the robustness of PrOX to a broad range of system parameters.
- We develop a scalable VLSI architecture for PrOX that uses a linear array of processing elements (PEs) to achieve high-throughput at low hardware complexity.
- We show reference FPGA and ASIC implementation results, and compare our designs to that of the recently-reported JED implementations in.
- We use biconvex relaxation (BCR) to develop PROjection Onto convex hull (PrOX), a novel algorithm that achieves near-optimal JED performance at low complexity.

The results demonstrate that PrOX provides near-optimal JED at significantly lower complexity than existing reference designs.

Related Relevant Results

While a considerable number of algorithms and VLSI designs have been proposed for small- and large-scale multi-antenna wireless systems that separate channel estimation and data detection, only a few results have been proposed for JED. Sphere-decoding (SD) algorithms have been proposed to perform exact maximum-likelihood (ML) JED in SIMO and MIMO systems that use a small number of time slots. Unfortunately, the complexity of SD methods quickly becomes prohibitive for larger dimensional problems and approximate linear methods, which are widely used for coherent data detection in massive MIMO systems, cannot be used for JED. Very recently, a handful of approximate JED algorithms have been proposed for large wireless systems. To the best of our knowledge, reference describes the only VLSI design of a JED algorithm reported in the open literature. While this design achieves near-ML-JED performance, the algorithm relies on semi-definite relaxation (SDR), which lifts the dimensionality of the problem to the square of the number of time slots causing high hardware complexity. In contrast to all these results, PrOX avoids lifting while achieving near-ML-JED performance and can be implemented efficiently in VLSI, even for scenarios that operate with a large number of time slots.

Another line of related work investigates data detection algorithms that are robust to imperfect CSI. The idea is to statistically model channel estimation errors and to solve suitably adapted data detection problems. The resulting algorithms, however, (i) do not achieve the error-rate performance of JED as they are not taking into account all the received information (i.e., from training and data symbols received over multiple time slots) and (ii) do not improve the channel estimate itself the latter is critical in TDD systems that perform beam forming in the downlink using acquired CSI in the uplink. In contrast, we propose JED algorithms that (i) approach optimal error-rate performance as they jointly process all received information and (ii) generate improved channel estimates that can be used for beam forming.

Notation

Lowercase and uppercase boldface letters stand for column vectors and matrices, respectively. For the matrix \mathbf{A} , the Hermitian is \mathbf{A}^H and the k th row and 4 th column entry is $A_{k,4}$. For the vector \mathbf{a} , the k th entry is a_k . The Euclidean norm of \mathbf{a} ,

the Frobenius norm, and the spectral norm of \mathbf{A} are denoted by $\|\mathbf{a}\|_2$, $\|\mathbf{A}\|_F$, and $\|\mathbf{A}\|$, respectively. The real and imaginary parts of the vector \mathbf{a} are $\Re(\mathbf{a})$ and $\Im(\mathbf{a})$, respectively.

Paper Outline

The rest of the paper is organized as follows. Section II describes the system model as well as ML-optimal JED. Section III introduces the PrOX algorithm and provides a theoretical convergence analysis. Section IV details the VLSI architecture for PrOX. Section V shows error-rate performance and VLSI implementation results, and compares PrOX to existing FPGA and ASIC designs. We conclude in Section VI.

III. PROBLEM STATEMENT

While this approach resembles that of conventional, pilot-based data transmission, we emphasize that ML-JED is fundamentally different. In traditional, pilot-based data transmission, a small number of known training symbols are used to generate channel estimates, which are then used during the detection of the data symbols. In contrast, ML-JED uses all received symbols, i.e., pilots and data symbols, to improve the quality of CSI. We also note that ML-JED as in [1] jointly solves for the transmitted data vector \mathbf{s} and the channel vector \mathbf{h} .

IV. PROX: PROJECTION ONTO CONVEX HULL

We now develop a novel algorithm to approximately solve the ML-JED problem in [1] using biconvex relaxation (BCR), a recent framework to solve large semi-definite programs in computer vision.

For the above problem, it is likely to obtain a solution that is inside the convex hull. We are, however, interested in finding solutions that lie at the boundary of the convex hull \mathcal{CO} as the original constellation points in \mathcal{O} lie at the boundary.

Operation Details of the PrOX Architecture To implement the input-cyclic MVP architecture, the entries of the \mathbf{G}_b matrix for the k th PE are stored in the following way: The first address of the PE memory contains $G_{b,k,k}$; the second address contains $G_{b,k,k+1}$, and so on. For example, in the case shown in Figure 5(b), the second PE would have its \mathbf{G}_b matrix entries organized as follows: $\{G_{b,2,2}, G_{b,2,3}, G_{b,2,1}\}$. In the first clock cycle, the k th PE has access to both $G_{b,k,k}$ and $s^{(t-1)}_k$, so it can compute the $G_{b,k,k} s^{(t-1)}_k$ product, and store the result in its accumulator.

At the same time, this PE passes its current $s^{(t-1)}$ entry to the subsequent PE in the chain, i.e., the $(k-1)$ th PE. Passing the current $s^{(t-1)}$ entry to the next PE will be performed in all PEs during all the clock cycles of the MVP computation.

An example of this first clock cycle is shown in Figure 5(b), where the second PE computes $G_{b,2,2}s_2$ and passes the s_2 value to the first PE, so that the first PE has access to s_2 in the second clock cycle.

In the second clock cycle, the k th PE receives $s^{(t-1)}_{k+1}$ from the $(k+1)$ th PE, the previous PE in the array. As a result, the k th PE can compute $G_{b,k,k+1}s^{(t-1)}_{k+1}$ and accumulate it with the previous product. For example, in the second clock cycle of Figure 5(b), the second PE receives s_3 from the third PE and is hence able to compute $G_{b,2,3}s_3$ and add it with $G_{b,2,2}s_2$. In the third clock cycle, the k th PE receives $s^{(t-1)}_{k+2}$ from the $(k+1)$ th PE.

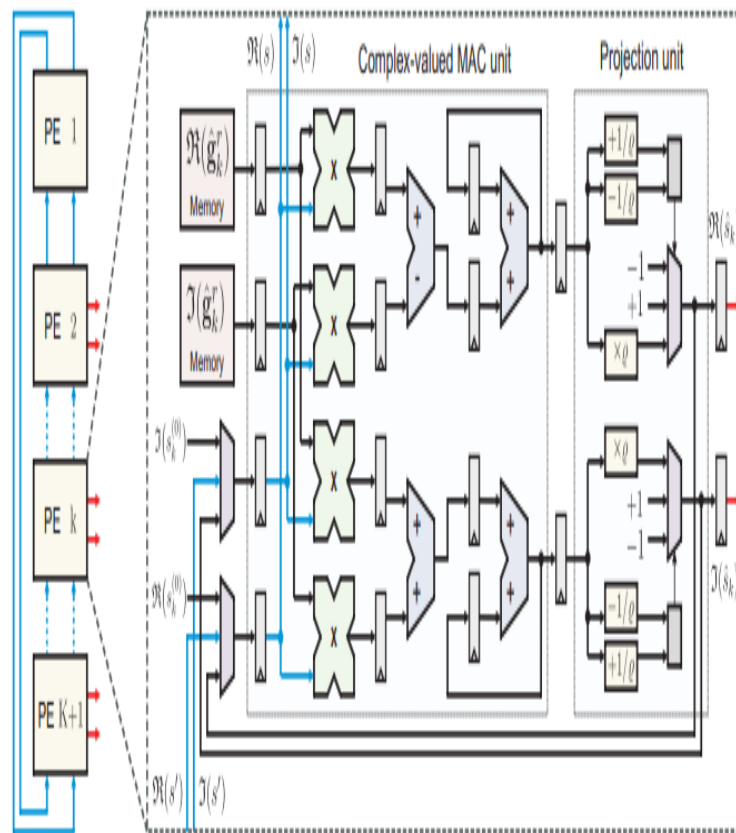


Fig. 4 VLSI architecture of PrOX. Left: linear array of $K + 1$ processing elements (PEs), which enables us to achieve high throughput at low complexity. Right: architecture details of the k th PE, which mainly consists of a complex-valued multiply-accumulate (MAC) unit and a projection unit.

Note that, while the $s(t-1)_{k+2}$ value was initially in the $(k+2)$ th PE, the $(k+2)$ th PE previously passed this value to the $(k + 1)$ th PE. Then, the k th PE has the necessary operands to continue executing its complex-valued MAC operation.

In general, after $K + 1$ clock cycles, all PEs have had access to all the entries of $s(t-1)$ and used them to compute their respective entry of $q^{\sim}(t)$. During this procedure, the first PE (which is implemented differently than the other PEs) executes the same procedure: it passes s^{\sim} to the $(K + 1)$ th PE during the first clock cycle, and in the subsequent clock cycles sends the $s(t-1)$ entry received from the second PE to the $(K + 1)$ th PE. As the MAC units contain three pipeline stages, two clock cycles are required to flush the pipeline.

Hence, the MVP operation in Step of Algorithm 1 is computed in only $K + 3$ clock cycles. We now describe the operation of the projection unit shown on the right side of Figure 1, which implements $s(t) = \text{prox}_{C+1} O(q^{\sim}(t))$.

For QPSK, the projection unit of the k th PE consists of two identical modules: one module takes $q^- = 0$, to determine if $q^- \geq +1/q$, one can also check $q^- \geq +1/q$ or, equivalently, if $q^- - 1/q \geq 0$, which can be extracted from the sign bit of $q^- - 1/q$. Analogously, to determine if q^-

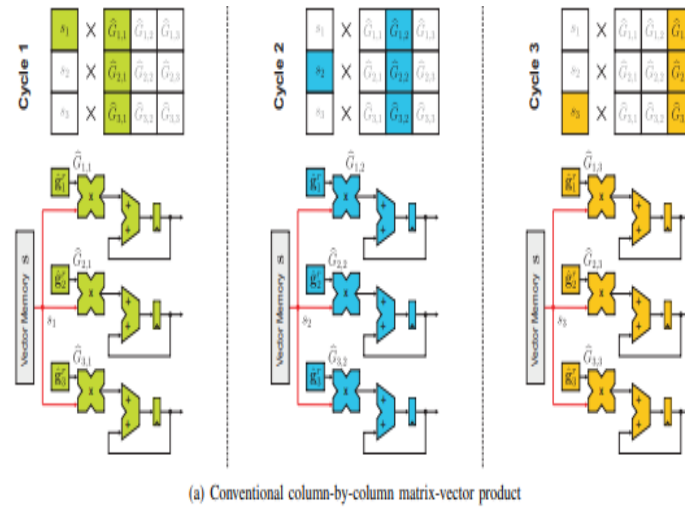


Fig. 5(a) Conventional column by column matrix vector product

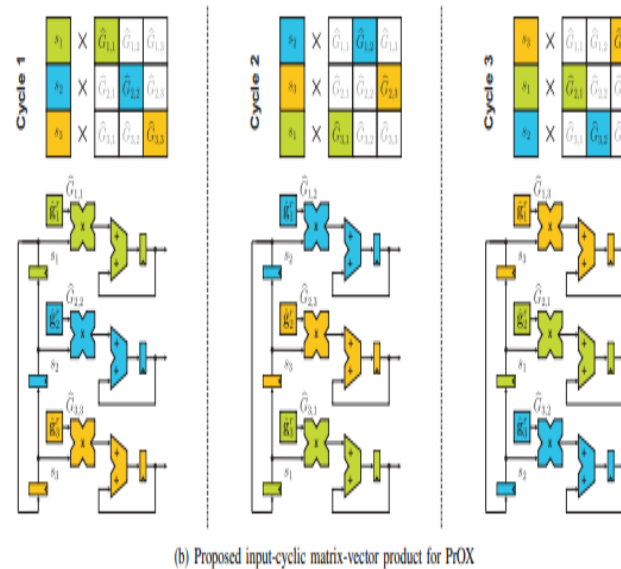


Fig. 5(b) Proposed input cyclic matrix vector product for prox

V.CONVENTIONAL METHOD

Joint channel estimation and data detection (JED) enables near-optimal error-rate performance in realistic wireless communication systems that suffer from channel estimation errors. In this paper, we propose a new JED algorithm and a corresponding FPGA design for large single-input multiple-output (SIMO) wireless systems that use constant modulus constellations. Our algorithm, referred to as ProX (short for PROjection Onto conveX hull), relies on biconvex relaxation (BCR) in order to efficiently compute an approximate solution of the maximum likelihood JED problem that exhibits prohibitive complexity. ProX is a simple and hardware-friendly algorithm that achieves near-optimal error-rate performance for a wide-range of system configurations. To demonstrate the efficacy of ProX, we develop a scalable VLSI architecture and present reference implementation results on a Xilinx Virtex-7 FPGA. Compared to a recently-reported reference JED design, ProX achieves 3→ higher throughput, 20→ better hardware-efficiency (in terms of throughput per look-up tables), and 8→ improved energy-efficiency.

To demonstrate the efficacy of ProX, we develop a scalable VLSI architecture and present reference implementation results on a Xilinx Virtex-7 FPGA. Compared to a recently-reported reference JED design, ProX achieves 3→ higher throughput, 20→ better hardware-efficiency (in terms of throughput per look-up tables), and 8→ improved energy-efficiency. I. INTRODUCTION Large wireless systems, in which the base-station (BS) is equipped with hundreds or thousands of antenna elements, have recently gained significant attention. The large number of BS



antennas enables fine-grained beam forming and improved spectral-efficiency within each cell compared to traditional, small scale single-input multiple output (SIMO) and multiple-input multiple-output (MIMO) wireless systems.

Pilot contamination is known to be a limiting factor in such large wireless systems, i.e., channel training is contaminated by pilot or data transmission of users communicating in adjacent cells. To mitigate the effects of pilot contamination, one can rely on joint channel estimation and data detection (JED), which is capable of approaching the performance of idealistic systems with perfect channel-state information. While a few JED algorithms have been proposed for traditional, small-scale SIMO and MIMO wireless systems, their complexity is typically very high and not much is known about their efficacy for systems with hundreds or thousands of antennas. Moreover, with the exception of the VLSI design in, no hardware designs for JED have been described in the literature.

CONTRIBUTIONS

The JED algorithm and a VLSI design for large SIMO wireless systems that use constant-modulus constellations. Our algorithm, referred to as PrOX (short for PROjection Onto conveX hull), relies on the biconvex relaxation (BCR) framework, a general method for computing approximate solutions to semi definite problems at low complexity. PrOX solves the biconvex problem that arises after relaxing and regularizing the optimal maximum-likelihood (ML) JED problem, enabling near ML-JED performance at low complexity. We develop a scalable VLSI architecture for PrOX that achieves high throughput and low implementation complexity.

VLSI ARCHITECTURE

Architecture Overview

Figure 6(a) shows the proposed VLSI architecture for PrOX in a system with QPSK modulation. Our architecture is a linear array formed of $N = K + 1$ processing elements (PEs), each associated with an entry of s and q^* . To execute Algorithm 1, each PE consists of three key components. The first component is the G_b -matrix memory: The k th PE contains memory for the real and imaginary parts of g^*r .

VI.IMPLEMENTATION RESULTS

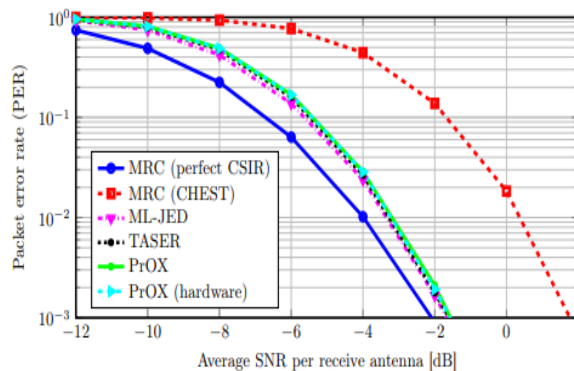


Fig.6(a)

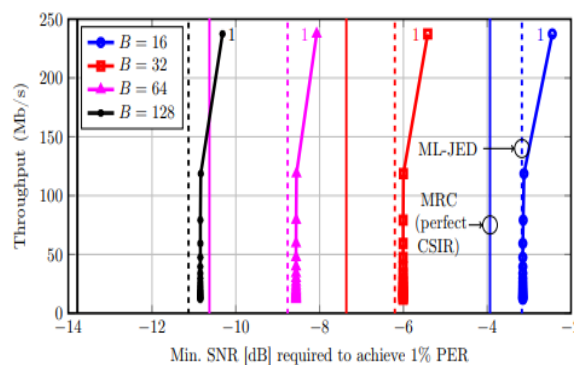


Fig.6(b)

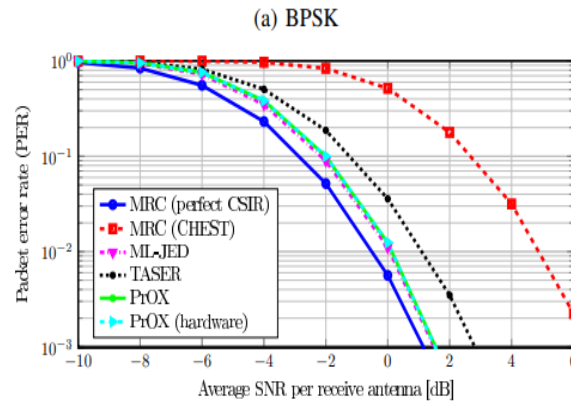


Fig.6(c)

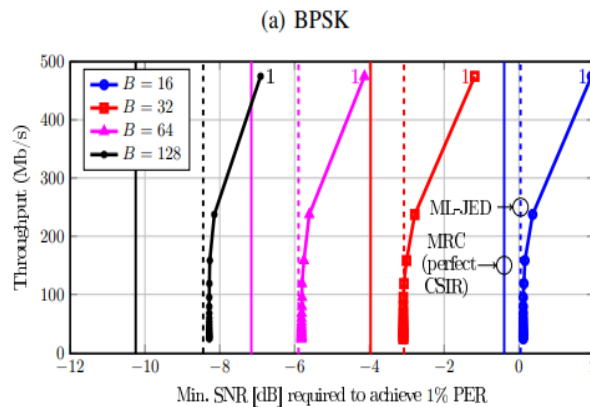


Fig.6(d)

Fig. 5(b) Uncoded packet error rate (PER) for a SIMO system with $B = 16$ BS antennas and transmission over $K = 16$ time slots.

PrOX achieves near optimal PER performance (close-to perfect CSIR) and exhibits a performance similar to ML-JED. TASER entails a 1 dB SNR loss for the QPSK case, while conventional MRC with CHEST suffers a 4 dB SNR loss. This memory is implemented using FPGA lookup tables (LUTs) as distributed RAM. We assume that the memory contents were computed during a pre-processing step. The second component is a complex-valued multiply-accumulate (MAC) unit, used to compute the matrix-vector product in line 3 of Algorithm 1.

The third component is the projection unit, which executes line 4 of Algorithm 1. The hard-output estimates (see line 7 of Algorithm 1) are extracted from the sign bits of the outputs of the projection unit. As $s(t) = \tilde{s}$ is forced at the end of each iteration (line 5 of Algorithm 1), the first PE only contains two multiplexers and flip-flops that stores.

Fixed-Point Parameters

We use 6 bit fixed-point values for representing the $s(t)$ entries, with 3 fraction bits. For the elements of G_b , 12 bit fixed-point values are used, with 11 fraction bits. The intermediate values and outputs of the complex-valued MAC unit use 15 bits with 11 fraction bits.

VII. IMPLEMENTATION RESULTS AND COMPARISON

Error-Rate Performance Figures 6(a) and 6(b) show packet error rate (PER) simulation results for PrOX as in (5) for $t_{max} = 5$ iterations. The results are obtained from 50,000 Monte-Carlo trials in a $B = 16$ BS antenna SIMO system with $K = 16$ time slots, using an i.i.d. flat Rayleigh block fading channel model. We show the performance of maximum ratio combining (MRC) detection with both perfect receive-side channel state information (CSIR) and channel estimation (CHEST), ML-JED.

Table.1 Implementation results on a XILINX VIRTEX-7

Array size ($N=K+1$)	$N=5$	$N=9$	$N=17$	$N=33$
Time slots ($K=N-1$)	$K=4$	$K=8$	$K=16$	$K=32$
Slices	327	658	1491	3018
LUTs	990	1991	4818	9861
FFs	515	989	1953	3857
DSP48s	16	32	64	128
Max. clock freq. [MHz]	358	341	297	240
Min. latency [cycles]	8	12	20	36
Max. throughput ^a [Mb/s]	358	454	475	426
Power estimate ^b [W]	0.45	0.47	0.79	1.14

The joint channel estimation and data detection (JED) algorithm for large SIMO systems with constant modulus constellations, as well as a VLSI architecture. The low complexity of ProX translates into a low-area, high-throughput, and low-power FPGA design. Our FPGA implementation for a SIMO system with $K = 8$ time slots achieves a maximum throughput of 454 Mb/s, while using only 2 k FPGA LUTs. In addition, ProX significantly outperforms, the only other existing JED design, in all performance metrics. We conclude by noting that ProX is a first step towards hardware accelerators that are able to find approximate solutions to the Max Cut problem at low complexity and in a hardware-efficient manner. The design of accelerators for MIMO JED is part of ongoing research.

MAC UNIT:

The Multiplier-accumulator (MAC) unit supports large number of digital signal processing (DSP) applications. It also furnishes signal processing ability to the microcontroller for various applications such as servo/audio control etc. MAC, being an execution unit in the processor implements a 3-stage pipelined arithmetic architecture which optimizes 16×16 multipliers.

This design supports both 16-bit and 32-bit operands. It also supports signed/unsigned integers plus signed, fixed-point fractional input operands.

The MAC unit supports mainly three functions:

- Signed and unsigned integer multiplies
- Multiply-accumulate operations supporting signed, unsigned, and signed fractional operands
- Miscellaneous register operations An accumulator adder and multiplier together form a MAC unit. Usually Carry-select/Carry-save adders are mostly implemented due to the DSP application requirement of fast speed. The memory fetches the inputs from its location to multiplier for further multiply-accumulate operations. The generated result of MAC unit is stored at a relevant memory location. The situation demands that this complete process should be carried out into a single clock cycle

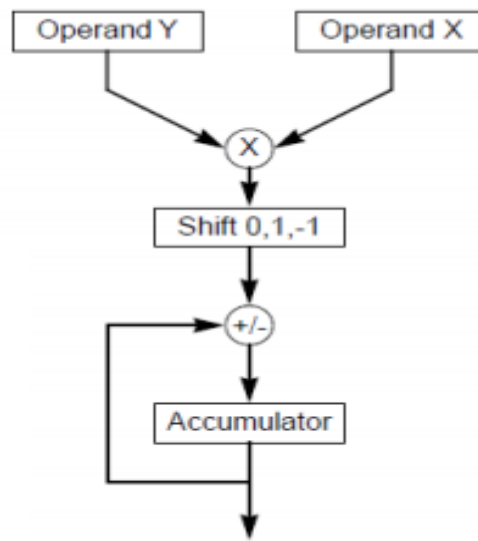


Fig. 7 Block diagram of MAC unit

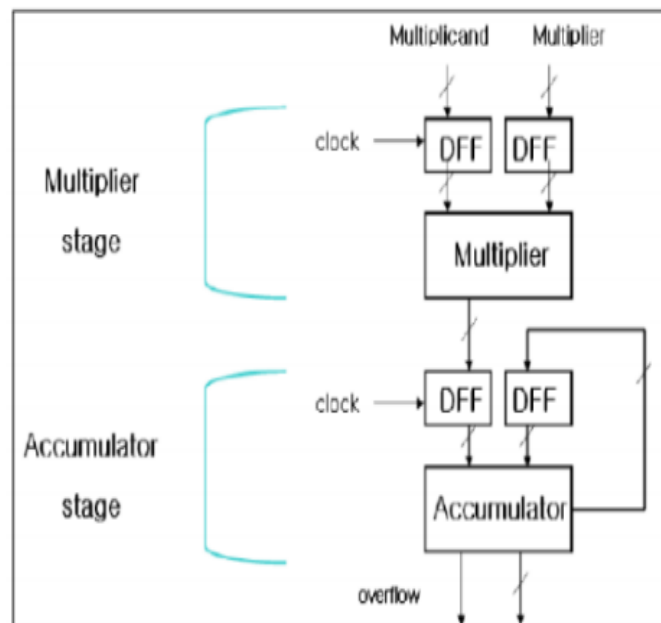


Fig. 8 Architecture of MAC unit

This architecture makes use of multiplier-accumulator (MAC) of finite field of order 2^m . Proposed architecture is designed on the basis of Karatsuba-ofman algorithm in order to reduce the area. On the other hand, data paths are designed on the basis of Montgomery ladder algorithm so as to obtain shortest data-path execution. The goal of this is to speed-up the ECSM thereby achieving area reduction. The architecture is comprised of mainly two blocks:

- 1) Non-pipelined FF Squarer and
- 2) Pipelined bit-parallel FF MAC Thorough analysis of pipeline registers helps to determine the optimal no. of pipeline stages which states that the proposed method is far better than the existing methods in terms of area and speed.

Various practical applications such as image restoring and signal recovery obtained by inclusive sensing utilize sparse signal recovery mechanism.

VIII. LITERATURE REVIEW

Joint Channel Estimation / Data Detection in MIMO-FBMC/OQAM Systems – A Tensor-Based Approach

Filter bank-based multicarrier (FBMC) systems are currently being considered as a prevalent candidate for replacing the long established cyclic prefix (CP)-based orthogonal frequency division multiplexing (CP-OFDM) in the physical layer of next generation communications systems. In particular, FBMC/OQAM has received increasing attention due to, among other features, its potential for maximum spectral efficiency. It suffers, however, from an intrinsic self-interference effect, which complicates signal processing tasks at the receiver, including synchronization, channel estimation and equalization. In a multiple-input multiple-output (MIMO) configuration, the multi-antenna interference has also to be taken into account. (Semi-)blind FBMC/OQAM receivers have been little studied so far and mainly for single-antenna systems. The problem of joint channel estimation and data detection in a MIMO-FBMC/OQAM system, given limited or no training information, is studied in this paper through a tensor-based approach in the light of the success of such techniques in OFDM applications. Simulation based comparisons with CP-OFDM are included, for realistic transmission models.

A Simple Design for Joint Channel Estimation and Data Detection in an Alamouti OFDM System

To obtain full benefits of the Alamouti space-time code design on a time-varying acoustic channel, the channel variation is decoupled into two parts: the gain, which is assumed to be constant over an Alamouti pair (two consecutive OFDM blocks), and the phase, which is not restricted in this manner, but allowed to vary from one block to another in a piecewise linear fashion. Under this model, the receiver assumes a simplified structure in which conventional Alamouti data detection and channel estimation are aided by Doppler tracking. System performance is demonstrated using experimental data transmitted over a 1 km shallow water channel in the 8-18 kHz acoustic band, using QPSK modulation and a varying number of carriers (up to 1024). The proposed design shows a gain of up to 2 dB as compared to the reference single-transmitter case.

Massive MIMO for next generation wireless systems

Multi-user MIMO offers big advantages over conventional point-to-point MIMO: it works with cheap single-antenna terminals, a rich scattering environment is not required, and resource allocation is simplified because every active terminal utilizes all of the time-frequency bins. However, multi-user MIMO, as originally envisioned, with roughly equal numbers of service antennas and terminals and frequency-division duplex operation, is not a scalable technology. Massive MIMO (also known as large-scale antenna systems, very large MIMO, hyper MIMO, full-dimension MIMO, and ARGOS) makes a clean break with current practice through the use of a large excess of service antennas over active terminals and time-division duplex operation. Extra antennas help by focusing energy into ever smaller regions of space to bring huge improvements in throughput and radiated energy efficiency. Other benefits of massive MIMO include extensive use of inexpensive low-power components, reduced latency, simplification of the MAC layer, and robustness against intentional jamming. The anticipated throughput depends on the propagation environment providing asymptotically orthogonal channels to the terminals, but so far experiments have not disclosed any limitations in this regard. While massive MIMO renders many traditional research problems irrelevant, it uncovers entirely new problems that urgently need attention: the challenge of making many low-cost low-precision components that work effectively together, acquisition and synchronization for newly joined terminals, the exploitation of extra degrees of freedom provided by the excess of service antennas, reducing internal power consumption to achieve total energy efficiency reductions, and finding new deployment scenarios. This article presents an overview of the massive MIMO concept and contemporary research on the topic.

Bayes-optimal joint channel-and-data estimation for massive MIMO with low-precision ADCs

This paper considers a multiple-input multiple-output (MIMO) receiver with very low-precision analog-to-digital converters (ADCs) with the goal of developing massive MIMO antenna systems that require minimal cost and power. Previous studies demonstrated that the training duration should be relatively long to obtain acceptable channel state information. To address this requirement, we adopt a joint channel-and-data (JCD) estimation method based on Bayes-optimal inference. This method yields minimal mean square errors with respect to the channels and payload data. We develop a Bayes-optimal JCD estimator using a recent technique based on approximate message passing. We then present an analytical framework to study the theoretical performance of the estimator in the large-system limit. Simulation results confirm our analytical results, which allow the efficient evaluation of the performance of quantized massive MIMO systems and provide insights into effective system design.

A 74.8 MW soft-output detector IC for 8×8 spatial-multiplexing MIMO communications

In this paper, VLSI implementation of a configurable, soft-output MIMO detector is presented. The proposed chip can support up to 8×8 64-QAM spatial multiplexing MIMO communications, which surpasses all reported MIMO detector ICs in antenna number and modulation order. Moreover, this chip provides configurable antenna number from 2×2 up to 8×8 and modulation order from QPSK to 64-QAM. Its outputs include bit-wise log likelihood ratios (LLRs) and a candidate list, making it compatible with powerful soft-input channel decoders and iterative decoding system. The MIMO detector adopts a novel sphere decoding algorithm with high decoding efficiency and superior error rate performance, called modified best-first with fast descent (MBF-FD). Moreover, a low-power pipelined quad-dual-heap (quad-DEAP) circuit for efficient node pool management and several circuit techniques are implemented in this chip. When this chip is configured as 4×4 64-QAM and 8×8 64-QAM soft-output MIMO detectors, it achieves average throughputs of 431.8 Mbps and 428.8 Mbps with only 58.2 mW and 74.8 mW respective power consumption and reaches 10^{-5} coded bit error rate (BER) at signal-to-noise ratio (SNR) of 24.2 dB and 22.6 dB, respectively.

And development of wearable tremor suppression technology have shown a promising third solution for tremor management. Tremor is a rhythmical and involuntary oscillatory movement of a body part and it is one of the most common movement disorders. Orthotic devices have been under investigation as a noninvasive tremor suppression alternative to medication or surgery. The Challenge in musculoskeletal tremor suppression is estimating and attenuating the tremor motion without impeding the patient's intentional motion. The device is designed as wearable and personal equipment using wireless communication. Tremor is continuously monitored with help of heart beat sensor, temperature sensor and accelerometer. Sensor output is given to controller which is used to control the valve with help of driver circuit for controlling tremor action. Non return valve is used to arrest the air pressure in the valve. SMS to the doctor or relatives using GSM modem automatically if the heart beat is high and tremor is not controlled by maximum times of suppression.

III. RESULTS AND CONCLUSION

In the Proposed system joint channel estimation and data detection (JED) algorithm is low computational complexity for large SIMO systems with constant-modulus constellations. We have provided theoretical convergence guarantees for PrOX and introduced an approximation that significantly reduces the pre-processing complexity.

To demonstrate the effectiveness of our algorithm, we have proposed a VLSI architecture that consists of a linear array of processing elements (PEs). Our architecture enables high-throughput near-ML-JED at low silicon area and power consumption. We have provided FPGA and ASIC implementation results, which demonstrate that PrOX significantly outperforms the only other existing JED design in terms of hardware- and energy-efficiency as well as error-rate performance.

More generally, PrOX constitutes a first step towards hardware accelerators that are able to find approximate solutions to problems that resemble. Finally, while some algorithms exist for JED in the MIMO case and for general constellation sets they are either computationally complex or exhibit a considerable loss with respect to the optimal ML-JED performance.

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