

FPGA-Based Implementation of MicroBlaze Processor as UART Soft IP Core

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ABSTRACT: The present research work focuses on the implementation of MicroBlaze processor as Universal synchronous Receiver / Transmitter (UART) Soft IP Core based on the Field Programmable Gate Array (FPGA). Xilinx ISE's Core Generator tool was used to design the soft IP core embedded with the MicroBlaze MCS. Xilinx Spartan 3E Field Programmable Gate Array (FPGA) device was preferred for implementing the Soft IP core.

KEYWORDS: VHDL, FPGA, Xilinx, MicroBlaze Processor, UART, IP Core.

I. INTRODUCTION

The present paper is an outcome of a research work in which the FPGA based MicroBlaze processor as UART soft IP core was developed for serial communication between various systems. In this work we deployed Digilent Nexys 2 board consisting of Spartan 3E FPGA device with personal computer. The present prototype developed in this research work display the status of switches present on the board itself was displayed on HyperTerminal as well as on the LEDs on the board. The reconfigurable device was hardwired using FPGA based 'MicroBlaze' processor; working as Universal Asynchronous Receiver /Transmitter (UART). As stated in (MicroBlaze Processor Reference Guide,2012), the soft core processor for MicroBlaze is extremely configurable, which allows user design to select its explicit set of features. The serial communication is carried out using RS232 cable connected between FPGA board and COM port of PC. For this the UART soft IP core is designed by the use of Core Generator system present in Xilinx Integrated Software Environment (ISE) design suit. Xilinx's Embedded Development Kit (EDK) is a package designed to build Xilinx FPGAs with MicroBlaze embedded processor systems. The core generator system includes this soft core processor [1]. The design flow is targeted on Nexys2 Spartan 3E FPGA board; developed by Digilent Inc. for MicroBlaze embedded soft processor core. The Nexys2 reference guide is provided in [3]. Xilinx CORE Generator System consists of a soft processor core, which significantly improves the time required for design by providing Xilinx FPGAs with access to Intellectual Properties (IP). Architecture specific, domain-specific and market specific IPs are provided by CORE Generator [4].

II. DESIGNING OF MICROBLAZE PROCESSOR AS UART SOFT IP CORE

The CORE Generator System is a design tool which offers optimized Xilinx FPGAs with parameterized Cores. It gives a catalog of ready-made functions. A MicroBlaze MCS embedded processor was designed using Xilinx ISE Design flow. The processor was designed using Core-Generator system. The processor core was located in Embedded Processing menu of the Architecture Wizard Intellectual Proprietary (IP) Cores. The system development was done for Nexys2 board. It consists of the on-board clock source producing 50 MHz clock signal. Thus, the I/P clock frequency was configured 50 MHz for the MicroBlaze processor. For the processor 16KB memory size was selected. To input the digital data a GPI port of the processor was set to accept an 8 bit value. An output was also taken from the processor output and displayed on the Light Emitting Diodes (LEDs) available on the board. For that the MicroBlaze GPO port was set to the same number of outputs to that of GPI port. The UART port of the processor was programmed to send ASCII data elements serially at the baud rate of the order of 9600. The UART Receiver and Transmitter were enabled. The Fig.1 interprets the input output lines of the MicroBlaze processor; indicating the ports that are being utilized in this soft IP core development. The 'Generate' button on the wizard shown in Fig.1 generates the Xilinx core with .xco and it was revealed in the hierarchy of the main project.

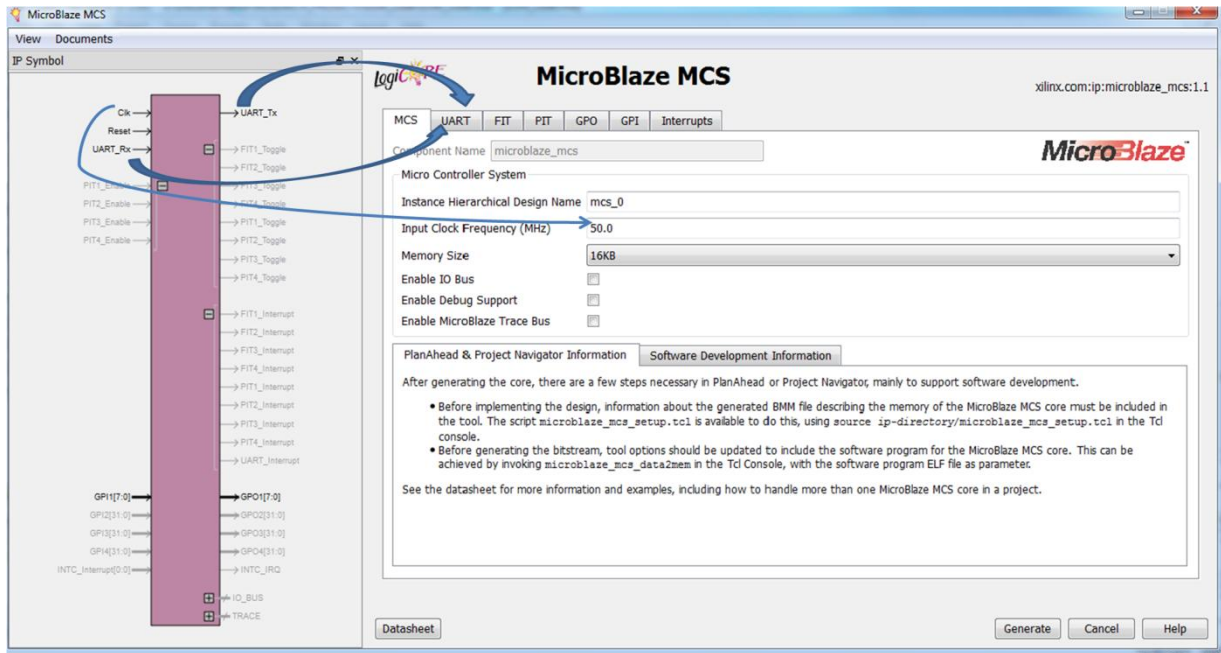


Fig.1. Xilinx MicroBlaze MCS Processor Configured for 50 MHz input clock, 9600 Baud Rate for UART and 8 bit GPI/GPO

A new top level entity 'microblaze_mcs_top' was created. For the top level module the source code has been developed as shown in Fig. 2 below. The darkened rectangle depicts the the top level entity and the port mapping.

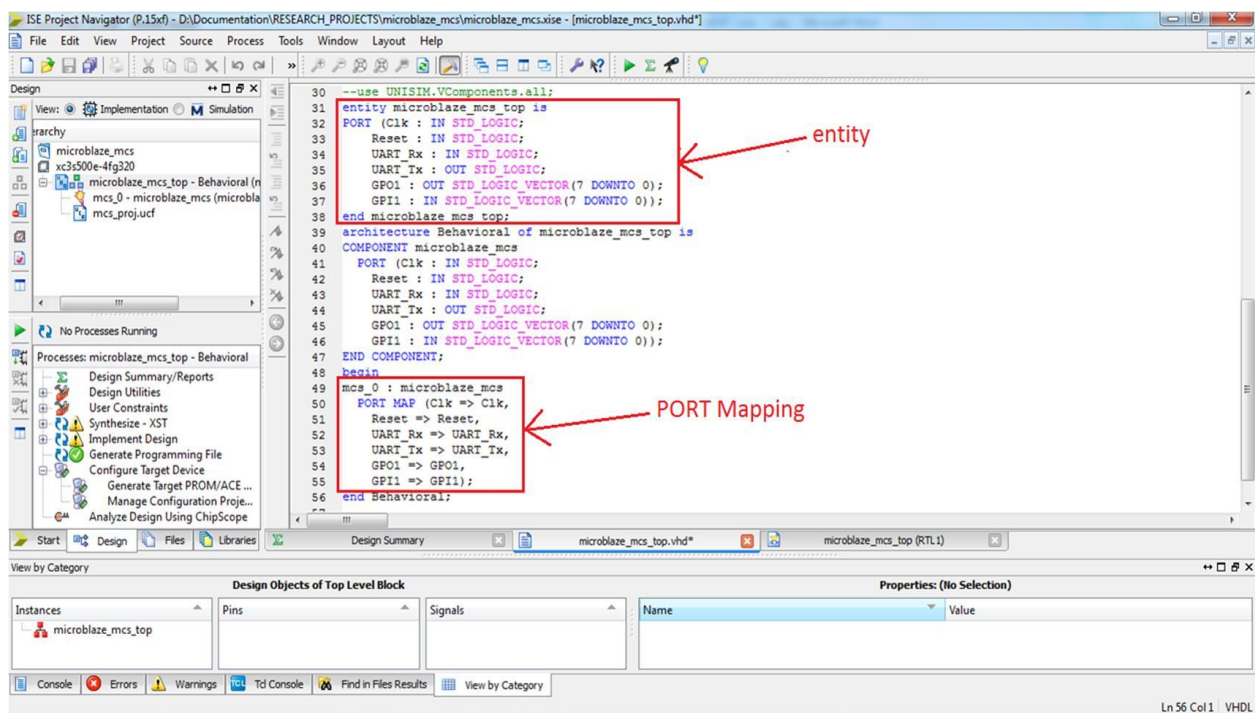


Fig.2. source code of Top level module in Xilinx ISE Project Navigator Tool

III. SYNTHESIS RESULT

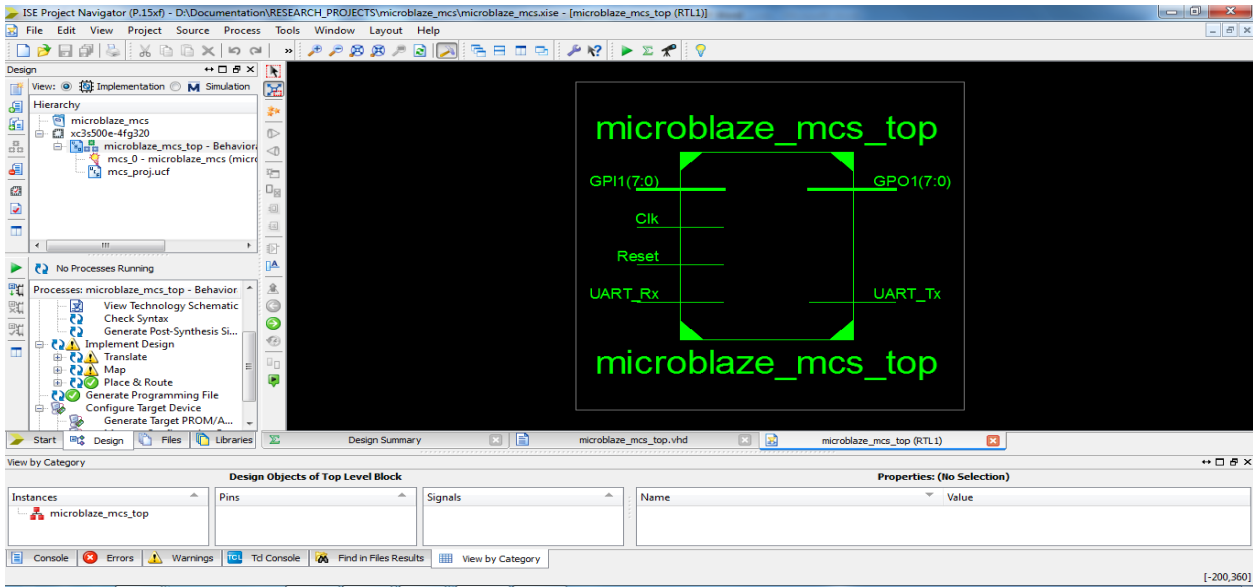


Fig.3. Register Transfer Level (RTL) schematic obtained by Xilinx ISE project Navigator

Fig. 3 depicts the Register Transfer Level (RTL) schematic of the top module ‘microblaze_mcs_top’. The level of Soft IP Core hierarchy is given along with the flow of Xilinx ISE Design. The user constraint file (.ucf) named as ‘mcs_proj’ was created to synchronize required FPGA I / O lines. The Fig. 4 demonstrates the component named ‘microblaze_mcs’ which is further interconnected to the entity named as ‘microblaze_mcs_top’. It explores a clock input ‘Clk’, ‘Reset’ input and an input vector named ‘GPI (7:0)’ is of eight bit. Another input port named as ‘UART_Rx’ is shown which is used for performing UART operation, and receiving the serial bits. To transmit the serial bits an output port 'UART Tx' is used. LEDs available on the Nexys2 Spartan 3E board were given the 8 lines of top level module which are implied as GPO (7:0) .

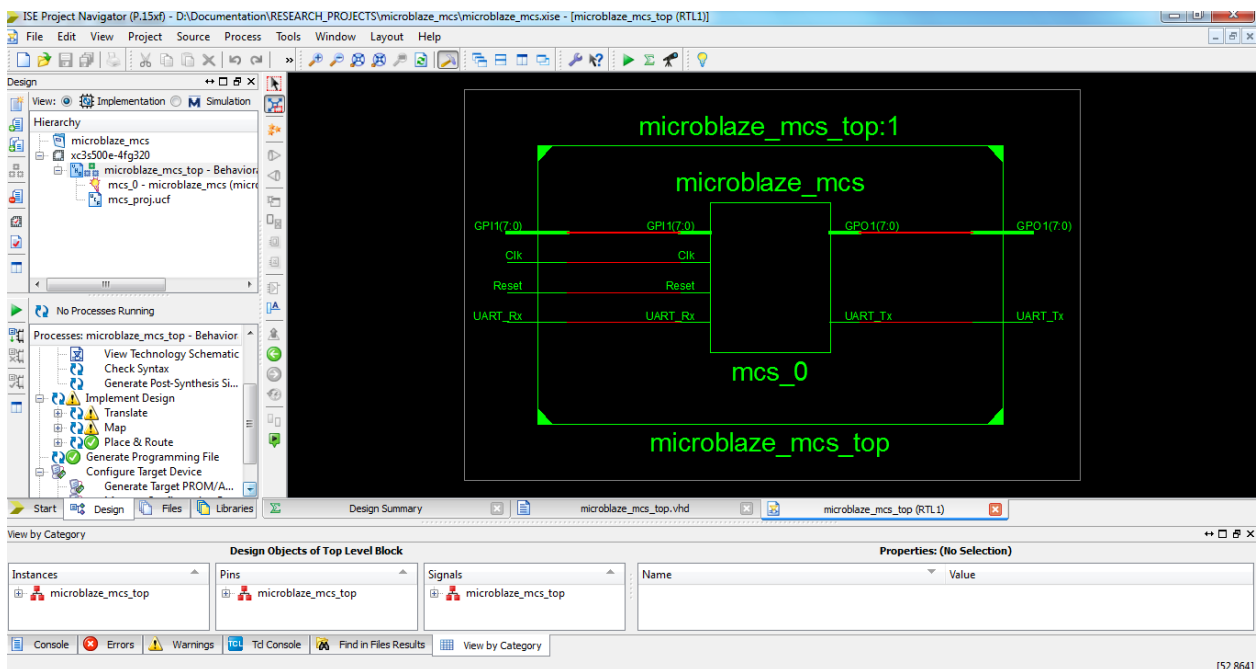


Fig.4. Illustration of Component Interconnection of the Top Level Entity

The project work deals with monitoring the status of input switches present on the FPGA Board. When the position of slide switches changes then the status of the LEDs on the board also changes with respective switch and simultaneously the message is displayed on the HyperTerminal as shown in Fig.5.

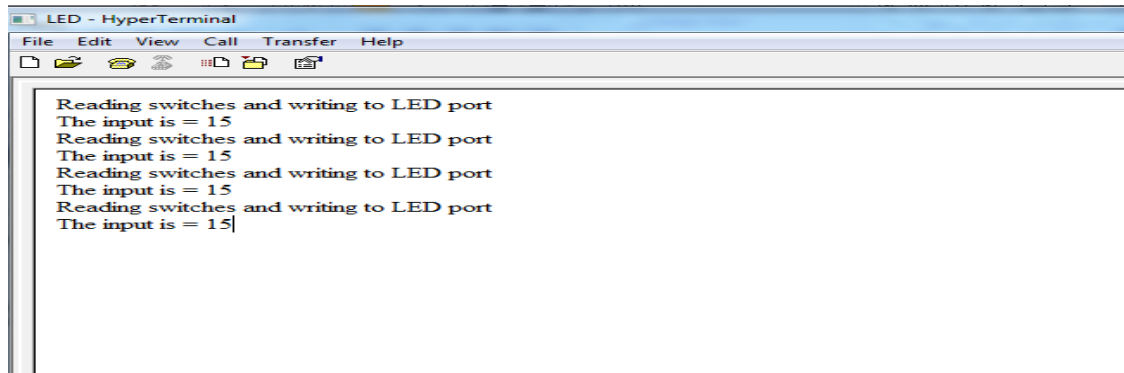


Fig.5. Hyper Terminal window

IV. CONCLUSION

The research paper uses Xilinx Core Generator to design MicroBlaze processor based UART. The 8 bit input is associated with position of slide switches on the FPGA Board. The same concept can be used to conduct serial communication between FPGA devices and other system. The setup can be used to detect and monitor various physical parameters at Farm Sight, laboratory, industrial plants, and so on.

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