

An Fault Tolerance Hamming Technique for SOC with Efficient Network on Chip Architecture Using Optimized Algorithm

M.Sangeetha¹, G.S.Saranya², G.Vennila³, M.Varshini⁴, R.Poovendran⁵

U.G. Students, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India ¹²³⁴

Associate Professor, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India ⁵

ABSTRACT: The maximum bit rate error correction code (MBRBECC) is capable of correcting any type of errors including random and burst errors. This system uses SEC-DED extended hamming code (39,32) to encode and decode the message bits. Here we use triplication error correction algorithm, where each of the encoded message bits is triplicated. The interconnection error is easily identified while encoding and the error is decoded within the process. Thus if the initial SEC-DED extended Hamming code is (n,l), where n is the encoded message and l is the original message, then the last number of bits in the triplication message is 3n. The triplication of the message bit is used to correct the errors and simultaneously avoids interconnection errors. Here, the MpSoC helps to send multiple bits during encoding. The throughput and the presentation of multiprocessor frameworks on chips (MPSoCs) are reliant on the speed of information Network on Chip over the worldwide interconnects.

KEYWORDS: MBRBECC, Hamming code, Triplication error, SEC-DED, MpSoC, NoC

I. INTRODUCTION

With the compressed feature size and expanding die size, mix of enormous number of useful functional blocks, storage components and Intellectual Property(IP) in a single chip increments. As the quantity of functional blocks in a single chip expands, the bus based correspondence gets wasteful in a System-on-Chip (SoC)[1]. Network-on-Chip(NoC) is a worldview that gives answer for the correspondence issue in a SoC. In NoC, the functional blocks convey through routers are interconnected utilizing interconnection wires. In Nano scale innovation, because of scaling of supply voltage, expanding interconnect thickness and quicker clock rates, on chip interconnect wires experience the ill effects of three significant issues. They are: (I) delay; (ii) power utilization; and (iii) unwavering quality. The issue is because of high capacitive coupling and is called capacitive interconnect. While the entryway delay lessens with scaling, the worldwide interconnection wire postpone increments. Because of high parasitic capacitance and coupling capacitance, power utilization is expanded.

Low force coding strategies have been proposed to decrease the force utilization of the interconnection wire by lessening the exchanging action in the interconnection wires. Interconnect avoidance codes (IACs) are proposed to lessen the delay problem. Right now, address the deferral and unwavering quality issue of NoC interconnect connect, we propose joined irregular and torrent mistake amendment code with interconnect evasion.

The proposed code Power scattering has become a basic plan paradigm in most framework structures, particularly in versatile battery-driven applications. Besides, with the expanding drive towards System on Chip (SOC) applications, power has become a significant parameter that should be upgraded alongside speed and region[2]. Hamming code uses triplication algorithm which triplicates the incoming message bits during encoding and The works proposed use DAP coding scheme and correct only one, two or three bits errors with interconnect avoidance. But, the work proposed in this paper corrects any error pattern up to five including

combination of random and burst errors and simultaneously avoiding interconnect between interconnect wires. This is the first error correction code proposed with interconnect avoidance to correct any error pattern up to five for on chip interconnect link. The proposed error control code is named as Multi Bit Random and Burst Error Correction code with interconnect avoidance (MBRBEC). In addition, around 20–36% of the complete framework power is exhaust by interconnection arrange in numerous NoCs. The syndrome is calculated within the process during the triplication takes place. The fast and vitality effective handsets for worldwide interconnects of system on chips (NoCs) has become a functioning field of research throughout the most recent decade. The throughput and the presentation of multiprocessor frameworks on chips (MPSoCs) are reliant on the speed of information Network on Chip over the worldwide interconnects.

II. RELATED WORKS

A. *Low-Power, High-Speed Transceivers for Network-on-Chip Network on Chip*

Network on chips (NoCs) are getting mainstream as they give an answer for the interconnection issues on enormous coordinated circuits (ICs). Be that as it may, even in a NoC, interface force can turn out to be inadmissibly high and information rates are constrained when regular information handsets are utilized. Right now, present a low-power, rapid source-synchronous connection handset which empowers a consider 3.3 decrease interface power together with a 80% expansion in information rate[3]. A low-swing capacitive pre-accentuation transmitter in mix with a twofold tail sense-intensifier empower speeds more than 9 Gb/s over a 2 mm contorted differential interconnect, while devouring just 130 fJ/progress without the requirement for an extra stockpile. Various handsets can be associated consecutive to make a source-synchronous handset chain with a wave-pipelined clock, working with balance unwavering quality at 5 Gb/s.

B. *On-Chip Interconnection transceivers.*

This paper, an interconnect pay conspire for rapid single-finished on-chip flagging is exhibited. To lessen the impact of interconnect in transfer speed improved channel utilizing capacitive determined interconnect, an interconnect feed-forward equalizer is proposed, which makes up for the low-pass nature of the interconnect. The proposed plan is confirmed utilizing a three-channel 10 mm on-chip interconnect executed in 130 nm CMOS process.

III. EXISTING METHOD

In Existing work, the XY routing is utilized to delegate deterministic plan since its straight forwardness and prevalence[4]. XY steering is an insignificant way directing calculation and to stay away from halt and livelock in the system. The deterministic steering, the source and goal address are given and the directing way is fixed once. Yet, in the versatile directing mode different steering way exist in light of the fact that versatile steering offers bundles greater adaptability in picking their steering paths. To take care of the issue, this might be brought about by bundles sitting tight for one another in a cycle.

Check bits	Max Data bits	Max Total size
3	1	4
4	4	8
5	11	16
6	26	32
7	57	64
8	120	128

Table 1 shows the check bit, data bit and the error correction bits within it. If they're not equal, the x-coordinate of destination is initially compared to the x-coordinate of current router. When x-coordinate of current router is less than x-coordinate of destination router, the data packets will be transmitted to the East direction, when x-coordinate of current router is greater than x-coordinate of destination router, then packets will be routed to West direction. The figure 1 explains the FIFO multi architecture where the input and the output is calculated within the single row in accordance with the clock pulse. Then check if the info packet is already on the destination column or not. If this last condition is true, the vertical address of destination is compared to the vertical address of current router. Data packets will be traversed to South direction when vertical address of current router is less than vertical address of destination router, to North when vertical address of current router is greater than destination router[5].

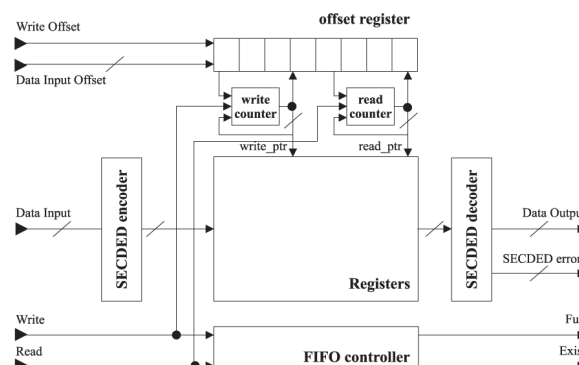


Figure 1: FIFO Block diagram

IV. PROPOSED METHOD

The proposed for joined mistake shirking and blunder remedy code, have concentrated distinctly to address error of most extreme three bits as it were. The works proposed use DAP coding plan and address just one, a few bits mistakes with crosstalk shirking. In any case, the work proposed right now any mistake design up to five including blend of irregular and burst error and at the same time keeping away from crosstalk between interconnect wires. This is the main blunder revision code proposed with crosstalk shirking to address any mistake design up to five for on chip interconnect interface. The proposed mistake control code is named as Multi Bit Random and Burst Error Correction code with correction evasion (MBRBEC).

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The figure 2 explains the SEC-DED process with the help of encoding and decoding. First the bits are encoded and triplication occurs within the encoding thus the syndrome is calculated. Later, the bits are decoded while the error is found. Codes that right error are basic to present day human advancement and are utilized in gadgets from modems to planetary satellites. The hypothesis is experienced, troublesome, and numerically arranged, with a huge number of insightful papers and books, yet this undertaking will depict just a basic and rich code[6].

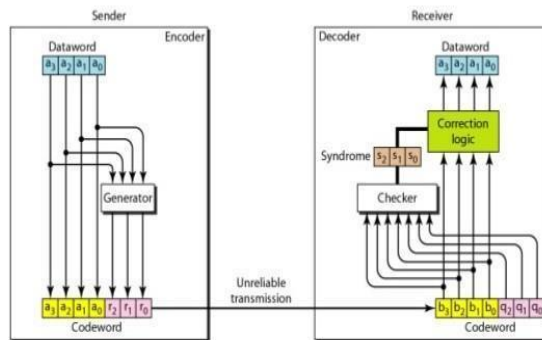


Figure2 Block diagram of SEC-DEC

Codes that right error are basic to present day human advancement and are utilized in gadgets from modems to planetary satellites. The hypothesis is experienced, troublesome, and numerically arranged, with a huge number of insightful papers and books, yet this undertaking will depict just a basic and rich code. An equality bit is an additional 0 or 1 connected to a byte (or bigger square of information) to help distinguish if a mistake has happened. For instance, with even equality, every byte together with its equality bit will contain a considerably number of 1s. On the off chance that the byte itself contains an odd number of 1s, at that point the equality bit is set to 1, to make the all out number even. In any case the equality bit is set to 0. Clearly, if any of the bits gets flipped, the quantity of 1s will be odd and we can confirm that the byte contains a blunder.

Bit position		1	2	3	4	5	6	7	
Encoded data bits		p1	p2	d1	p3	d2	d3	d4	
Parity bit coverage	p1	X		X		X		X	...
	p2		X	X			X	X	
	p3				X	X	X	X	

Table II The encoded parity bits

The table II shows the position of the parity bit determines the sequence of bits that it alternately checks and skips.

There are a few issues with equality bits[7]. In the first place, if numerous mistakes happen inside a similar byte, our equality check probably won't restore a blunder. Additionally, all the equality bits can do is check if a mistake has happened. It has no real way to figure out which bit is off base, so it is difficult to address the mistake. Paradoxically, Hamming codes are error amending codes. Hamming codes can recognize and address single-piece error or can distinguish (yet not right) up to two concurrent piece mistakes. Hamming codes require $O(\lg(n))$ equality bits for n information bits[8].

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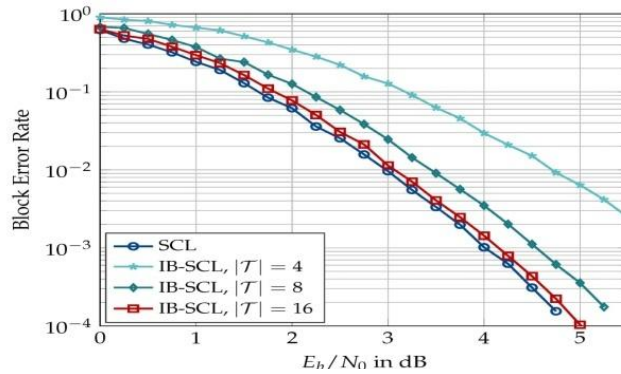


Figure 3 Comparison of XY and Hamming code

Every equality bit checks a few (however not the entirety) of the information bits. In the event that a error happens in an information bit, all the equality bits that watched that information bit will show the mistake, permitting us to extraordinarily figure out where the blunder happened. A parity bit is an extra 0 or 1 attached to a byte (or larger block of data) to help detect if an error has occurred.

Position	1	2	3	4	5	6	7	8	9	10	11
Binary	1	10	11	100	101	110	111	1000	1001	1010	1011
Word	1	1	1	0	1	0	1	0	1	0	1
Check:1	1		1		1		1		1		1
Check:2		1	1			0	1			0	1
Check:4				0	1	0	1				
Check:8								0	1	0	1

Table III Implementation of Hamming code for data bits **1101101**.

The table 3 shows the implementation of hamming code for data bits. In even parity, each byte together with its parity bit will contain an even number of 1s. The figure 3 shows the comparison of XY and Routing If the byte itself contains an odd number of 1s, then the parity bit is set to 1, to make the total number even[9]. Otherwise the parity bit is set to 0. Obviously any one of the bits gets flipped the number. The Figure 4 shows the maximum delay, LUT and INIT within the process.

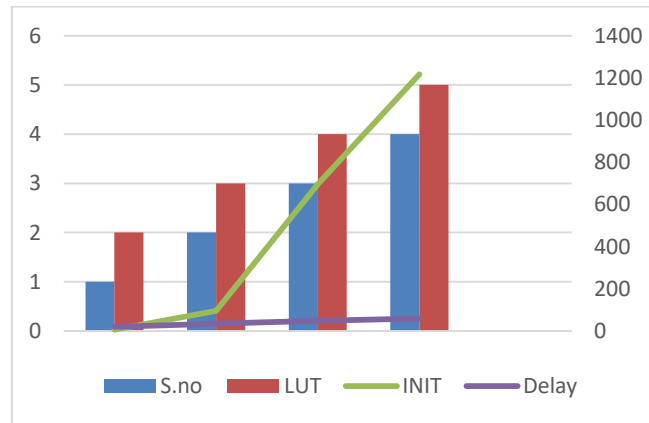


Figure 4 Flow graph of LUT

V. EXPERIMENTAL RESULTS

The Incoming bits have been triplicated during the encoding, then the syndrome of the bits have been calculated and then the bits are decoded. Later the error will be detected where the interconnection error been declared in NoC.

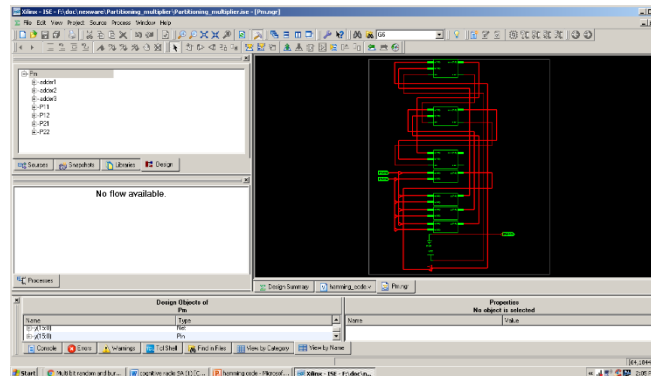


Figure 5 RTL view for network configuration

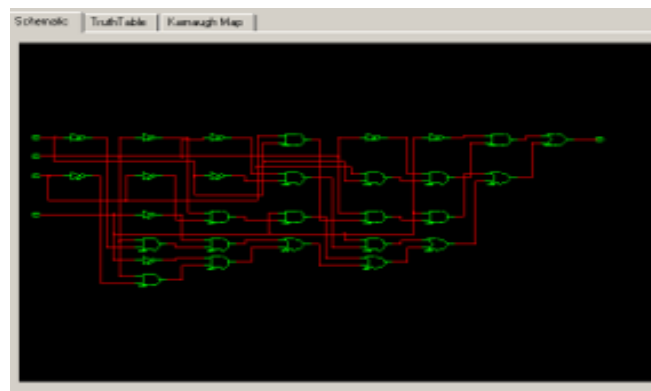


Figure 6 Inner view of hamming encoder

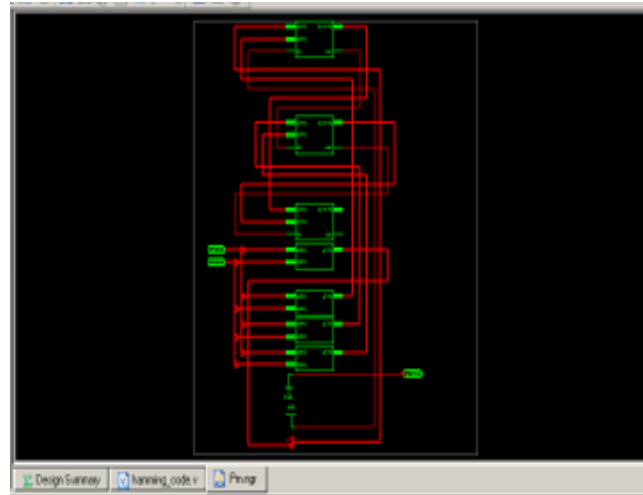


Figure 7 RTL view of Topology Generation

VI. CONCLUSION

The proposed MBRBEC encoder utilizes SEC–DED broadened Hamming code (39,32) to encode the underlying message bits. Triplication blunder rectification conspire is one of the standard mistake redress plans utilized in NoC framework to address error. Propose triplication mistake adjustment plan to address the error in on chip interconnection interface. Utilizing triplication blunder redress conspire, every one of the encoded message bit is triplicated. Along these lines if the underlying SEC–DED broadened Hamming code is (n,l), where n is the encoded message and l is the first message, at that point the last number of bits in the triplication message is 3n[10]. The triplication of the message bit is utilized to address the mistakes and all the while stays away from interconnection. The future work will be to identify the blunder has twofold triplication and mistake redress process as decided. Simultaneously procedure to scramble with code as an encoder and decoder in the hamming code.

REFERENCES

- [1] "Efficient fault detection Dyad routing algorithm for 3D Networkonchip".B.Kavithra,Prof.Dr.R.Poovendran, 2016.
- [2] R.Poovendran, S.Sumathi. "An Area-efficient low-power SCM topology for high performance NoC architecture using an optimized routing design". Concurrency and computation: practice and experience – WILEY. ISSN 1532-0634, volume 30,Issue 18, pp 1-9,(2018).
- [3] R.Poovendran , S.Sumathi. "An Area- efficient FPGA implementation of NOC Router Architecture for optimized Multicore SOC communication ".Sensors Letters American Scientific Publishers. EISSN:1546-1971,volume no:16,pp 1-9,(2018).
- [4] Poovendran.RandS.Sumathi"An Low-Power AreaEfficient Routing Analysis and Optimization for a Fat TreeBased Optical Network-On-chip(Network-on-Chip) Architectures", Sensor Letters- American Scientific Publishers", vol.16, Issue 11, page 862-876, March 2018.
- [5] Poovendran R, Muniraj S, Nandakumar A 'On Chip Implementation of Packet Switched Network' IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 9, Issue 2, Ver. V (Mar - Apr. 2014), PP 38-42
- [6] S. Hoppner et al., "An energy efficient multi-gbit/s NoC transceiver architecture with combined AC/DC drivers and stoppable clocking in 65 nm and 28 nm CMOS," IEEE J. Solid-State Circuits, vol. 50, no. 3, pp. 749–762, Mar. 2015.
- [7] M. P. Flynn, and S.park "A 9-Gbit/s serial transceiver for on-chip global signaling over SEC DEDtransmission lines," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 8, pp. 1807–1817, Aug. 2009.
- [8] Cho.s, and W.Lee, "A 2.5-Gb/s on-chip interconnect transceiver with crosstalk and hamming code," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 124–136, Jan. 2012.
- [9] .W. Luo and D. Xiang, "An efficient adaptive deadlock-free routing algorithm for torus networks," IEEE Trans. Parallel Distrib. Syst., vol. 23, no. 5, May 2013.
- [10] T.Watanabe, Zin Jiang" A novel fully adaptive fault tolerant routing algorithm for 3D NOC"IEEE TENCON.vol 4,no 54, 2013 Oct.