

Hybrid Adder Pipelined Architecture for FFT

C.V.Thejashwini¹, A.Sumathi²

P.G Student, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India ¹

HOD, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India ²

ABSTRACT: In current inventive technology, latency, area, power are the crucial parameters to outline any kind of algorithm on FPGA. FFT is frequently used fundamental tool in DSP applications. FFT plays a vital role in acquiring the signal characteristics with least use of carrying out parameters. The adder plays an utmost importance. To make the best possible adder design in terms of area and delay, various works have been proposed before. In proposed system we combined different sub adders like CSA, RCA, CLA. This reduces the delay and area, but also increases the speed. Hybrid adder is proposed to represent FFT architecture in place of normal adder. Hybrid adder will act as a complex adder in FFT architecture. Pipeline register is applied to a hybrid adder to increase the speed. FFT with pipelined Hybrid adder is coded in Verilog language. Using Xilinx 14.5i tool with Spartan 6 kit, Simulation can be achieved.

KEYWORDS: FFT, Radix-2, RCA, CSA, CLA.

I.INTRODUCTION

Currently, FFT has got the great prominence in the fields of biomedical applications and communication to analyse the signal features. The conversion of original domain in to a frequency domain signal called FFT, which performs frequency analysis on Discrete Time signal. To design FFT processor, power, area and delay are the crucial parameters. To make full use of hardware resources, algorithm of FFT is exposed. The computers and calculators are used by the engineers, scientists and accountants to solve complex arithmetic problems and also to save the effort along with time. FFT/IFFT is one of the important used blocks used in OFDM/OFDMA system. This FFT algorithm plays a crucial role in the communication field and also signal processing which is involved in Frequency Division Multiplexing signal. Adders, multiplier and subtractors are present in FFT block. FFT is one of the most widely used algorithms for calculating the discrete Fourier transform owing to its efficiency in reducing computation time.

The following equation shows the length-N forward DFT $x(n)$ sequence:

$$X[k] = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} \quad (1)$$

Where $K=0, 1 \dots N-1$

$$x(n) = (1/N) \sum_{k=0}^{N-1} X[k]e^{j2\pi nk/N} \quad (2)$$

Where $n=0, 1 \dots N-1$

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

II. RADIX-2 ALGORITHM

Cooley and Tukey presented the first FFT algorithm, which is Radix-2 algorithm. The DFT of a given sequence $X[n]$ can be evaluated using the formula.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, \quad k=0,1,\dots,N-1 \quad (1)$$

Where twiddle factor is denoted as W_N .

$$\begin{aligned} x_1(r) &= x(2m) \\ x_2(r) &= x(2m + 1); \quad m = 0,1,\dots,(N/2) - 1 \end{aligned} \quad (2)$$

Then, the N -point DFT becomes,

$$\begin{aligned} X(K) &= \sum_{n(\text{even})=0}^{N-1} x(n) W_N^{nk} + \sum_{n(\text{odd})=0}^{N-1} x(n) W_N^{nk} \\ &= \sum_{m=0}^{(N/2)-1} x_1(2m) W_N^{nk} + W_N^{nk} \sum_{m=0}^{(N/2)-1} x_2(2m + 1) W_N^{2mk} \end{aligned} \quad (3)$$

Properties of twiddle factors are used. They are symmetry and periodicity.

$$\begin{aligned} X(k) &= X_1(k) + W_N^k X_2(k) \\ X(k+N/2) &= X_1(k) - W_N^k X_2(k) \end{aligned} \quad (4)$$

Where, $k = 0,1,\dots,N/2 - 1$.



Figure 1: Butterfly Unit

III. BASIC CONCEPTION OF ADDERS

The building block of ALU is adder. Adders are generally found in microprocessor design. Increase in speed of adder will enhance the microprocessor performance.

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

A. RIPPLE CARRY ADDER

RCA are easily understood and more compact digital adders to generate carry and sum. Full adders are building blocks of RCA. RCA propagates the carry from LSB to MSB. This may not happen to all the input conditions we give, but there do exist some input combinations where a carry i.e. coming from the LSB stage may have to ripple through all the different stages and have to go to the final stage to generate sum and carry. This RCA is easy but delay is more because it should wait for the each bit of carry that is calculated by the existing adder.

This diagram represents that 4 bit binary adder is implemented by cascading four 1 bit full adder. This $C_{in}, (A_1, B_1)$ will change S_1 and S_2 . When S_2 comes, A_2 and B_2 along with C_2 results in S_2 and S_3 . There is something called rippling of carry. The carry that is generated from C_{in} may go and change the values of S_1 and C_2 . C_2 may go and change the values of S_2 and C_3 , which intern may change the value of S_3 and C_4 and so on. The carry that is generated in right most stage may ripple through the rest of the circuits and may result in a change of C_4 . The delay we get from the circuit is quite long. Critical path is also known as longest path.

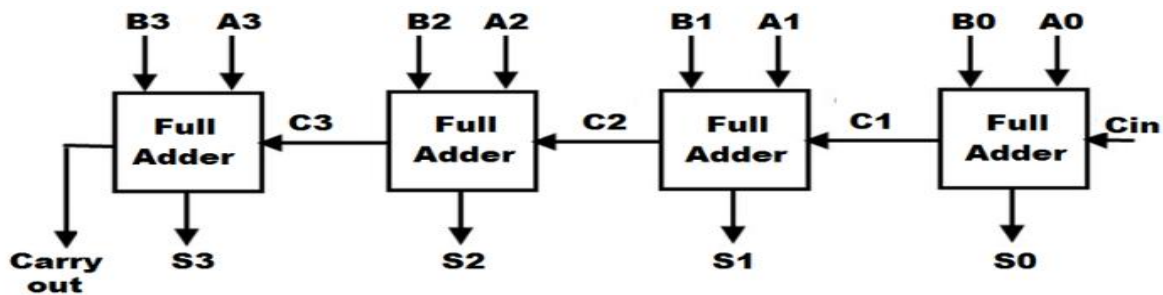


Figure 2: 4 bit RCA

B. CARRY LOOK AHEAD ADDER

CLA is a fast adder using digital logic to calculate the carry signal in advance from the input signal. In CLA, carry does not wait. Depending on input signal, carry generates the input. Due to this, delay is reduced. The look ahead generation fastens addition operation by eliminating ripple carry adder. In binary adder, each stage depends upon the carry generated by previous stage. It creates a lot of delays when we want to add two large binary number. So, in CLA, carry is generated based on input signals, due to this delay is reduced.

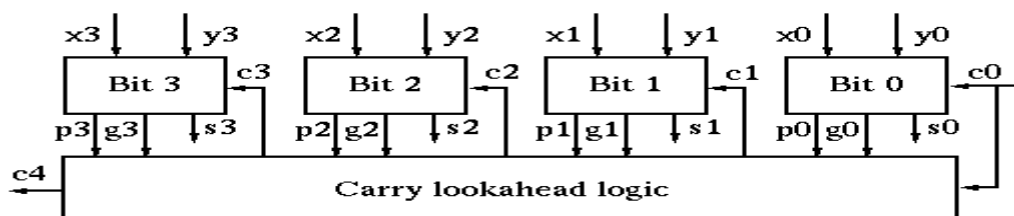


Figure 3: 4 bit CLA

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

C. CARRY SAVE ADDER

CSA is similar to full adder, but architecture is different. CSA has 3 inputs and process 2 outputs. The operation and principle of CSA is based on formulae.

$$A+B+C=2D+E$$

Essentially it takes 3 inputs which are three numbers, produces D and E as output. D is carry bit and S is the sum bit. CSA also called Wallace tree multiplier. It will go much faster than RCA. Both RCA and CSA have similar qualities. CSA bits will work in parallel manner. The carry does not propagate all the way, instead it is saved for future. So, CSA works faster than any adder

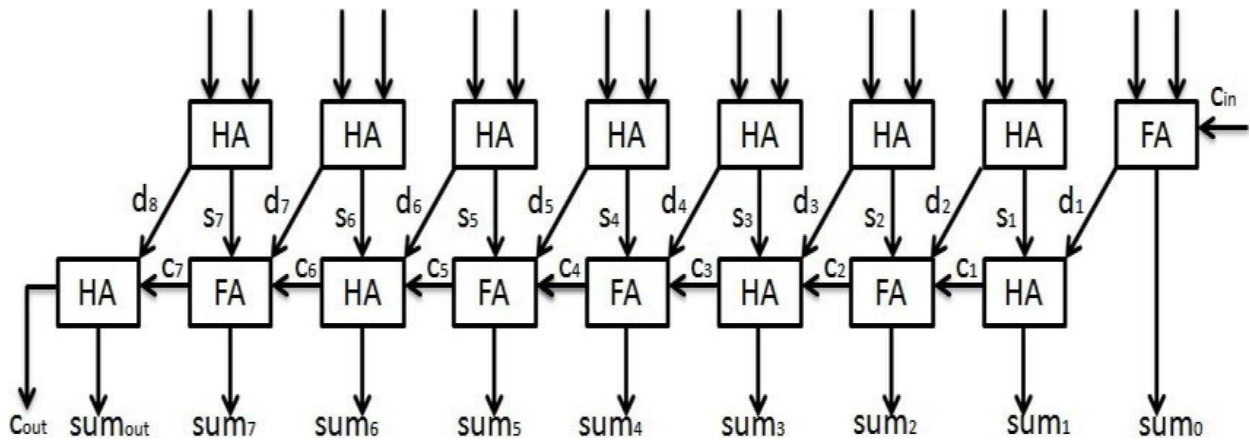


Figure 4: 8 bit CSA

IV. PROPOSED SYSTEM

A. FFT WITH HYBRID ADDER

Butterfly diagram of Radix-2 FFT is presented in Figure (5). Butterfly diagram is shown for first stage of 8 point of FFT. $y(0)$, $y(1)$ are inputs. $Y(0)$, $Y(1)$ are outputs of FFT.

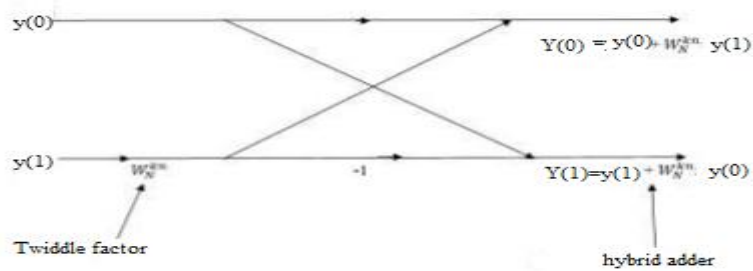


Figure 5: Radix-2 FFT butterfly diagram

This diagram represents Radix-2 FFT using Hybrid adder. This block contains compliment unit, hybrid adder, and multiplier.

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

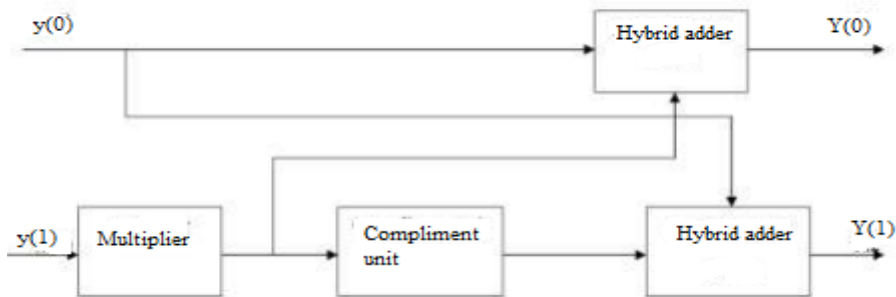


Figure 6: Block Diagram for Radix-2 FFT using Hybrid adder

B. PROPOSED HYBRID ADDER

In FFT, both complex addition and complex multiplication are included. The ideal way to enhance the rapidity of FFT is by using less delay adder in place of normal adders. The different adders are joined together to form a hybrid adder. So, the delay can be reduced with the selection of adders. Here, 16 bit hybrid adder is used, which is the combination of different adders. They are 4 bit CLA, 4 bit RCA, 8 bit CSA. Once we obtain results for FFT, we can insert pipeline registers to improve speed.

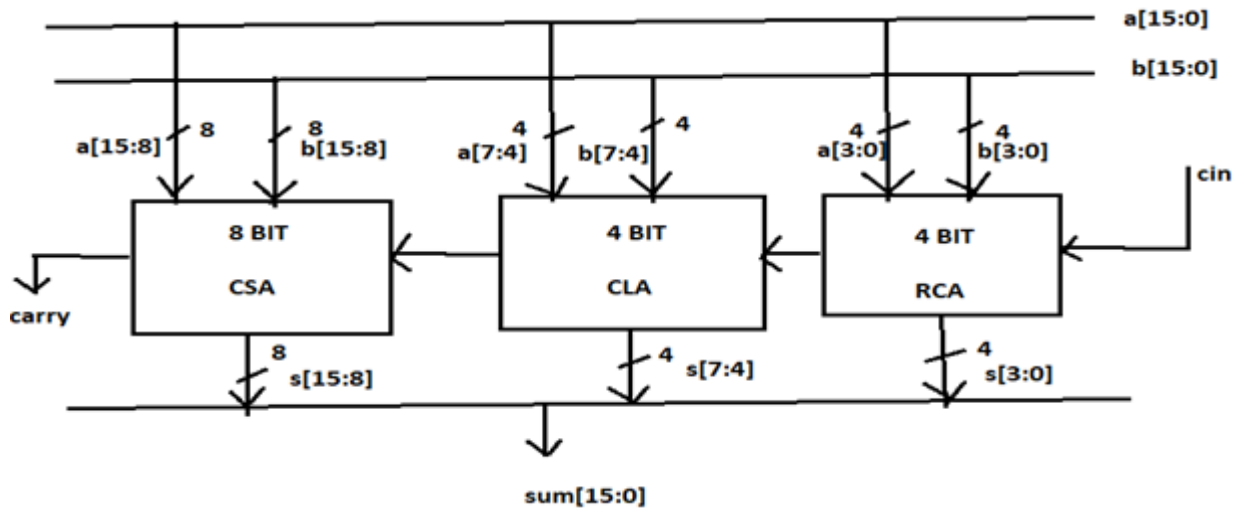


Figure 7: Proposed hybrid adder

C. PIPELINED HYBRID ADDER

To enhance high throughput of the system and for better performance, pipelining technique is used. Pipelining is done by breaking down the path into several sub paths. Between sub paths, pipelined registers are inserted to improve speed. The objective is to increase throughput and to achieve low latency and cost.

The following definitions are necessary to understand pipelining

1. Throughput = (no. of usable outputs) / (unit time)
2. Latency = Time delay from valid inputs provided until outputs valid.
3. Cost = Area + Power.

Pipelined registers are applied to a hybrid adder circuit.

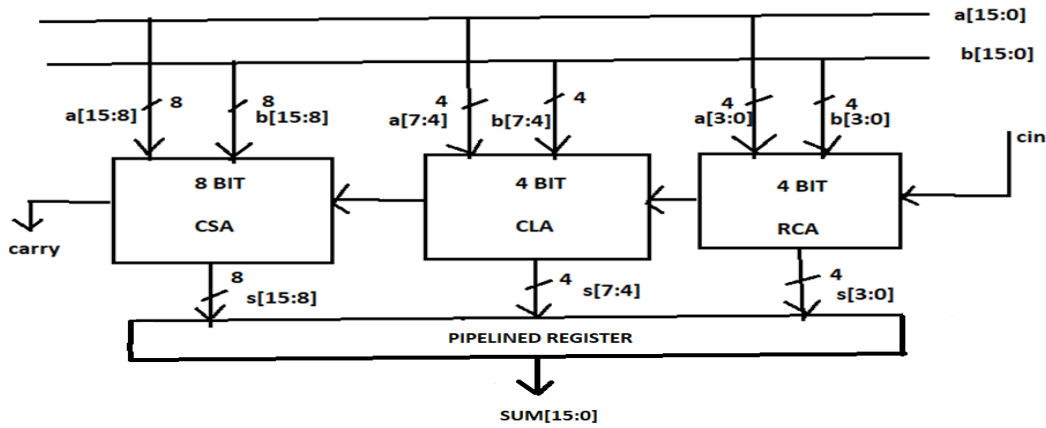


Figure 8: Pipelined Hybrid adder.

V. RESULTS

A. RTL SCHEMATIC VIEW FOR PIPELINED HYBRID ADDER

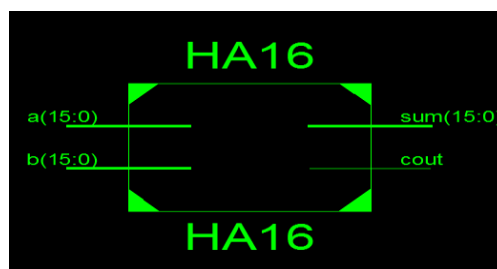


Figure 9: RTL schematic view for pipelined hybrid adder.

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

B. TECHNOLOGY SCHEMATIC VIEW FOR PIPELINED HYBRID ADDER

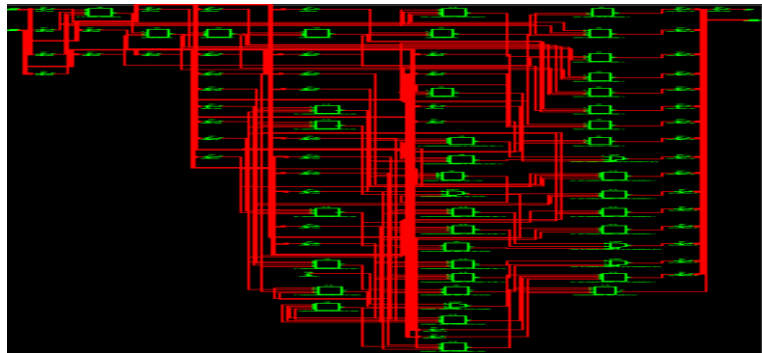


Figure 10: Technology schematic view for pipelined hybrid adder

C. SIMULATION FOR HYBRID ADDER

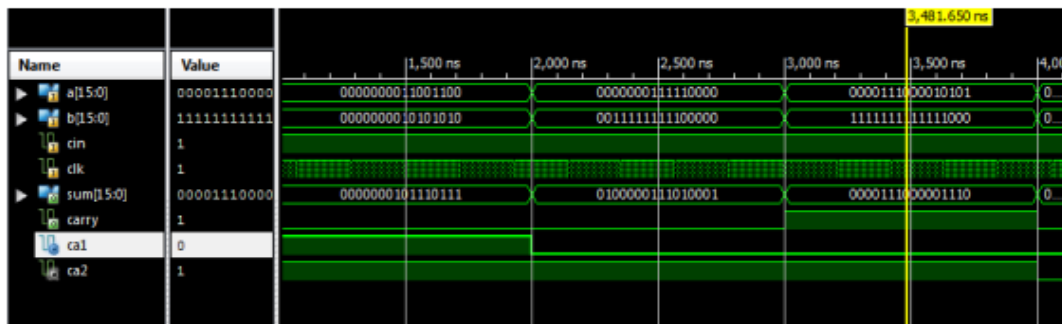


Figure 11: Simulation for Hybrid Adder

D. SIMULATION FOR PIPELINED HYBRID ADDER

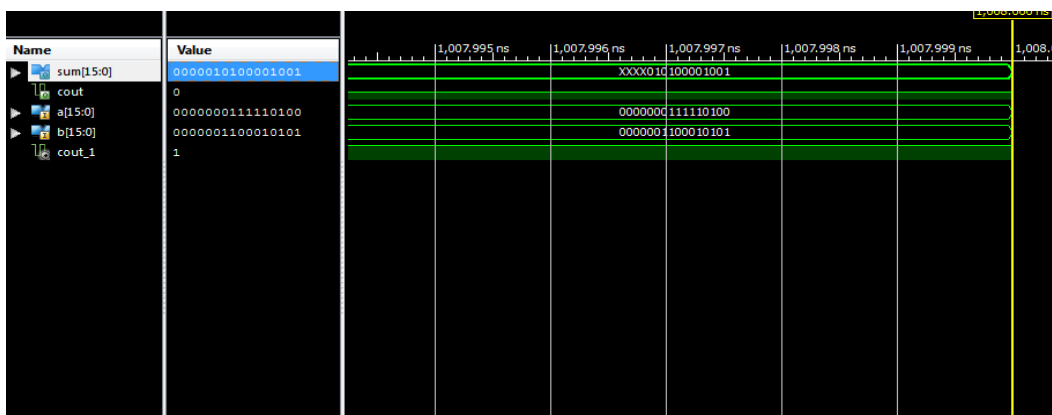


Figure 12: Simulation for pipelined Hybrid Adder

Organized by

Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

E. ADDER COMPARISON

ADDER TYPE	RESOLUTION	NO.OF.LUTs	NO.OF.OCCUPIED SLICES	DELAY(ns)
CARRY SELECT ADDER	16 BIT	48	35	12.440
PROPOSED HYBRID ADDER	16 BIT	42	30	10.856
PIPELINED HYBRID ADDER	16 BIT	39	24	8.397

Table 1: Comparison of Different Adders

VI.CONCLUSION

In this paper, FPGA implementation of FFT using hybrid adder is proposed. The delay of pipelined hybrid adder is less than normal adder. The area performance of Pipelined Hybrid adder is improved when compared with CSLA. FFT with Pipelined hybrid adder is coded in Verilog. Using Xilinx 14.5i with Spartan 6 kit, Simulation can be achieved.

VII. FUTURE SCOPE

The proposed block is designed for 16 bit inputs. It can be further extended for 32 bit, 64 bit, 128 bit inputs. Even other design can be tried for even better analysis. In fact by combining adders including technology, used to implement a suitable less delay can be achieved.

REFERENCES

- [1] Kavitha M.V, S,Ranjiyha, Dr. S.G.Hiremath, Dr.Suresh H.N,"A Novel RTL Architecture for FPGA Implementation of 32-point FFT for High Speed Applications" IOSR-JCE,ISSN:2278-0661, Volume 19, Issue 2, Ver.II(Mar 2017).
- [2] J.Manikandan, M.Manikandan "VLSI based pipelined Architecture for Radix-8 combined SDF-SDC FFT" IJST, ISSN: 0974-5645, Vol. 9(28), July 2016.
- [3] Magandeep Kaur, Pragati Kapoor,"Analysis of r² SDF pipeline FFT architecture in VLSI" IJESAT, ISSN: 2250-3676, Vol. 2, Issue-3,555-560.
- [4] Deepika Hiremath, B.Rajeshwari, "Implementation of pipelined Radix-2 FFT using SDC-SDF architecture", 10 conference, Nov-2016.
- [5] Allred D.J, H.Yoo,Krishnan" For high throughput distributed arithmetic based LMS adaptive filters" IEEE Transactions on circuit systems", Jul.2005, Volume 52, Page no: 1327-1337.
- [6] Jasbir Kaur, Lalit sood" Comparison between various Types of Adder topologies", IJCST, ISSN: 0976-8491, Vol. 6, Issue 1, and Jan 2015.
- [7] V.N.Sreeramulu"Prefix tree structure for low power and High speed", IJSETR, ISSN: 2278-7798, Vol. 4, Issue 9, Sep 2015.
- [8] K.Venkata subba reddy ,"Implementation of 64 point FFT/IFFT by using Radix-8 algorithm", IJEETC, ISSN: 2319-2518, Vol. 2, No. 4, Oct 2013.