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Implementation of 1024-Point FFT Processor with Reduced Hardware Architecture

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ABSTRACT: Radix- 2^k delay feed-back and radix-K delay commutator are the most well-known pipeline architecture for FFT design. The radix- 2^k fast Fourier transform (FFT) algorithm is used to reduce the number of twiddle factor multiplication. 1024-point FFT processor with two parallel data paths is implemented in 65nm CMOS process technology. The FFT processor occupies an area of 3.6 mm^2 , successfully operates in the supply voltage range from 0.4–1 V and the maximum clock frequency of 600 MHz. 1024-point FFT processor with two parallel data paths is implemented parallel path technique in 65nm CMOS process technology. The FFT processor occupies an area of 3.6 mm^2 , successfully operates in the supply voltage range from 0.4–1 V and the maximum clock frequency of 600 MHz. Four parallel path FFT architecture utilizing the advantages of the radix-4 algorithm, such as simple butterflies and less memory requirement. The entire FFT algorithms were implemented in Verilog hardware description language and synthesized with Xilinx ISE design suite.

KEYWORDS: Discrete Fourier Transform), butterfly stage, commutator, sample/clock, twiddle factor.

I. INTRODUCTION

The Fourier transform (FT) is a technique to transform a signal from the time domain into the frequency domain to analyze the signal's frequency components. In the frequency domain, the absolute value at each frequency represents its contributing amount to the original signal while the complex value explains the phase offset of the sinusoid at that frequency. By decomposing a time domain signal into a summation of multiple sinusoid signals, FT offers a great conversion tool for processing a signal that is difficult or even impossible to handle in the time domain, which makes it one of the most important algorithms in digital signal processing.

Fast Fourier Transform (FFT) is a commonly used technique for the computation of Discrete Fourier Transform (DFT). DFT computations are required in the fields like filtering, spectral analysis etc. to calculate the frequency spectrum. However, direct computation of Discrete Fourier Transform (DFT) requires on the order of N^2 operations where N is the transform size. FFT is used in digital video broadcasting and OFDM systems. The FFT algorithm, first explained by Cooley and Tukey, opened a new area in digital signal processing by reducing the order of complexity of DFT from N^2 to $N \log_2 N$. There are a number of different 'Fast Fourier Transform' (FFT) algorithms that enable the calculations much faster than a DFT. FFT algorithms used for quick calculation of discrete Fourier transform of a data vector. FFT is used to speed up the DFT, it reduces the computation time required to compute a discrete Fourier transform and improves the performance by factor 100 or more over direct evaluation of DFT.

In Cooley-Tukey radix-2 algorithm, the N point DFT is sub divided into two $(N/2)$ point DFTs and then $(N/2)$ point DFT is recursively divided into smaller DFTs until a two point DFT, whose butterfly is just an addition and a subtraction of input complex numbers. It is the best suitable algorithm for a number N , which is a power of 2. Higher radix algorithms such as radix-4, radix-8, etc can be employed to reduce the complex multiplications but the butterfly structure becomes complex with the multiple input complex adders.

In Single-path pipelined structures are useful for high-speed, real-time applications that have a sequential input/output data. On the other hand, most transforms require global data inter connections, which calls for parallel hardware structures. However, the parallel structures typically use many arithmetic units in hardware, which leads to a large chip area and high power consumption.

In some real-time applications such as OFDM or ultra-wide band (UWB) systems, where high throughput is a requirement, it is important to be able to process the input samples in parallel. Also, it is a challenge to process several samples of an input sequence in parallel when they are received in parallel. Thus, parallel pipelined FFT architectures have become popular in recent times. In this paper, we propose four path-parallel Radix-4 MDC, which is more power efficient than the regular Radix- 2^2 MDC and is suitable for use as an accelerator. Also, it has a simpler butterfly structure and simple control than the corresponding Radix-4 architecture.

II. 1024-POINT RADIX-2² FEED-FORWARD FFT PROCESSOR

Pipeline FFT processor is a specified class of processors for DFT computation utilizing fast FFT algorithms. It is characterized with real-time, non-stopping processing as the data sequence passing the processor. Digital signal processors offer flexibility and, therefore, low development costs but at the expense of limited performance and typically high power dissipation. Field programmable gate arrays (FPGA) combine the flexibility and the speed of application specific integrated circuit (ASIC).

Input data is stored in input buffer and commutated by the control signal such that to provide correct required distance to the butterfly inputs, in processing unit FFT algorithm is used to perform operation on inputs and it uses twiddle values from ROM memory according to the algorithm used, after the completion of operation result is stored in memory.

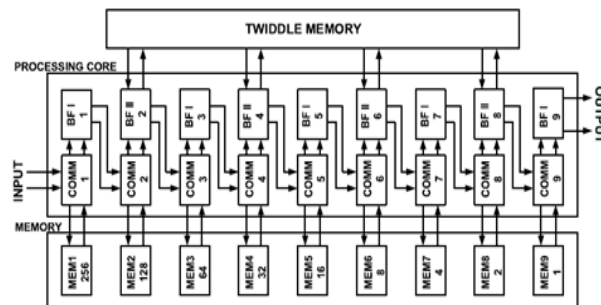


Fig.1: 1024-Point Radix-22 Feed-Forward FFT Architecture with dual path

For two parallel path operation, input data is divided in to two equal half's and are given to inputs, input data values are stored in memory by the commutator, commutator provides the control signal such that to provide correct required distance to the butterfly inputs, for this purpose n-bit counter is used, here we have two butterflies BF I and BF II. Architecture includes nine butterfly stages, in these we have even-numbered BF's and odd-numbered BF's, even-numbered BF's includes adders and subtractors where as odd-numbered BF's includes one more multiplier along with adders and subtractors. BF II Multipliers takes required twiddle factor value from twiddle factor memory, there are four multiplier butterfly stages out of nine processing stages. Size of the multiplier up to fourth stage is 16bit*16bit, then after that size of the multiplier is increased, so in this architecture variable size multipliers are used and also truncation is required as the product increases, truncation is required after the fourth stage such that to store result in registers, truncation is not required in last stage because as there is no multiplication Butterfly stage.

Delay Feedback

FFT stage consists of an adding stage or butterfly (BF) and a twiddle multiplying stage. The inputs of each BF need to be separated by a correct distance ($N/2$ for the 1st stage, $N/4$ for 2nd stage ...), which can be realized by a delay path. Two well-known architectures to implement this requirement are delay feedback and delay commutator. In the delay feedback scheme, outputs from BF are delayed by a predetermined distance to pair with the next coming inputs and then fed back to the BF for next operation cycles. Shift registers store the data in the feedback path as presented in the Single Delay Feedback (SDF) topology [10]. To increase the FFT's throughput, more delay paths can be used as in Multiple Delay Feedback (MDF) [11]. However, it increases the hardware complexity with additional parallel data paths.

Delay Commutator

Instead of feeding back BF's output, the output can be arranged immediately at the commutator using different delay paths with a correct delay distance. Because of the parallel data paths, the throughput of the MDC architecture is higher than that of the delay feedback architecture. However, the MDC architecture shows a lower multiplier utilization rate and requires a larger memory size [13]. Recently, a few research works have investigated Radix-2²MDC for minimizing the hardware cost without throughput degradation except in [14] where an FPGA implementation for $R2^k$ MDC

III. FOUR PARALLEL PATH PROCESSOR ARCHITECTURE

Figure below shows the new four parallel path delay Feed-Forward FFT Architecture, where input data is divided in to four equal size data inputs and they are processed to the butterfly stages in parallel, memory is also divided in to four equal size parts to store four equal size data inputs at a time.

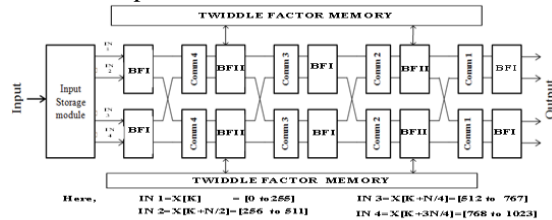


Fig.2: Four Parallel Path Feed-Forward FFT Processor Architecture

here commutator provides the required correct distance to the butterfly operation ,input storage module takes input data and stores in four equal size memory parts and they are given to BF's to perform algorithm operation in parallel. Two types of BF stage's are used, BF I includes adders and sub tractors where as BF II includes one more multiplier along with adders and sub tractors, BF II Multiplier takes required twiddle factor value from twiddle factor memory. Radix- 2^4 based 4-Path Delay Commutator FFT architecture suitable for low power, high throughput applications

IV. RESULT ANALYSIS

Four path FFT Processor achieves the lowest hardware requirements for multipliers and memory size in compared with delay feedback architecture and Radix-K MDC and MDF with combining the benefits of Radix- 2^2 , Radix-4 algorithm and Feed-Forward architecture. Processor has better energy efficiency for mid-high range performance while it has slightly higher energy consumption in ultra low voltage domain (below 0.4 V).

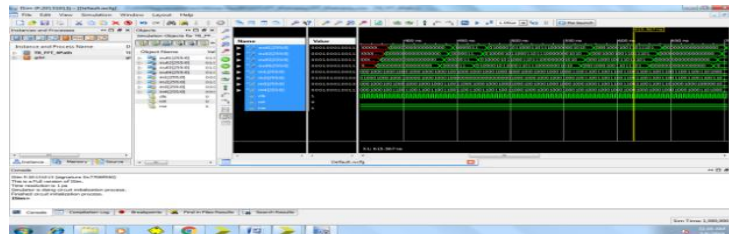


Fig.3: Simulation output of Four Parallel Path FFT processor

V.CONCLUSION

The proposed processor can process the data into four independent data streams simultaneously, and thus by making it is suitable for low power and area efficient real-time applications. High throughput i.e four samples/clock can be obtained with parallel processing with same hardware as used in two parallel path processor. Four parallel path processor provides high throughput, less area requirement, lower power consumption but all are can be obtained with increasing complex control structure and delay. In future we can extend the FFT Processor can be implemented with SRAM design.

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BIOGRAPHY



Telagamalla Gopi Received B-Tech degree from Scientist Institute of Technology Hyderabad, completed M-Tech with VLSI system design from Sree dattha Institute of Engineering and Science. Currently working as Assistant Professor in Annamacharya Institute of Technology and Sciences, hyderabad. Has 8 years of teaching experience. Has published six papers in reputed journals. Areas of interest includes digital signal processing and VLSI.



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