



e-ISSN: 2319-8753 | p-ISSN: 2320-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 9, Issue 9, September 2020

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.512

9940 572 462

6381 907 438

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Implementation of a Hybrid UPQC Topology with an Isolated Bi-directional DC-DC Converter at DC Link

K.Naresh Kumar¹, Ashok Kumar².G, Manikandan.S², Praveen Kumar .M²,
Harkarthick Meiyappan³

Assistant Professor, Department of Electrical and Electronics, R.M.K Engineering College, Tamilnadu, India¹

UG Scholar, Department of Electrical and Electronics, R.M.K Engineering College, Tamilnadu, India²

Project Manager, GE Renewable Energy GE T&D India Limited, Chennai, Tamilnadu, India³

ABSTRACT: This paper introduces an original hybrid unified power quality conditioner (HUPQC) topology as an alternative solution to electrical power quality problems. The proposed HUPQC consists of the shunt hybrid active power filter (SHAPF), the dynamic voltage restorer (DVR) and the isolated bi-directional DC-DC converter (BiDC) located at the common DC link. The SHAPF enables reduction in the voltage rating of the DC link capacitor, helps to reduce the cost and the size of the DC link and hence reduces switching losses of the voltage source inverter (VSI). Besides the novelty of its topology, dynamic reactive power compensation capability is realized for the first time in literature within HUPQC concept by achieving adaptively controlling DC link voltage. The BiDC not only provides isolation and bi-directional power flow between the DVR and the SHAPF but also operates to keep the DC link voltage of DVR constant against adaptively changing DC link voltage of the SHAPF. In addition to these, a new hybrid voltage sag/swell detection algorithm based on the combination of the improved clarke transformation and the enhanced phase-locked loop is developed and introduced. In order to verify the viability and effectiveness of the proposed HUPQC topology, experimental studies are carried out.

KEYWORDS: Power quality, SHAPF, UPQC, Harmonics.

I. INTRODUCTION

Increase in electricity demand makes electrical power quality an important issue. Variations in the amplitude of voltage and current, system frequency deviations and waveform distortions that cause damage to equipment's or consumer loads are defined as power quality problems. Low performance of traditional compensation devices for compensation of power quality problems necessitated the development of advanced technology, power electronics based compensation devices.

In recent years, the number of studies on UPQC has increased and several topologies have been put forward for different purposes. In [3], an exhaustive literature review on various power circuit topologies, control strategies and the latest advances of UPQC is provided. Researchers have explored attractive configurations to improve alternative solutions for power quality problems. The Interline UPQC and the Multiconverter UPQC that VSIs are connected between two or more adjacent distribution feeders are suggested in [4] and [5], respectively. In [6-8], Open UPQC, in which DVR and APF are supplied from separate DC link sources instead of common DC link, is proposed. With the growing interest in the design of UPQC for higher power levels, modular (multicell) [9, 10], multilevel [11] and modular multilevel matrix converter [12] based UPQC topologies are developed. In [13-15], integration of solar photovoltaic arrays into the DC link of the UPQC is addressed with the aim of reducing load demand on supply system. In [1] and [16], implementation of transformer less UPQC is presented for single phase (three leg) and three phase systems, respectively. In [17], a new structure of the UPQC using less number of semiconductor switches is introduced.

Lately discussed two different approaches, HUPQC [18-21] and UPQC with the isolated BiDC [15, 22-24] are brought to the attention. UPQC systems containing hybrid active power filter (HAPF) and DVR in their topology reveals a relatively new concept known as HUPQC and not much work has been reported on it yet. There are only a few theoretical and simulation based studies related to HUPQC. In hybrid UPQC topology, the cost, the size and the losses of inverters are considerably reduced depending on the decrease in the required DC link voltage owing to the use of SHAPF. With the advantage of the SHAPF topology, voltage ratings of the shunt VSI is significantly decreased due to

the series connection of passive filter (PF). PF capacitor holds the fundamental supply voltage across its terminals so that the shunt VSI operates with lower voltage rating at the DC link.

Paper is organized as follows. Section II describes

II. PROPOSED HUPQC SYSTEM

The proposed HUPQC system is designed to operate at 400V line voltage in three-phase three-wire distribution systems according to the theoretical calculations and the data obtained as a result of simulations performed by using PSCAD/EMTDC software. The power circuit configuration of the HUPQC formed from the SHAPF, the DVR and the BiDC is illustrated in Fig. 1. As shown in the figure, the SHAPF and the DVR are connected back to back via the BiDC at the common DC link. The SHAPF consists of precharge resistors (R_p), PF tuned to 350 Hz with the inductor (L_f) and the capacitor C_f , three phase three wire VSI and the DC link capacitor bank (C_{dc2}). The components of the DVR power circuit are three H-Bridge

VSI which are connected in series with busbar through series injection transformers (TR_2 , TR_3 and TR_4), inverter side filter employed to attenuate the switching ripple harmonics and the DC link capacitor bank (C_{dc1}). The BiDC part of the HUPQC is comprised of auxiliary reactors (L_{dc1} and L_{dc2}), two symmetrical single phase H-bridge VSIs and a high frequency transformer (TR_5). The SHAPF side is connected in parallel with nonlinear and sensitive load at the end of the feeder. The nonlinear and sensitive load includes the inductive loads and two pieces of three phase bridge rectifiers that supply RC load.

The supply current, the current passing through the inverter side filter, the load current and the harmonic filtering current are denoted by i_s , i_d , i_L and i_f , respectively. Unlike other known compensation devices, the proposed HUPQC system has superior features on account of performing the functions of voltage sag/swell mitigation, current harmonics elimination and dynamic reactive power compensation with adaptively changing DC link voltage simultaneously. In the proposed HUPQC, the losses are quite low as compared to an ordinary UPQC topology. In a conventional UPQC topology, the switching losses are high depending on the continuous operation of the APF with high DC link voltage.

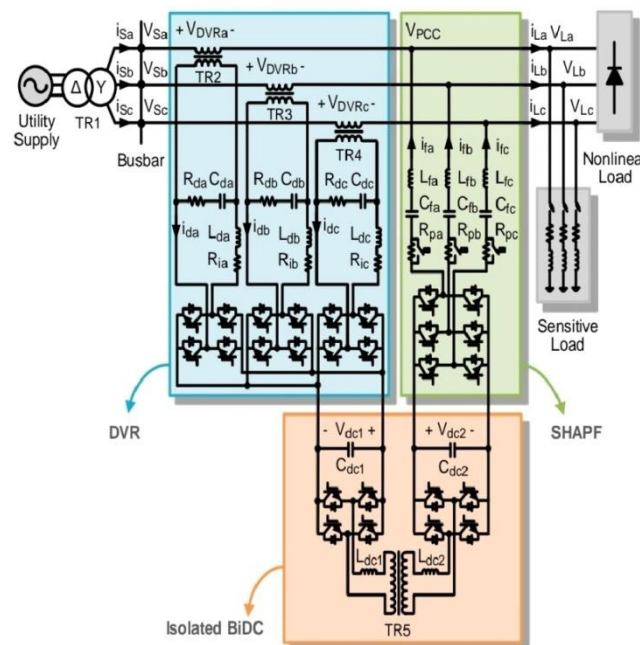


Fig. 1. Power circuit configuration of the proposed HUPQC

On the other hand, the SHAPF in the proposed HUPQC topology has less switching losses due to its operation with reduced DC link voltage under low loading conditions. Furthermore, there is low conduction loss in BiDC as long as voltage sag/swell event does not occur. The conventional SRF method uses the real three phase voltages in the transformation and calculates the averages of them so that it is unable to detect the unbalanced voltage sag/swell accurately. Besides, the conventional SRF method cannot detect a voltage sag/swell lower than a definite depth for

unbalanced conditions. With the use of ICT, the magnitude of each phase can be determined separately instead of the average value of three phase magnitudes as in the conventional SRF method so that the drawback of the conventional SRF method is eliminated.

III. CONTROL STRATEGIES

A. DVR Controller

The control system of the DVR part of the HUPQC includes three controller blocks namely voltage sag/swell detection, reference voltage extraction and gate signal generation. In order to obtain the required injection voltage by the DVR, the measurement of the busbar voltage is performed and processed in the control system as shown in Fig. Voltage sag detection method has a significant impact on the performance of the DVR controller. In order to detect both balanced and unbalanced voltage sag/swells fast and accurately, a hybrid detection method based on the combination of the ICT and the EPLL is proposed. The instantaneous magnitude signal of the distorted busbar voltage in any phase is calculated by taking the average of the magnitude signals obtained from the ICT and the EPLL. The proposed method is simple, reliable and practically applicable for single and three phase systems.

According to the control scheme, the distorted busbar voltage $V_{s,n}(t)$ is firstly converted to per unit (p.u.) value $un(t)$ neurons. Few of the researchers carries investigation in the field of driver drowsiness detection using Artificial Neural Network. People who has fatigue exhibit various visual behavior that are easily observable from the changes in facial expressions. Visual readings reflect a person's degree of fatigue which includes movement of eyelid, gaze, movement of head, and expression of face. By using these visual cues the artificial neural network is made to detect drowsiness of a person. Many test samples have been done and got 90% result.

B. SHAPF Controller

The control algorithm of the SHAPF is formed from three main parts namely harmonic compensation controller, reactive power compensation controller and adaptive DC link voltage controller as shown in Fig. 3. The measurements of the supply current, the load current, the busbar voltage and the DC link capacitor voltage are performed by control algorithms of the SHAPF to generate the required compensation signals.

In order to compensate harmonic currents generated by the load group, supply current detection method based on a feedback control strategy is preferred. The supply current detection method is usually implemented with indirect current. Control (ICC) and has sufficient compensation performance. In this method, SHAPF part of the HUPQC is operated as a current controlled voltage source that acts as high series impedance between the supply and the load to isolate harmonic currents. The series connection of the VSI and the PF seems to be as a disadvantage for the dynamic response of the harmonic compensation. However, the SHAPF presents a considerable harmonic filtering performance with considerably low impedance characteristic of PF in harmonic frequencies and the contribution of the VSI.

C. BiDC Controller

In BiDC controller, simple phase shift (SPS) modulation technique is used to maintain bidirectional power flow between the SHAPF and the DVR sides and to regulate the DVR side DC link voltage against changing SHAPF side DC SPS is one of the most prevalently used modulation technique that provides high power transfer. The main waveforms of the BiDC conducted with SPS control are illustrated in Fig. 4. The primary (DVR side) and secondary (SHAPF side) VSIs are composed by $S1-4$ and $Q1-4$ gate signals which are identical square waves controlled with fixed 50% duty ratio (ignoring the small dead time) [35-37]. There is a phase shift of 180 degrees between the diagonal switching pairs in each VSI to ensure almost square wave AC output voltages ($\pm VHP$ and $\pm VHS$). These two output voltages (VHP and VHS) can be phase shifted to control the power flow between the VSIs in the presence of auxiliary reactors and the leakage inductance of the high frequency transformer.

The phase shift angle, denoted by δ , is a significant parameter specifying the direction and amount of power transfer between the DVR and the SHAPF side DC links. By controlling the phase shift angle δ [rad] between VHP and VHS , the transformer voltage and the current flowing from the transformer ($iHFT$) can be changed and then the power transfer takes place as described. The DVR side DC link voltage value is maintained constant at the desired value with a proper phase shift angle obtained by PI controller against the variations of SHAPF side DC link voltage level. The measured DVR side DC link voltage ($Vdcl$) is subtracted from the reference voltage value ($Vdcl^*$) to acquire the error of the DC link voltage. The error signal is then applied to the PI controller to obtain the phase shift angle. The gate signals are then generated using the phase shift angle.

DC Link Controller	
Proportional Gain (K_{p_dc})	2
Integral Gain (K_{i_dc})	0.3
Reactive Power Compensation Controller	
Proportional Gain (K_{p_reac})	0.05
Integral Gain (K_{i_reac})	0.5

Table.1 Controller Parameter

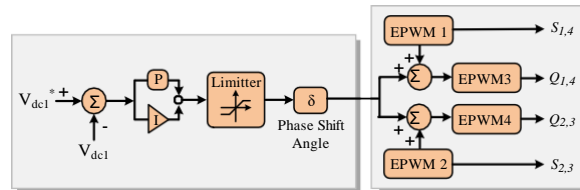


Fig 2. Active Controller

D.VOLTAGE SAG SWELLS

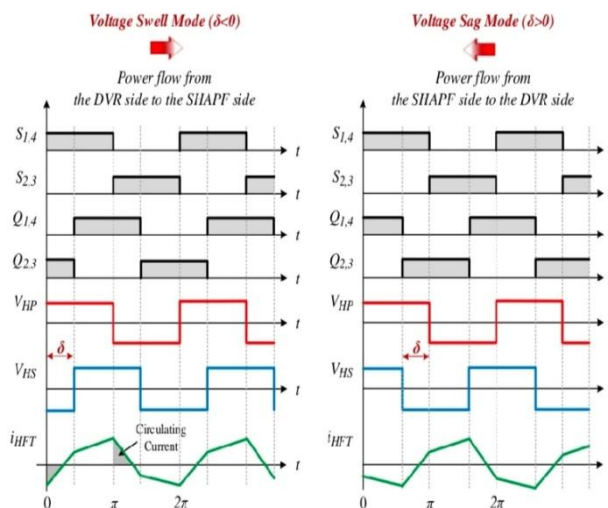


Fig 3. Sag Swell Comparison

Voltage sag detection method has a significant impact on the performance of the DVR controller. In order to detect both balanced and unbalanced voltage sag/swells fast and accurately, a hybrid detection method based on the combination of the ICT and the EPLL is proposed. The instantaneous magnitude signal of the distorted busbar voltage in any phase is calculated by taking the average of the magnitude signals obtained from the ICT and the EPLL. The proposed method is simple, reliable and practically applicable for single and three phase systems. According to the control scheme, the distorted busbar voltage $V_{s,n}(t)$ is firstly converted to per unit (p.u.) value $un(t)$. The DVR side DC link voltage value is maintained constant at the desired value with a proper phase shift angle obtained by PI controller against the variations of SHAPF side DC link voltage level. The measured DVR side DC link voltage (V_{dcl}) is subtracted from the reference voltage value (V_{dcl}^*) to acquire the error of the DC link voltage. The error signal is then applied to the PI controller to obtain the phase shift angle. The gate signals are then generated using the phase shift angle.

The BiDC has two different operating modes depending on the power flow direction determined according to the sign of the phase shift angle. The phase shift angle is positive and the power flows from the SHAPF side to the DVR side (voltage sag mode) when voltage V_{HP} leads voltage V_{HS} . In the opposite case, the phase shift angle is negative and power flows from the DVR side to the SHAPF side (voltage swell mode) when voltage V_{HP} lags voltage V_{HS} . The circulating current, shown in Fig. 4, is caused by the difference between the magnitudes of the voltages V_{HP} and V_{HS} , and it affects power loss and the efficiency of the BiDC

IV. EXPERIMENTAL RESULTS

The effectiveness of the proposed HUPQC is verified through experimental studies carried out on a DSP controlled three-phase laboratory scale prototype. The experimental setup of the HUPQC has been installed on a two-layer panel made up of metal sheet with dimensions of 230x100 cm. The power circuits and the electronic control systems are located on the first and second layers of the metal panel separately, as shown in Fig. 5. The power circuit parameters of the implemented HUPQC system are provided in Table IV. The power circuits of the inverters in the HUPQC system are formed by using a total of thirteen half bridge Semikron SEMiX-202GB12E4s Trench IGBT modules that are driven with Semikron SKYPER PRO 32 R drivers. The high frequency transformer used in the BiDC part of the HUPQC is specially designed with a volume of 297 cm³ by using UU 93 ferrite core that offers high permeability at high frequencies. The capacitor bank at both the DVR and the SHAPF side DC The controller algorithms of the SHAPF, the DVR and the BiDC have been performed digitally by using three independent DSPs (32-bit floating-point DSP TMS320F28335 of Texas Instruments). The DSP in which the BiDC controller is embedded, receives the synchronized control signals from other parts of the HUPQC and manages the operation of the entire system in real-time with respect to the conditions of these signals. The sampling and switching frequencies for the DVR, the SHAPF and the BiDC controller algorithms are assigned to be 10 kHz, 10 kHz and 20 kHz respectively. The AC source and load voltages as well as the DC-link voltages are measured with LEM LV 25P voltage transducers employed in the signal conditioning boards, whereas all the current measurements are realized with Multimic CTF 50A split type current sensors

In order to validate voltage compensation performance of the HUPQC, a sag-swell generator capable of producing balanced/unbalanced 50% voltage sag and 30% voltage swell, is developed. Additionally, an experimental platform for the test load group consisting of three phase six pulse rectifiers and inductive loads is built in the laboratory as demonstrated in Fig. 6. The assembled HUPQC prototype is tested in terms of suppression of the low-order dominant current harmonics up to 7A and compensation of the reactive power in the range of 10kVAR \pm 30% caused by the load group. Experimental results are taken over 9-minute time interval together with a pre-designed measurement card. The current and voltage waveforms are processed by using four-slot NI cDAQ 9184 Ethernet chassis and NI 9205 module that features 16-bit resolution with a maximum sampling rate of 250 kS/s. The power, RMS and harmonic measurements are recorded

	Parameters	Value
Supply	Utility Supply ($V_{g,abc}$)	31.5 kV (L-L)
	Grid Frequency (f_g)	50 Hz
	Step-Down Transformer ($TR1$)	1 MVA, Δ/Y , 31.5/0.4 kV Uk: 5%
	Busbar Voltage (V_s)	400 V (L-L)
DVR	Power Rating	12 kVA
	Maximum voltage injection capability	110 V _{rms} (each of the phase for 50% sag)
	Injection Transformers ($TR2, TR3, TR4$)	4 kVA, 150:150 V 50 Hz, Uk: 1%
	Cut-off frequency of the inverter side filter	918 Hz
	Filter Capacitor ($C_{d,abc}$)	150 μ F
	Filter Reactor ($L_{d,abc}$)	0.2 mH
	Damping Resistor ($R_{d,abc}$)	0.7 Ω , 150W
BiDC	Power Rating	10 kVA
	SHAPF Side DC Link Capacitor (C_{dc1})	180 mF (100-300V adaptively changes)
	DVR Side DC Link Cap.	700 mF (160 V constant)
	High Frequency Transformer ($TR5$)	10 kVA, 400:400 V, 20 kHz, Uk: 2%, Leakage reactance: 7 μ H
	Auxiliary Reactances of the BiDC (L_{dc1}, L_{dc2})	DVR Side (L_{dc1}): 12.4 μ H SHAPF Side (L_{dc2}): 17.6 μ H
	SHAPF	PF Reactor ($L_{f,abc}$)
PF Capacitor ($C_{f,abc}$)		200 μ F (Rated voltage: 450 V _{rms})
PF cut-off frequency (f_c)		350 Hz
Reactive Power Rating		10 kVAr \pm 3 kVAr
Rated har. Comp. current		7 A

Table 2. Parameter of Compensating Devices

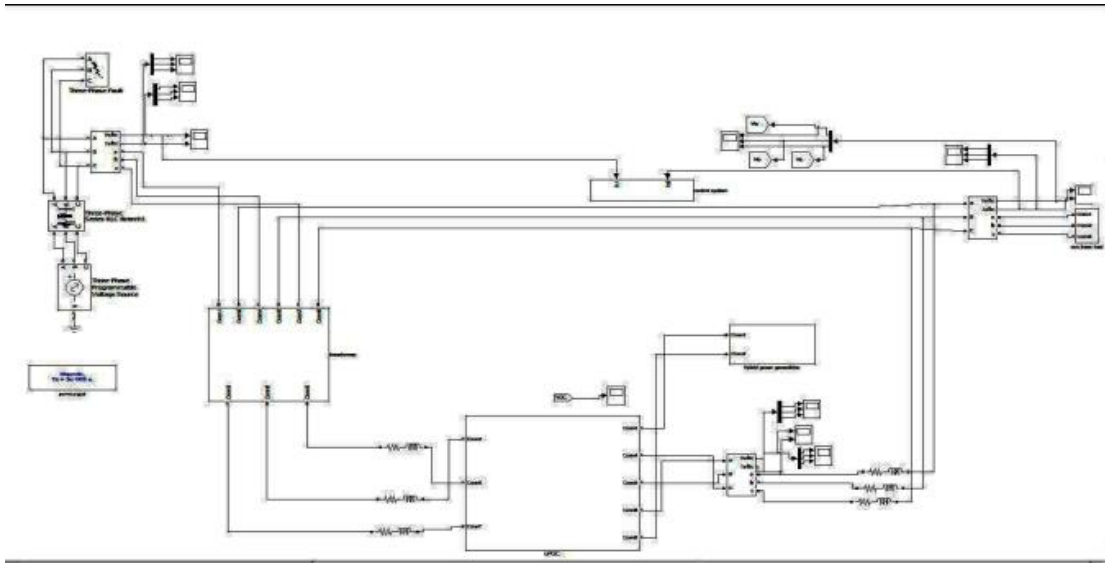


Fig 4. Simulation Diagram

The average active and reactive powers of the load group are 11.91kW and 13.92kVAr respectively. The PF of the SHAPF part of the HUPQC supplies close to 10.65 kVAr capacitive reactive power and the remaining 3.27kVAr inductive reactive power of the load group is compensated by the VSI of the SHAPF. Because of the inductive reactive power of the load is higher than the reactive power capacity of PF, the VSI of the SHAPF operates in the capacitive mode in order to meet the reactive power demand of the load group

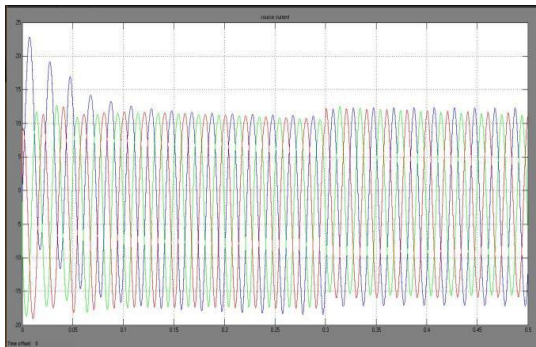


Fig. : Distorted source current

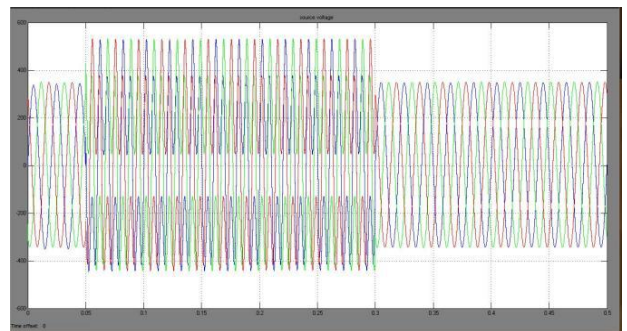


Fig. : Distorted source

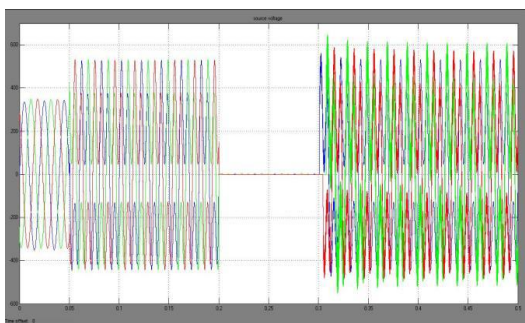


Fig. : Source voltage Interruption

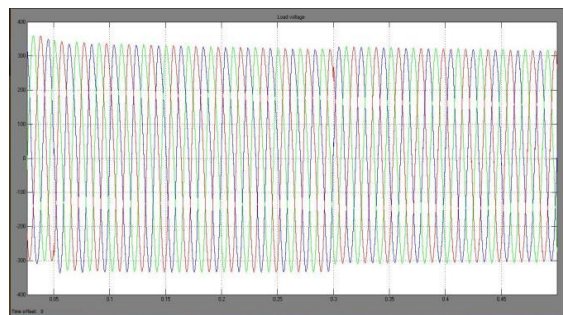


Fig. : Compensated load

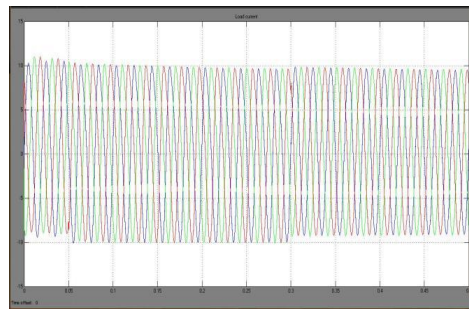


Fig.: Compensated load current

The main advantage of proposed method is to compensate deep voltage interruption. The interruption voltage present in the supply voltage is eliminated by interconnecting hybrid power generation into unified power quality conditioner through capacitor. The purpose of using this combined system is to reduce the harmonics effectively. The power factor also improved by using the combined system. The proposed model for the UPQC is to compensate input voltage harmonics and current harmonics caused by nonlinear load. The load current in both case is found to be content of all odd harmonic providing a total harmonic distortion. The hybrid power generation system proposed in this paper has the functions of improving power quality, blocking reverse power, and ensuring the continuity of electricity supply.

V. HARDWARE MODEL

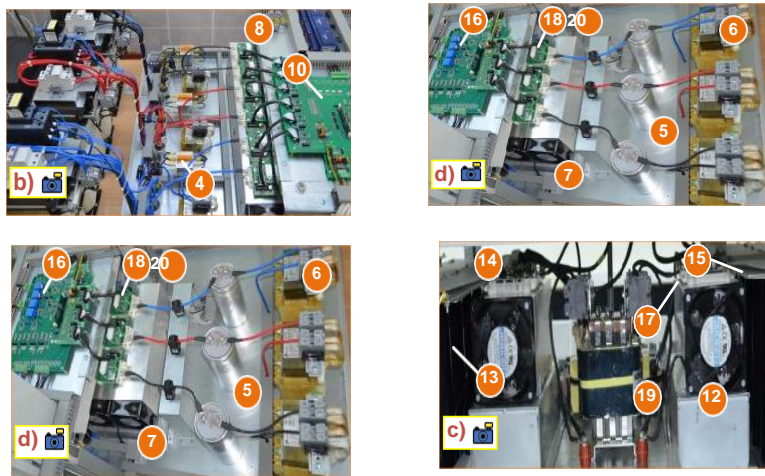


Fig.: Hardware Design

The assembled HUPQC prototype is tested in terms of suppression of the low-order dominant current harmonics up to 7A and compensation of the reactive. The controller algorithms of the SHAPF, the DVR and the BiDC have been performed digitally by using three independent DSPs (32-bit floating-point DSP TMS320F28335 of Texas Instruments). The DSP in which the BiDC controller is embedded, receives the synchronized control signals from other parts of the HUPQC and manages the operation of the entire system in real-time with respect to the conditions of these signals. The sampling and switching frequencies for the DVR, the SHAPF and the BiDC controller algorithms are assigned to be 10 kHz, 10 kHz and 20 kHz respectively. The AC source and load voltages as well as the DC-link voltages are measured with LEM LV 25P voltage transducers employed in the signal conditioning boards, whereas all the current measurements are realized with Multimic CTF 50A split type current sensors. Three generic case studies have been created to evaluate the performance of the proposed HUPQC system in point of harmonic elimination, reactive power compensation and voltage sag/swell mitigation. Each case study is performed with different varying load conditions to demonstrate the realization of the dynamic reactive power compensation and the adaptive change in the SHAPF side DC link voltage.



Table 3. Case Study

	Switched-on Loads	Reactive Power	Load Current THD	SHAPF Operation Mode
Case 1	Rectifier 1 & 2 + 5kVAr + (2 x 2kVAr) + (2 x 1kVAr)	13.92 kVAr	24.97 %	Capacitive
Case 2	Rectifier1 +(5kVAr) +(2kVAr) +(1kVAr)	9.73 kVAr	20.54 %	Capacitive & Inductive
Case 3	Rectifier1 +(5kVAr)	6.36 kVAr	27.06 %	Inductive

VI. CONCLUSION

This Paper addresses a new and versatile UPQC configuration, whose effectiveness has been validated through experimental studies to improve power quality problems in distribution networks. In the proposed HUPQC configuration, the DC link connection between SHAPF and DVR is realized by BiDC that assures galvanic isolation and allows bi-directional power flow during voltage sag and swell. Beyond the benefits of a conventional UPQC such as current harmonic elimination and voltage sag/swell mitigation, the implemented HUPQC prototype ensures dynamic reactive power compensation. In order to decrease the switching losses in low loading conditions, the SHAPF side DC link voltage level is determined adaptively depending on current harmonics level and reactive power demand of the load group. Owing to the inclusion of the BiDC in the HUPQC topology, the DVR side DC link voltage is kept constant at the reference value against adaptively changing SHAPF side DC link voltage during dynamic conditions. With the aforementioned hybrid control algorithm, both balanced and unbalanced voltage sag/swells are detected fast and compensated precisely.

The DVR part of the HUPQC system successfully provide effective protection against both balanced and unbalanced voltage sag/swells up to the depth of 50% and the duration of 100 ms. The load voltage is kept between 0.9822 p.u. and 1.023 p.u. level and the detection time is recorded as a maximum of 9.2 ms and an average of 5.9ms during case studies because of applying UPQC shunt inverter and also is the ability of compensating the voltage interruption using UPQC because of connecting distributed generation to DC link.

REFERENCES

1. K. Jindal, A. Ghosh, and A. Joshi, "Interline Unified Power Quality Conditioner," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 364-372, 2007.
2. H. R. Mohammadi, A. Y. Varjani, and H. Mokhtari, "Multiconverter Unified Power-Quality Conditioning System: MC-UPQC," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1679-1686, 2009.
3. M. Brenna, R. Faranda, and E. Tironi, "A New Proposal for Power Quality and Custom Power Improvement: OPEN UPQC," *IEEE Transactions on Power Delivery*, vol. 24, no. 4, pp. 2107-2116, 2009.
4. Teke, M. E. Meral, M. U. Cuma, M. Tümay, and K. Ç. Bayindir, "OPEN unified power quality conditioner with control based on enhanced phase locked loop," *IET Generation, Transmission & Distribution*, vol. 7, no. 3, pp. 254-264, 2013.
5. J. Wang, X. Hu, and S. Chen, "Research on detection algorithm of voltage sag characteristics," in *Proc. 7th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, July 18-20, 2012, pp. 313-318.
6. M. Inci, K. Ç. Bayındır, and M. Tümay, "Improved Synchronous Reference Frame based controller method for multifunctional compensation," *Electric Power Systems Research*, vol. 141, pp. 500-509, 2016.
7. M. Karimi-Ghartermani and M.R. Irvani, "A nonlinear adaptive filter for online signal analysis in power systems: applications", *IEEE Transactions on Power Delivery*, vol. 17, issue. 2, 2002, pp. 617-622.
8. Tan, T. Koroglu, T. Demirdelen, M. Inci, M.U. Cuma, K.C. Bayindir,
9. M. Tumay, "Performance investigation of shunt hybrid active power filter with a synchronous reference frame based controller," in *Proc. IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 22-25, 2015, pp. 1-8.
10. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091-4106, 2014.
11. R. Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 12-16, 2010, pp. 1129-1135



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