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Implementation of Low Power Vedic Multiplier Using Reversible Logic Gates

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ABSTRACT: Reversible logic is one of innovative technology in present days due to power consumption is drastically reduced. In the digital circuits amount of energy is dissipated as the bits of information are lost during logical operations and loss of information can be reduced by using reversible logic gates. Multiplication plays important role in the dsp processors Reversible computation is an emerging area of research, having applications in numerous fields. In this paper a reversible Vedic multiplier is designed and compared with booth multiplier. The design is based on Vedic method of multiplication. The design is based on Vedic method of multiplication. In booth multiplier 41.7 nsec delay and power 2.23mw is obtained, Vedic multiplier the delay has reduced to 24.7nsec and power 1.3 mw. From the obtained results, it is clear that the UT reversible Vedic multiplier can perform better than the existed booth multiplier. And it is implemented by using Xilinx software using Verilog.

KEYWORDS: Reversible logic, Vedic multiplier, Urdhva Tiryakbhyam

I. INTRODUCTION

Energy dissipation is of fundamental in the design and implementation of VLSI circuits [1]. As the number of circuits integrated on a chip increases and the chip size decreases, energy dissipation thus becomes the greater area of important for designers. Conventional digital circuits dissipate an important amount of energy owing to loss of information. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least $KT \ln 2$ joules, where K is the Boltzmann's constant and T is the temperature at which operation is performed [1]. Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of Mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirtha after his research on Vedas. He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhila Sutra, Urdhva Tiryakbhyam, and Anurupya. It has been found that Urdhva Tiryakbhyam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline [3]. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. Hence Vedic mathematics can be applied here to perform multiplication. Reversible logic is one of the promising fields for future low power design technologies. Since one of the requirements of all DSP processors and other hand-held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical. This paper proposes an implementation of Reversible Urdhva Tiryakbhyam Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm Urdhva Tiryakbhyam and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. [4]

II. REVERSIBLE LOGIC GATES

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs [8- 10]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. There are many numbers of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity.

2.1 TOFFOLI GATE:

TOFFOLI gate which is a 3*3 gate with inputs (A, B, C) and outputs $P=A$, $Q=B$, $R=AB \text{ XOR } C$. It has Quantum cost is five.

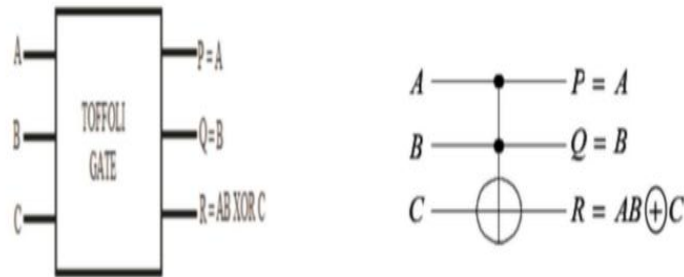


FIG1toffoli Gate and Its Symbolic Representation

2.2 Feynman Gate:

It is a 2*2 Feynman gate. Quantum cost of a Feynman gate is 1 and is called as Controlled NOT gate or CNOT gate. It is identical to single control input Toffoli gate.



Fig 2: Feynman Gate and Its Symbolic Representation

2.3 Peres Gate:

It is a 3*3 Peres gate. The vector input is $I(A, B, C)$ and the vector output is $O(P,Q,R)$. The outputs are defined by $P=A$, $Q=A \text{ XOR } B$, $R=AB \text{ XOR } C$. Quantum cost of a Peres gate is 4. It needs two Toffoli gates for its construction

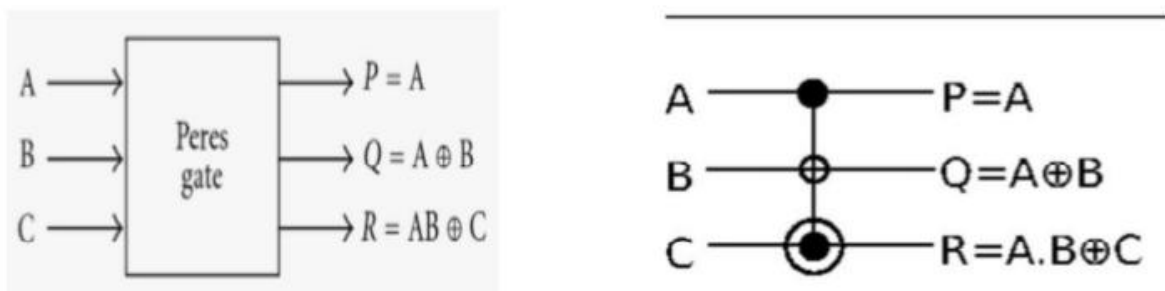


FIG 3:Peres Gate and Its Symbolic Representation



2.4 CNOT Gate:

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as the input vector is I(X, Y) and the output vector is O(P,Q). The outputs are defined by P=X, Q=X XOR Y. Quantum cost of CNOT gate is 1.

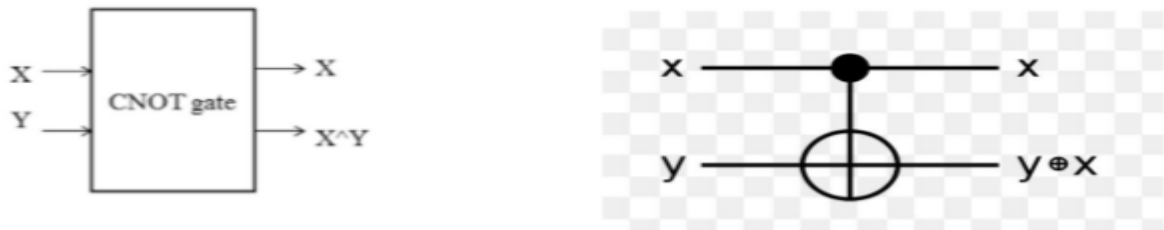


Fig:4 Cnot Gate and Its Symbolic Representation

III. VEDIC MULTIPLIER

Vedic Mathematics is much simple and easy to understand. It also improves the speed of calculation. The word ‘Vedic’ is obtained from word “Veda” and its meaning is “store house of all knowledge”. The Vedic multiplier has applications in microprocessors, filtering, Fourier transform, communication and Digital Signal Processing. Ancient Vedic mathematics consists of 16 Sutras that are related to different branches of mathematics like algebra, arithmetic and geometry. Vedic Multiplier mainly used “Urdhva Tiryagbhyam” (Vertically and Crosswise) which is used for both binary and decimal multiplication. This technique consists of generation of partial products and then performs addition simultaneously. This method can be used for 2x2, 4x4.....NxN bit multiplication.

IV. REVERSIBLE VEDIC MULTIPLIER

Vedic multiplication is divided into sixteen sutras. Urdhva Triyakbhyam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved. The algorithm uses vertically and crosswise multiplication. As the partial products and their sum are calculated parallelly algorithm is independent of clock frequency of the processor. Hence, it is well adapted to parallel processing. This in turn reduces delay, which is the primary aim behind this work. The main advantage of Urdhva Triyakbhyam algorithm is to design a low power multiplier.

V. URDHVA TRIYAKBHYAM

UrdhvaTiryakbhyam is the general formula applicable for all cases of multiplication and also in the division of a large number by another large number [6]. It means vertically and crosswise where we multiply the numbers by places that is unit place multiply by unit place gives the unit place while tens place multiply by unit’s place give the ten place and so on.

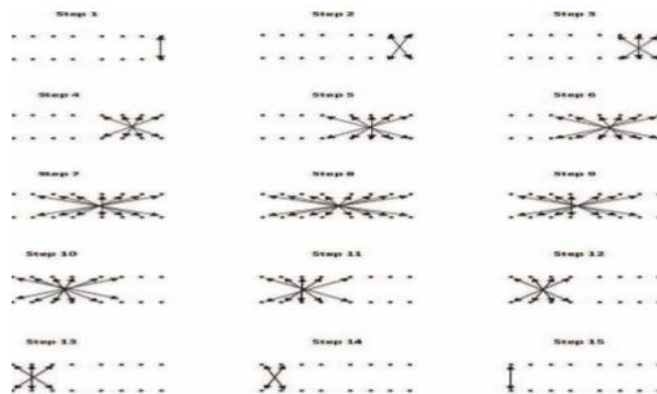


Fig 5 Urdhva Triyakbhyam Algorithm

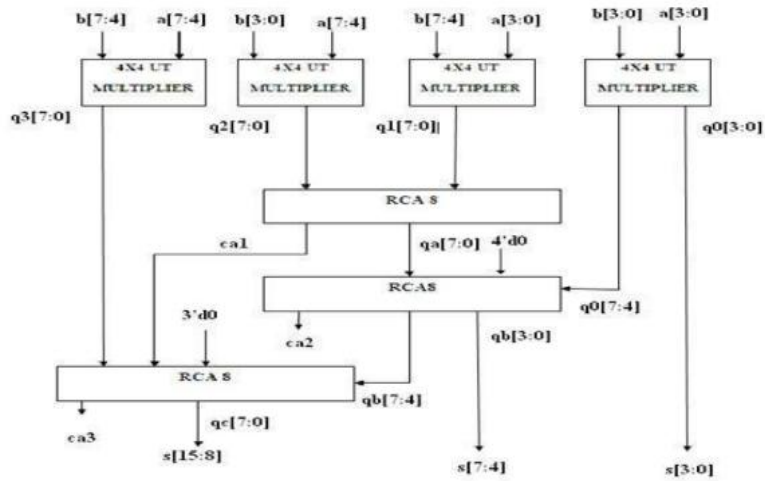
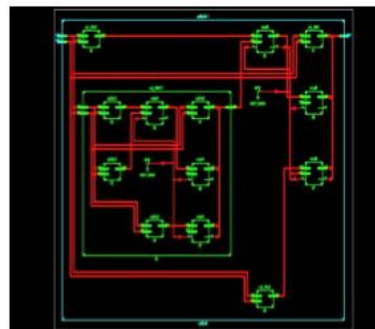
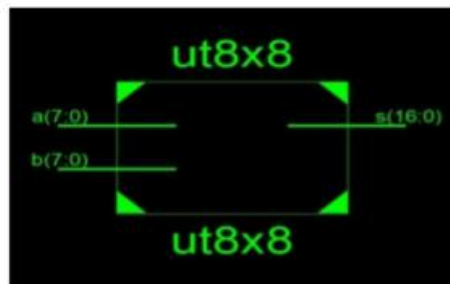


Fig 6 Reversible 8*8 Vedic Multiplier

VI. SIMULATION RESULTS

RTL Schematic:



Signal	0	1	2	3	4	5	6	7	8
q3	0000	0000	0000	0000	0000	0000	0000	0000	0000
q2	0000	0000	0000	0000	0000	0000	0000	0000	0000
q1	0000	0000	0000	0000	0000	0000	0000	0000	0000
q0	0000	0000	0000	0000	0000	0000	0000	0000	0000
ca1	0000	0000	0000	0000	0000	0000	0000	0000	0000
ca2	0000	0000	0000	0000	0000	0000	0000	0000	0000
ca3	0000	0000	0000	0000	0000	0000	0000	0000	0000
qa	0000	0000	0000	0000	0000	0000	0000	0000	0000
qb	0000	0000	0000	0000	0000	0000	0000	0000	0000
qc	0000	0000	0000	0000	0000	0000	0000	0000	0000
s	0000	0000	0000	0000	0000	0000	0000	0000	0000

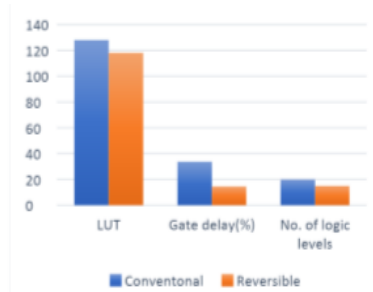


Table :1 comparison with different parameters

PARAMETERS	CONVENTIONAL MULTIPLIER (BOOTH MULTIPLIER)	VEDIC MULTIPLIER
Gate Delay(Logic	2.361ns (33.6%)	1.262ns (14.5%)
Look Up Tables	128	118
Number Of Logic Level	20	15
Power	2.2mW	1.3mW

VII. CONCLUSION

Multiplication plays important role in the processors. Reversible computation is an emerging area of research, having applications in numerous fields. In this paper a reversible Vedic multiplier is proposed using Urdhva Tiryakbhyam sutra. In this paper, an 8*8 UT Reversible Vedic multiplier is designed and compared with 8*8 Conventional Vedic multiplier by using Xilinx software. The design is based on Vedic method of multiplication. In Conventional Vedic multiplier 2.361nsec gate delay is obtained, whereas in UT Reversible Vedic multiplier the gate delay has reduced to 1.262nsec. So, from the obtained results, it is clear that the UT Reversible Vedic multiplier can perform better than the existing Conventional Vedic multiplier.

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