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# Design of IEEE 754 Floating-Point Multiplier by Vedic Sutra's Application

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**ABSTRACT:** The Technique of Vedic Multiplication is used to implement IEEE 754 Floating point multiplier. The Urdhva-triyakbhyam sutra is used for the multiplication of Mantissa part. The underflow and overflow cases are handled by it. The inputs to the multiplier are provided in IEEE 754, 32-bit format. The multiplier implemented here is based on the ancient Vedic Multiplication Technique. The Urdhva-Tiryakbhyam and Nikhilam sutras are used for multiplication iteration. The multiplier based on ancient technique is compared with the modern multiplier to highlight the power and speed advantages in the Vedic Multipliers. The Vedic Multiplier is tested by using BIST (Built in Self-Test) and it is found Fault free design. The results are compared with the Booth's Multiplier in terms of time delay and power. The multiplier is implemented in VHDL and Virtex-5 FPGA board is used.

**KEYWORDS:** Vedic multiplication, Urdhva-Tiryakbhyam sutra, Nikhilam sutra, BIST, Floating Point multiplier, FPGA board.

## I. INTRODUCTION

Sometimes DSP applications essentially require the multiplication of binary floating-point numbers. The IEEE 754 standard provides the format for representation of binary Floating-point numbers. The Binary Floating-point numbers are represented in Single and Double formats. The Single consist of 32 bits and the Double consist of 64 bits. The formats are composed of 3 fields: Sign, Exponent and Mantissa. The figure 1 shows the structure of Single and Double formats of IEEE 754 standard. In case of Single, the Mantissa is represented in 23 bits and 1 bit is added to the MSB for normalization, Exponent is represented in 8 bits which is biased to 127, the Exponent is represented in excess 127-bit format and MSB of Single is reserved for Sign bit. When the sign bit is 0 that means the number is positive. In 64bits format the Mantissa is represented in 52 bits..

## II. RELATED WORK

In 64 bits format the Mantissa is represented in 52 bits, the Exponent is represented in 11 bits which is biased to 1023 and the MSB of Double is reserved for sign bit. IEEE 754 format is done by multiplying the normalized 24-bit mantissa, adding the biased 8 bits exponent and resultant is converted in excess 127-bit format, for the sign calculation the input sign bits are XORed. The standard format for representation of floating-point number is

$$(-1)^S 2^E (b_0.b_1b_2.....b_{p-1})$$

The biased exponent  $e = E + 127$ , and the fraction  $f = b_1b_2 .....b_{p-1}$ . The Mantissa Calculation Unit requires a 24-bit multiplier if 32-bit single IEEE 754 format is considered [4]. In this paper we propose the efficient use of Vedic Multiplication Technique for this 24-bit multiplier. The Exponent Calculation Unit is implemented in this paper using 8 BIT Ripple Carry Adder. The advantages of ripple carry adder in addition to its implementation ease are low area and simple layout.

III. METHODOLOGY

This paper describes the implementation and design of IEEE 754 Floating Point Multiplier based on Vedic Multiplication Technique. Section II explores the basics of IEEE 754 floating point representation and implementation of floating-point multiplier using Vedic multiplication technique. The multiplier for the floating-point numbers represented in IEEE 754 format can be divided in four different units:

Mantissa Calculation Unit

Exponent Calculation Unit

Sign Calculation Unit

Control Unit

Here, MSB of the 32-bit operand shows the sign bit, the exponents are expressed in excess 127 bit and the mantissa is represented in 23 bits. Sign of the result is calculated by XORing sign bits of both the operands A and B. In this case sign bit obtained after XORing is 1. Exponents of A and B are added to get the resultant exponent and forwarded it to next level.

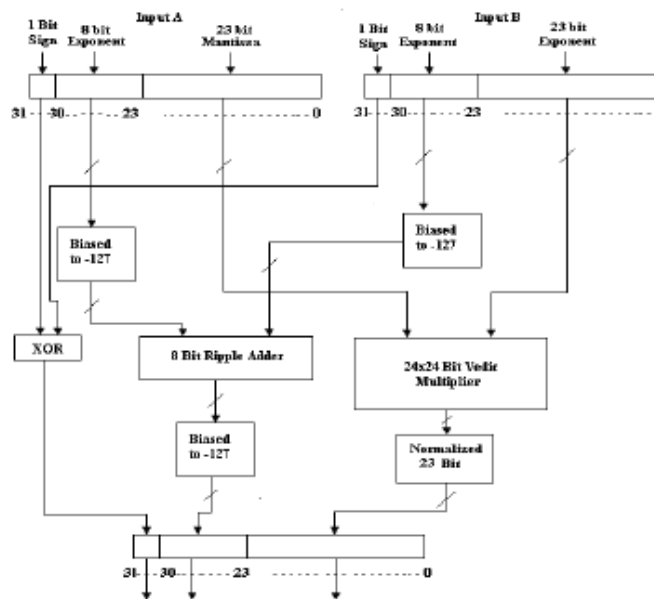


Fig 1. Proposed architecture for IEEE 754 multiplier

EIGHT BIT RIPPLE CARRY ADDER

Here, MSB of the 32-bit operand shows the sign bit, the exponents are expressed in excess 127 bit and the mantissa is represented in 23 bits. Sign of the result is calculated by XORing sign bits of both the operands A and B [8]. In this case sign bit obtained after XORing is 1. Exponents of A and B are added to get the resultant exponent. Addition of exponent is done using 8-bit ripple carry adder Figure 2.

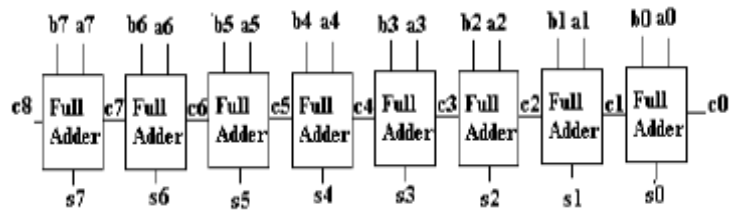


Fig 2. 8-bit ripple carry adder

After addition, the result is again biased to excess 127-bitCode. For this purpose, 127 is subtracted from the result. Two's complement subtraction using addition is incorporated for this purpose. If ER is the final resultant exponent then,

Where  $E_A$  and  $E_B$  are the exponent parts of operands A and B respectively. In this case  $E_R = 10000110$ . Mantissamultiplication is done using the 24-bit Vedic Multiplier. Themantissa is expressed in 23 bit which is normalized to 24 bits by adding a 1 at MSB. The normalized 24-bit mantissas are

$$\begin{aligned} &100110000000000000000000 \\ &100110000000000000000000 \end{aligned}$$

Multiplication of two, 24-bit mantissa is done using the Vedic Multiplier. In this case 48-bit result obtained after the multiplication of mantissa is

$$1011101001000$$

Now setting up three intermediate results the result normalizing the mantissa by eliminating most significant 1, we obtained is:

$$1\ 10000110\ 011010010000000000000000$$

$$\begin{aligned} AxB &= -19.0 \times 9.5 \\ &= -180.5 \\ &= -1.01101001 \times 2^{134-127} \\ &= (-10110100.1)_2 \\ &= (-180.5)_{10} \end{aligned}$$

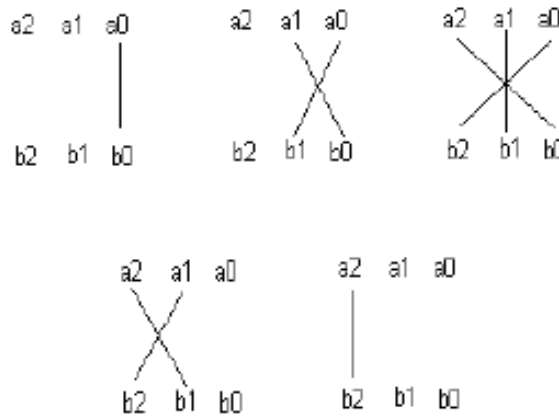
### MODELLING AND ANALYSIS

The performance of Mantissa calculation Unit dominates overall performance of the Floating-Point Multiplier. This unit requires unsigned multiplier for multiplication of 24x24 BITS. The Vedic Multiplication technique is chosen for the implementation of this unit. This technique gives promising result in terms of speed and power [9]. The Vedic multiplication system is based on 16 Vedic sutras or aphorisms, which describes natural ways of solving a whole range of mathematical problems. Out of these 16 Vedic Sutras the Urdhva-triyakbhyam sutra is suitable for this purpose. In this method the partial products are generated simultaneously which itself reduces delay and makes this method fast. The method for multiplication of two, 3 BITS number is shown Figure 3. Consider the numbers A and B where  $A = a_2a_1a_0$  and  $B = b_2b_1b_0$ . The LSB of A is multiplied with the LSB of B:

$$\begin{aligned} s_0 &= a_0b_0. \\ \text{Here } c_1 &\text{ is carry and } s_1 \text{ is sum. Next step is to add } c_1 \text{ with} \\ &\text{the multiplication results of } a_0 \text{ with } b_2, a_1 \text{ with } b_1 \text{ and } a_2 \text{ with} \\ &b_0. \\ c_2s_2 &= c_1 + a_2b_0 + a_1b_1 + a_0b_2. \\ \text{Next step is to add } c_3 &\text{ with the multiplication results of } a_1 \\ &\text{with } b_2 \text{ and } a_2 \text{ with } b_1. \\ c_3s_3 &= c_2 + a_1b_2 + a_2b_1. \\ \text{Similarly, the last step} \end{aligned}$$



$c4s4=c3+a2b2.$



**Fig 3. Vedic iteration sutra method**

Now the result of multiplication of A and B is  $c4s4s3s2s1s0$ . Consider the inputs A and B of 24 BIT each. The lower twelve BITS of input A (A11-A0) are multiplied with the lower twelve BITS of B (B11-B0). This produces the 24 BITS result out of which lower 12 BITS are considered as the lower 12 BITS of the result and the upper 12 BITS are considered as carry. The lower 12 BITS of A are multiplied with the upper 12 BITS of B, similarly the lower 12 BITS of B, are multiplied with the upper 12 BITS of A and the result of this multiplication is added with the previous carry.

#### IV. EXPERIMENTAL RESULTS

The multiplier is designed in VHDL and simulated using Modelsim Simulator. The design was synthesized using Xilinx ISE 12.1 tool targeting the Xilinx Virtex 5 xc5v1x30-3-ff324FPGA. A test bench is used to generate the stimulus and the multiplier operation is verified. The overflow and under flow flags are incorporated in the design to show the overflow and under flow cases.

the efficient use of Vedic multiplication method to multiply two floating point numbers. The lesser number of LUTs verifies that the hardware requirement is reduced, thereby reducing the power consumption. The power is reduced affectively still not compromising delay so much. The Table 1 shows the summary of the multiplier tested.

**Table 1.** Proposed Design Summary

S.N.	Parameter	Proposed work	Previous Work
1	Device	Virtex 5	Virtex 2p
2	Power Consumption	26.97mW	55mW
3	Time delay	5.01ns	3.070ns
4	Number of LUTs	947	1316
5	Number of IOs	97	100
6	Power Delay Product	136.53pJ	168.85pJ



## V. CONCLUSION

So finally, in this paper we have observed that the design of floating-point multiplier using vedic iteration technique gives more appropriate and precise results when we perform the analysis part on Virtex 5 despite Virtex 2p as we can easily check from table no 1.

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