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Innovative Low-Noise Amplifier Design for Enhanced RF System

Sai Kumar Marri, Sikender E

Student Researcher, Department of Electrical Engineering, UTD, USA

Student Researcher, Department of Electronics and Communications Engineering, VCE, India

ABSTRACT: Low-Noise Amplifiers (LNAs) are critical components in radio frequency (RF) systems, serving as the initial stage in receivers to amplify weak signals while minimizing noise contributions. This paper explores innovative LNA design methodologies aimed at enhancing RF system performance across various applications, including 5G, satellite communications, and IoT. The focus is on leveraging advanced CMOS, SOI, and GaAs technologies to achieve an optimal balance between noise figure, gain, linearity, and power efficiency [3].

Key design strategies discussed include inductive degeneration for noise matching, cascode topologies for improved isolation and stability, and magnetic feedback for enhanced input-output linearity. Additionally, advanced techniques such as simulated annealing algorithms and black-box modelling are introduced to optimize device parameters and streamline the design process [4].

Since the LNA is component that will set the noise figure for the rest of the receiver system. The purpose of this experimental study is to design an LNA that will be able to meet the required specifications. The specification on matching, noise figure, gain, and linearity are very important in LNA design. In this report we will discuss our design, layout of the LNA, and discuss how our design exceeded the required specifications, even with a 5% variation for the inductor dimensions and a 10% variation for the capacitor dimensions [1].

This work highlights the potential of innovative LNA designs to address the growing demands of next-generation wireless communication systems, offering insights into achieving superior performance in compact and efficient architectures.

KEYWORDS: Low-Noise Amplifier (LNA), Radio Frequency (RF) Systems, Noise Figure Optimization, High-Gain Amplifier Design

I. INTRODUCTION

Low-Noise Amplifiers (LNAs) play a pivotal role in modern radio frequency (RF) systems, functioning as the critical first stage in receiver architectures. Their primary purpose is to amplify weak incoming signals while minimizing the introduction of additional noise [2]. The performance of an LNA significantly impacts the overall sensitivity and dynamic range of the receiver, making its design a cornerstone for applications in wireless communication, radar systems, satellite communication, and emerging technologies like 5G and the Internet of Things (IoT).

As RF systems evolve to accommodate higher data rates, broader bandwidths, and increasingly stringent power efficiency requirements, LNA design faces multifaceted challenges. Key performance metrics for LNAs include a low noise figure (NF), high gain, wide bandwidth, excellent linearity, and low power consumption. Achieving a balance among these often-conflicting parameters necessitates innovative design strategies and advanced fabrication technologies [8].

Traditional LNA architectures, such as the common-source amplifier with inductive degeneration, provide a robust foundation for noise matching and gain optimization. However, to address the demands of modern applications, more sophisticated topologies, such as cascode structures and feedback-based designs, are being explored. The cascode topology, for instance, offers enhanced stability, high reverse isolation, and improved gain-bandwidth product. Similarly, techniques like magnetic feedback and simultaneous noise and input matching (SNIM) have been developed to push the limits of noise figure and linearity in compact designs [9].



In addition to circuit topologies and technology considerations, advanced optimization techniques are essential to fine-tune LNA performance. Simulated annealing algorithms, black-box modeling, and automated design frameworks allow designers to navigate the complex trade-offs between noise, gain, power, and linearity. These methodologies enable the systematic exploration of parameter spaces, ensuring optimal performance for specific application requirements.

Recent advancements in LNA design have expanded the scope of achievable performance metrics. For example, LNAs operating in the Ka-band for 5G applications have demonstrated noise figures as low as 1.4 dB, with gain exceeding 12 dB and power consumption below 10 mW. Similarly, innovations in sub-6 GHz designs for wireless metropolitan area networks (WMANs) have achieved high linearity and gain with minimal power budgets, showcasing the potential of optimized architectures and cutting-edge technologies [10].

In this paper, we delve into the principles and advancements of LNA design, exploring a range of techniques and technologies that enable high-performance RF front-end solutions. By examining both theoretical foundations and practical implementations, this work aims to provide insights into the design strategies that address the challenges of modern wireless communication systems [5]. The goal is to present a comprehensive understanding of how LNAs can meet the growing demands for low-noise, high-gain, and energy-efficient RF amplifiers in next-generation applications.

II. LNA CIRCUIT DESIGN ANALYSIS

For our LNA design, we chose a cascode circuit topology comprised of a common source amplifier with inductive degeneration and a common gate amplifier. The cascode design allows us to achieve high gain, low noise, and good isolation between the input and output ports. We used the common source stage to achieve a high gain, and the common gate stage to act as a buffer and to achieve good isolation between input and output ports. Achieving good isolation (S_{12} and S_{21}) is useful when applying matching networks to the input and output of the circuit, because any change in impedance occurring in either of the ports will not affect the other. The circuit schematic of the Cascode structure was designed and implemented by Cadence Virtuoso Schematic Editor. Off chip components were modeled in our schematic to include losses to give us a more realistic design to simulate. The required specs of transducer gain, noise figure, return loss at the input and output, and the IIP3 were satisfied. After getting satisfactory results, the layout of the circuit was designed with Cadence Virtuoso Layout Editor. We were able to integrate most of the circuit elements on the IC. Only a few off-chip components would be required for the circuit to operate properly. The off-chip components are mainly used for biasing purposes, and were not integrated on chip due to their high value

PARAMETERS	DESIRED	ACHIEVED					
		$V_{DD}=1.1$		$V_{DD}=1.2$		$V_{DD}=1.3$	
		2.4GHz	2.5GHz	2.4GHz	2.5GHz	2.4GHz	2.5GHz
S_{11} (dB)	<-10dB	-13.02	-20.26	-13.02	-20.25	-12.62	-19.57
S_{22} (dB)	<-10dB	-17.44	-11.08	-17.3	-11.72	-16.95	-12.38
G_T (dB)	>12dB	12.57	12.24	12.61	12.33	12.64	12.41
N_F (dB)	<2dB	1.874	1.999	1.865	1.99	1.857	1.981
IIP ₃ (dB)	>-7dB	-6.7435		-6.3532		-5.977	
K_f (stability)	>0	1.304	1.271	1.306	1.273	1.306	1.274
Z_{in} Real (ohm)	50	32.98	41.18	32.85	40.83	32.74	40.5
Z_{in} Imaginary(ohm)	0	-7.524	0.6648	-8.277	0.1757	-8.935	-0.2922
Z_{out} Real (ohm)	50	57.67	85.62	55.71	82.05	53.85	78.89
Z_{out} Imaginary (ohm)	0	-12.37	13.45	-13.39	12.55	-14.4	11.55

Figure 1: Desired and achieved specifications of the LNA

The variability is LNA operating at 2.4 – 2.5 GHz can meet all the specifications under worst variations of the on chip inductor by +/- 3% , MOS Capacitors by +/- 10%, capacitance associated with transistors by +/- 10 and also external component by +/- 10%. The simulations were also checked for VDD variations from 1.1V to 1.3 V.

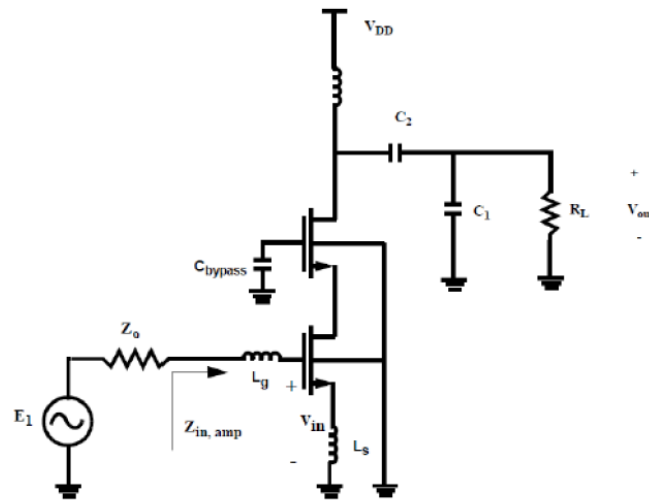


Figure 2: Ideal circuit of a Low Noise Amplifier

III. INITIAL MATLAB/HAND ANALYSIS OF THE CIRCUIT

It is important to choose suitable quality factor for input and output networks considering linearity and Power Gain. Moreover, Q_{in} and Q_{load} has to be set taking all the variations of the on-chip components and the frequency range over which the Receiver should work perfectly. If Q_{in} is high, power Gain and Noise Factor will improve but as Q_{in} is lowered, Linearity, Variability tolerance and bandwidth of the Receiver is improved. Q_{in} should be chosen in such a way so that LNA meets all the specifications. Q_{load} sets the value of Q_L , which is an important factor for improving Power Gain.

- CALCULATION OF Q_{IN} :

As per the project requirements there can be 10% variations for the on chip capacitors and 3% variations for on chip Inductors. Moreover, the receiver should work perfectly fine over the frequency range of 2.4 GHz to 2.5 GHz. Again, $S_{11lim} < -10$ dB. So, taking all these into account the Q_{in} can be calculated as:

```
S11 = -10 ;
S11_lim = 10^(S11/20);
w0 = 2*pi*2.45e9;
delta_w = 0.1e9;
var = 0.1;
a = sqrt(1 - S11_lim^2);
b = abs(((w0 + 0.1*w0 + delta_w)/w0) - (w0)/(w0 + 0.1*w0 + delta_w));
Qin_max = S11_lim/(a * b)
```

We calculated Q_{in_max} to be 1.64. We have chosen Q_{in} to be 1.5.

- ESTIMATION OF POWER GAIN(GT):

By considering the above analysis for setting Q_{in} & Q_L and taking an optimal value of 10 ohms for the resistance associated with LD, we have made an initial estimation of g_m as shown below.

```
Z0 = 50;
GT = 15;
GT_max = 31.2;
Qin = 1.5;
Qload = 3;
Rs = 10;
gm1 = sqrt(GT_max/(4 * Qin^2 * Qload^2 * Rs * Z0))
gm1 ~ 30m.
```


• ESTIMATION OF IIP3:

IIP3 is measure of linearity of the system, and mainly depends on the Q_{in} & overdrive voltage. Nonlinearity of the LNA is primarily due to drain current current nonlinearity. An ideal MOSFET, which is basically a square law device has an infinite IIP3, but the dependence of mobility on V_{gs} and V_{ds} make the drain current to have higher order non linearities. Lower Q_{in} leads to higher IIP3. Here IIP3 is calculated assuming an overdrive voltage of 0.2V and $Q_{in} : 1.5$.
 $IIP3 = 10 \cdot \log_{10}((1/(4 \cdot Q_{in}^2 \cdot Z_0)) \cdot (8 \cdot 0.2) \cdot 10^3)$

$IIP3 \sim 5dBm$

• ESTIMATION OF NOISE FIGURE:

One of the most important specifications while designing a LNA is to reduce the noise factor to a minimum value. This is because LNA is at the front end of the receiver chain and at times directly fed from the receiving antenna. The signal level is basically low and highly prone to be corrupted by noise. Here a rough value of noise figure is calculated taking the gate resistance to be 0.9 ohms which can be easily achieved with proper layout.

$R_g = 0.9;$

$g_{ds} = 7e-3;$

$\gamma = 2/3;$

$C_{gs} = 72e-15;$ %% Estimated from parameter extration

$N_f = 10 \cdot \log_{10}(1 + (R_g + \gamma \cdot g_{ds} \cdot Z_0^2 \cdot (C_{gs} \cdot \omega_0 / g_{m1}) + 20) / Z_0)$

$NF \sim 1.53dB$

IV. LNA CIRCUIT SCHEMATIC

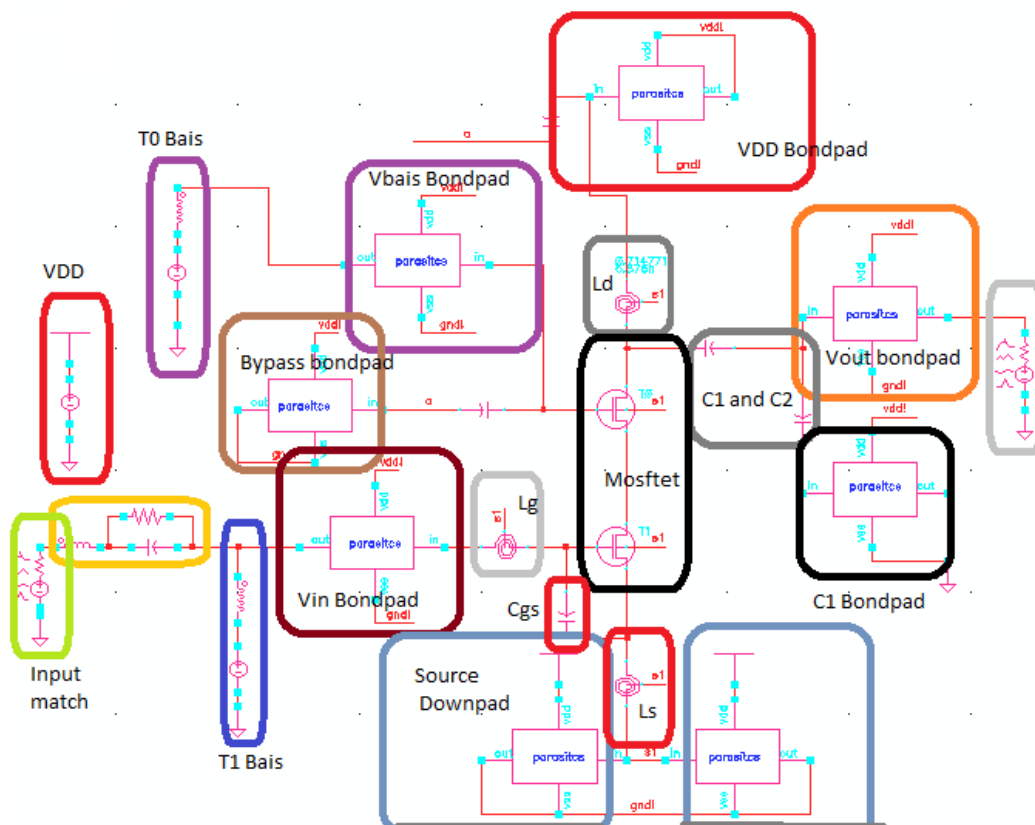


Figure 3: LNA Cadence Spectre Schematic

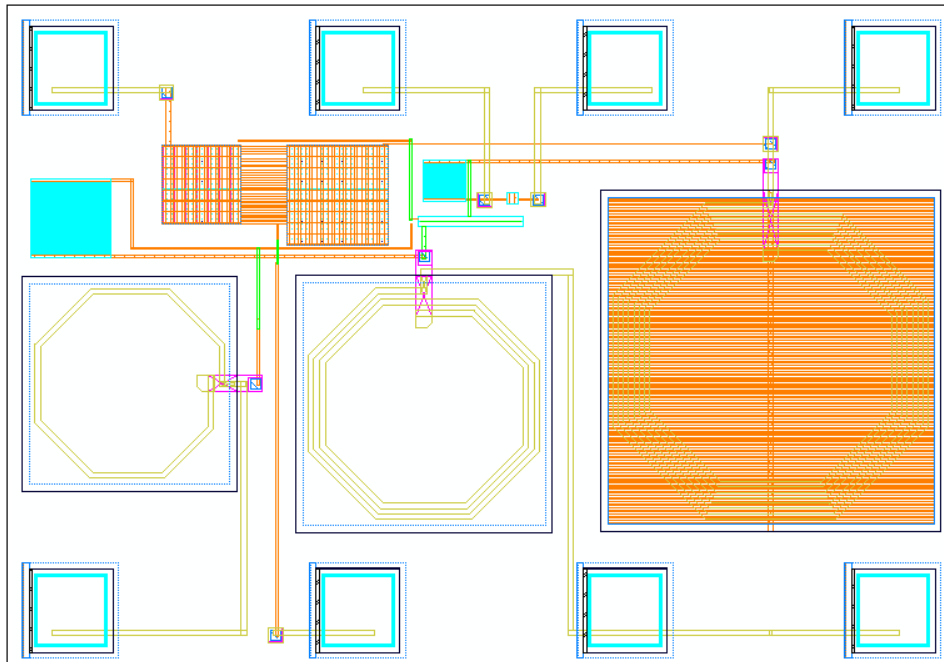


Figure 4: complete layout of the LNA circuit

Based on the above floor plan, the layout of the circuit was designed on Cadence Virtuoso. As seen in the schematic, the inductors, L_d , L_s and L_g , all are included on chip to meet the desired specifications. Thus, the chip area increased due to inclusion of more on chip inductors. Further the bias voltage capacitor (C_{bias}), supply voltage bypass capacitor (C_{supply}) are also incorporated on chip. This further adds on to the chip area. The main challenges encountered in the layout were the routing of the metal layers around the inductor coil. A minimum distance of 10um between the MG, MQ, M3, M2 and M1, and the inductor coil was maintained throughout in the layout to satisfy the DRC requirement. Thus there was a spacing-area trade-off in the layout. Also, the design has been such that the bond pads connected to ground are place together to reduce the effective bond wire inductance.

V. INSTRUCTIONS FOR THE LNA CIRCUIT OPERATION

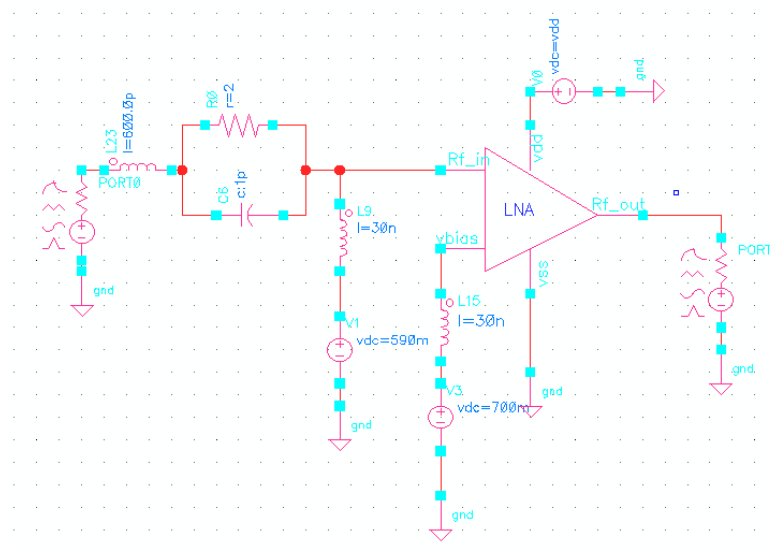


Figure 5: LNA with external circuitry



The above circuit shows the Low Noise Amplifier with appropriate DC biasing and the input and output external components. As seen in the figure, the LNA designed in this project needs DC bias voltages of 0.59V and 0.7V for the upper and lower MOSFETs of the LNA respectively. Abiding by the values specified for the external components, an RF choke of 30nH needs to be added in series to each DC bias voltage. An RF choke is used to choke or discard RF energy at the same time allowing DC current through it. Also, a 1pF capacitor needs to be used in series with the input AC source. Without this, the gate bias will be shorted by the AC source. Since it is an external or off chip component, its quality factor and parasitic inductance needs to be considered. Hence, a parallel resistance of 2 ohm and series inductance of 0.6nH are used. However, while using the circuit in practice, a capacitor of quality factor of 50 (at 1GHz) and parasitic inductance of 0.6nH is to be used.

Based on the LNA specifications listed out in this report along with the supply voltage and the on-chip component variations, one can effectively figure out the mode of operation of the circuit and hence decide the suitability of the circuit for his or her application. Following sections elaborate the specifications of the LNA and describe how they vary with the external and internal parameters.

VI. LNA CIRCUIT SIMULATION RESULTS

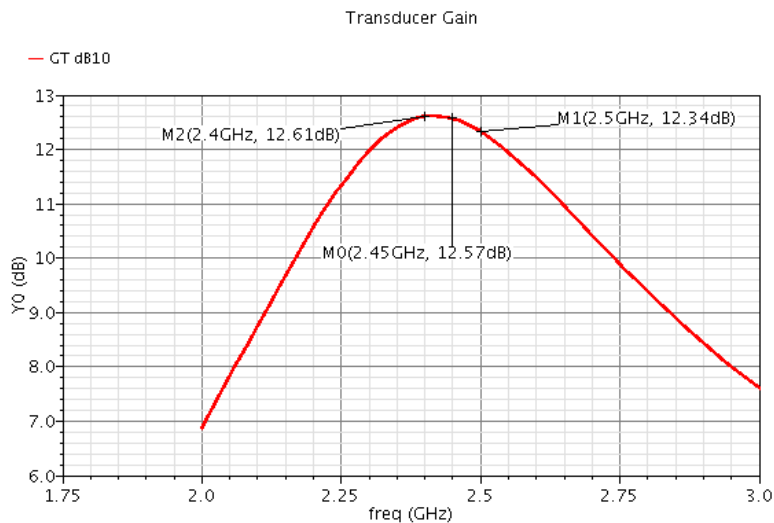


Figure 6: Plot of Transducer gain vs. frequency

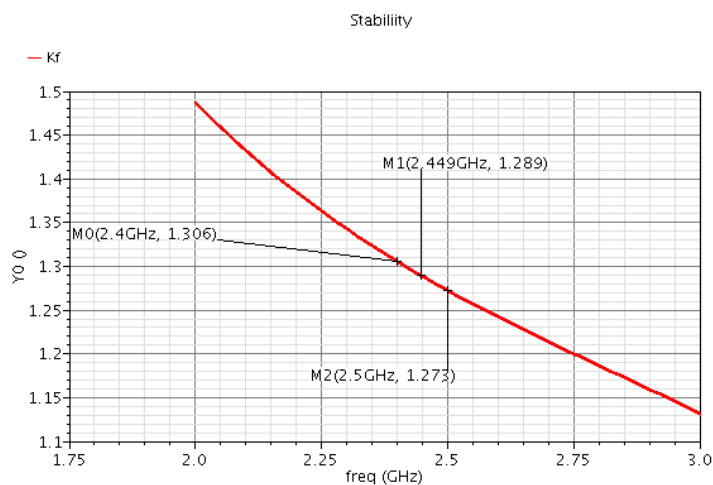


Figure 7: Plot of Stability vs. frequency

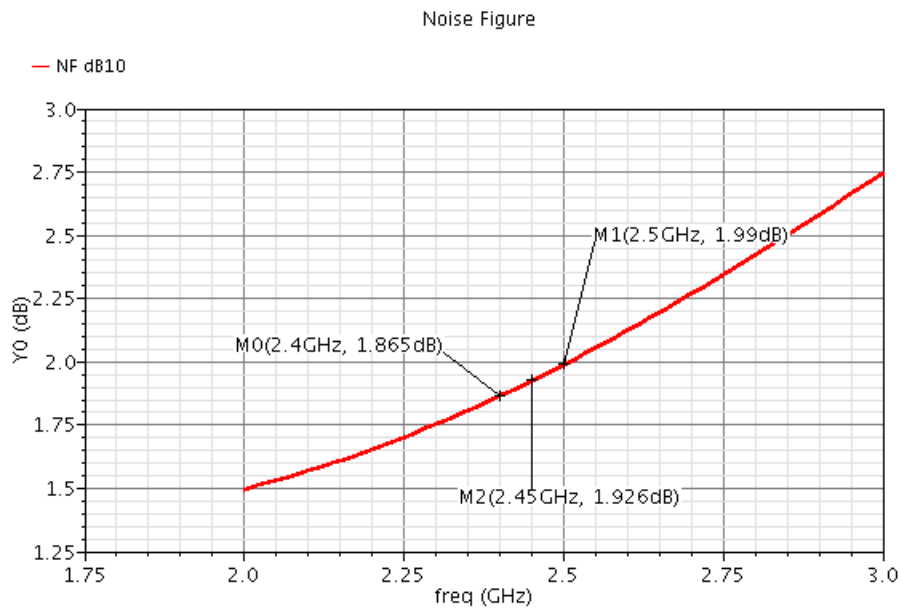


Figure 8: Plot of Noise Figure vs. Frequency

VII. COMPARISON OF HAND ANALYSIS & SIMULATION RESULTS

All the hand analysis are done taking the values provided for S11 and S22, but when the circuit is implemented and matched properly with the accurate values achieving higher S11 & S22. Thus, we have achieved values better than hand analysis.

Parameters	Hand Calculations	Simulations results (Vdd = 12V)
Lg	10nH	0.449nH
Ls	0.7nH	1.572nH
gm1	30mA/V	71.65mA/V
Width of MOS	200um	220um
IIP3	5dBm	-6.3532dBm
NF	1.53	1.865

VIII. CONCLUSION

Low-Noise Amplifiers (LNAs) are essential components in RF systems, where their design profoundly impacts the overall performance of wireless communication, satellite systems, and emerging technologies like 5G and IoT. This study has explored key LNA design methodologies, emphasizing the need to balance critical parameters such as noise figure, gain, linearity, bandwidth, and power consumption [6].

In this project, LNA cascoded amplifier is designed and implemented in 130nm CMOS technology at frequency range of 2.4-2.5Ghz. We have proceeded with the initial hand analysis as mentioned in the classroom discussions. We have taken inputs from the project description and made fair assumptions to compute the MOS parameters and passive component parameters. We have used Matlab to solve the equations. We started our design with the values derived from the hand calculations and fine-tuned the values to achieve optimal results. Also, the circuit is verified at different voltage variations (1.1v, 1.2v, 1.3v), and component variations as described in the design specification. We have come up with the layout floor plan before starting the layout and proceeded to the layout by extracting from the schematic. Connections are made using the metal layers and vias, and successfully fixed the DRC errors. Philosophies of circuit level design and layout are discussed to achieve the circuit specifications.



As wireless systems demand greater sensitivity and efficiency, LNA design will continue to be a focal point of RF engineering [7]. The insights provided in this study highlight how combining robust theoretical frameworks with advanced design tools and technologies can lead to superior RF front-end solutions, catering to the ever-growing requirements of next-generation communication systems.

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