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PERFORMANCE ANALYSIS OF AN ULTRA LOW POWER BASEBAND TRANSCIEVER IC FOR WBAN

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ABSTRACT: In this paper, we present a low complexity, ultra low power base and transceiver IC for wireless body network applications. A specified transceiver architecture is designed to implement the physical layer (PHY) and serial peripheral interface (SPI) and system performance is optimized. SIMULATED in 0.18 μm CMOS technology, the baseband chip consumes 33.18 μW for TX mode and 37.98 μW for RX mode when operating at 250 kHz system clock and 1.1 V supply.

KEYWORDS: Digital circuit design, wireless communication in a low-power WBAN wireless network.

I.INTRODUCTION

The pursuit of a higher quality of life motivates people to be more concerned about their health and potential illnesses. All this required a convenient health care monitoring system to monitor people's health anytime and anywhere, especially when people suffer from an acute event such as a sudden heart attack. The monitoring capability of such a system should also be able to ensure optimal post-surgical maintenance and support early detection of abnormal medical conditions. Recent advances in sensors, integrated circuits, and wireless communication are paving the way for the development of miniature, lightweight, ultra-low-power physiological health monitors that improve people's lives. These devices can be integrated into wireless body area networks (WBANs) for health monitoring [1]. Sport climbing encompasses a wide range of skills and abilities [2]. A WBAN topology consists of a series of physiological sensors and is able to communicate with other sensor nodes or with a central node. The central node has a higher computing capacity and communicates wirelessly with the personal server and subsequently with the outside world through standard telecommunications infrastructure such as wireless local area network and mobile phone networks. m-Health integrates mobile computing, medical sensors and communication technologies for mobile healthcare applications. Wireless Body Area Networks (WBAN) is a sensor represent a new technology for system integration with great potential to monitoring of health status over a longer period of the time. However, system designers will have to solve a number of issues, such as strict sensor weight and size constraints necessary to improve user compliance, sensor resource limitations, intermittent availability of uplink connectivity, and transmission reliability, security, and cross-platform interoperability [4]. The field of point networking is an interdisciplinary field that could enable low-cost, continuous health monitoring with real-time updating of medical records over the Internet. An array of intelligent physiological sensors can be integrated is a wireless sensor of body area network that can be used for computer-assisted rehabilitation or early detection of health problems. Implanted sensors in the human body will collect various physiological changes to monitor the patient's health status regardless of their location. The information will be transmitted wirelessly to the external processing unit. This device will instantly transmit all information in real time to doctors around the world. If an emergency is detected, doctors immediately inform the patient through the computer system by sending appropriate messages or alarms. Currently, the level of provided information and energy sources capable of powering the sensors is limiting. While this technology is still in its infancy, it is being widely researched and, once adopted, is expected to be a breakthrough in healthcare, leading to concepts such as telemedicine and m-Health becoming a reality. The long-term goal of the BAN project is to work to

reduce energy consumption to the lowest possible level, to improve acceptance and ease of use, to increase lifetime, to reduce size, to make energy-saving techniques reasonable and simply to save energy. Recently, wireless personal area network (WPAN) transceivers have been developed. For example, Texas Instruments' CC2420 can cover a range of 20-30m while consuming 60~70mW. However, such operating range and power consumption is not an optimal choice for WBAN applications, where the transceiver design target is an operating range of 1 to 3m to achieve ultra-low power. The expansion of technology into new areas could also help communication by seamlessly exchanging information between individuals or between individuals and machines. In the transmitter block, the physical layer data unit (PSDU) from the MAC layer is processed in the designed transmitter baseband (TX) processor module to generate a physical layer protocol data unit (PPDU) packet. Channel coding and signal processing is performed on PPDU in the baseband TX processor module. Raw baseband data is modulated and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low-power demodulator. The demodulated signal is processed by the proposed baseband RX processor module.

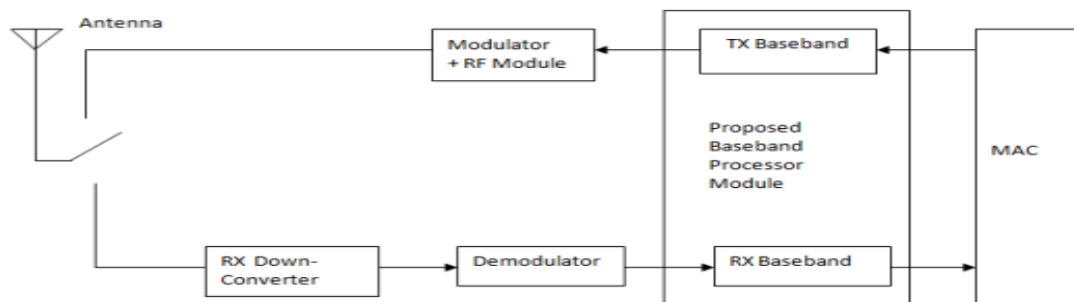


Fig.1 Block Diagram of a complete WBAN radio

II. TRANSCEIVER

The remainder of the paper is organized as follows: Section II discusses the proposed work; Section III. Proposed Codes; IVSPI section between MAC and PHYB time band; Section V design implementation and measurement results.

III. PROPOSED LOW POWER BASEBAND AND TRANSCEIVER

1. BASEBAND TRANSMITTER:

In the TX module, the baseband processor receives PSDUs from the MAC layer and creates PPDU. The allowed PSDU length within one packet should not exceed 127 octets and this information is contained in the PHY header (PHR) in octets. Once one PSDU packet is generated by the MAC layer, it is brought into the TXFIFO and ready for transmission. There is a Prefix MUX block controlled by the TX state control block to select the input of the encoder block. The output data of the encoder block is fed to the interleaving block to suppress the burst error. In order to eliminate long strings of similar bits that could disrupt the receiver's synchronization, and to eliminate most periodic bit patterns that could produce unwanted frequency components (including the DC component), the interleaved data payload is first fed into a scrambling block and then encoded by an encoder Manchester. A coding block generates a coding code in a serial sequence with a word length of 1 bit. The output data of the interleaving block is in a serial sequence with a 1-bit word length and is XORed with the generated encryption code. The encoded data is fed to the Manchester encoder. A Manchester encoder converts the "0" bit to "01" bits and converts the "1" bit to "10" bits so that the total number of "0" and "1" can be balanced. The output of the Manchester encoder is prefixed with a sync header (SHR) and sent to the modulator for transmission.

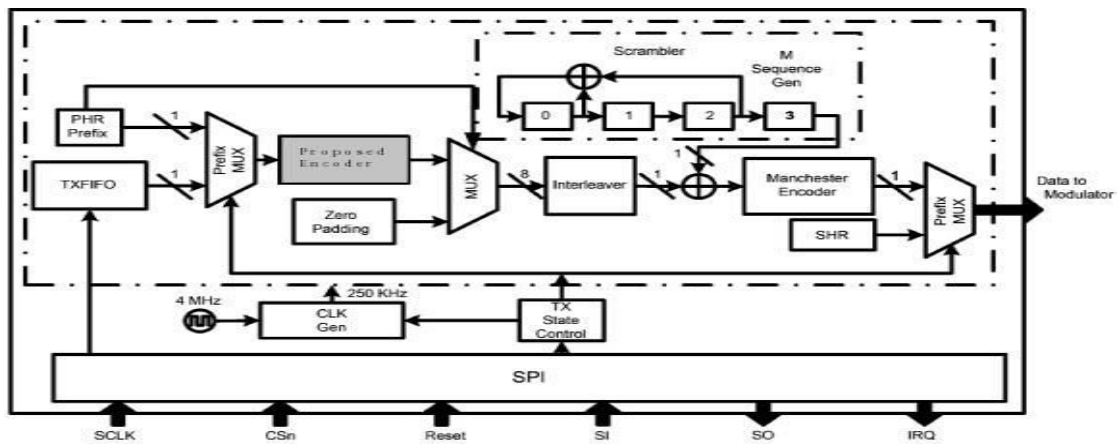


Fig.2 Block diagram of Baseband Transmitter

2.BASEBAND RECEIVER

In the receiver module, the received data stream is the demodulated binary signals from the demodulator. We use a D flip-flop provided by the technology library to sample and restore the analog input. If the input signal voltage is higher than VHL of flip-flop D, the output of flip-flop D will be “1”. If the input signal voltage is lower than the VLH of the D flip-flop, the output of the D flip-flop will be “0”. the signals are first fed in series to the synchronization and data recovery (SDR) block to achieve synchronization and recover the received data. The peak of the calculated correlation is continuously detected. Once a peak value is found, the start-of-frame delimiter (SFD) correlator block calculates the correlation between the incoming data and predefined SFD sequence and the peak value is searched using the following peak detector block. Once the peak value is found, packet synchronization is confirmed. The preamble and SFD sequences are removed and the Packet SYN block indicates to the RX State Control block that PHRs and PSDUs can be received. Manchester decoding is first performed on the received PHR and PSDU data stream by detecting the first bit for every two consecutive received bits. Then the incoming data is decoded and the structure of the decoding block is identical to the structure of the decoding block. The output of the decode block has a word length of 1 bit and the XOR operations are completed with the incoming data bit by bit. Then, the PHR and PSDU are fed to the FEC decoding block, which includes a deinterlacing block and a decoder block. The output of the deinterlacing block is fed to the decoder block. The decoder block checks the incoming data for any error and corrects the error. The PHR is decoded first, so length information about the PSDU can be obtained by the RX status control block, and there is a parallel to serial buffer, so the bits in the PSDU are fed into the RXFIFO in serial sequence with a 1-bit word length. and is read by the MAC layer.

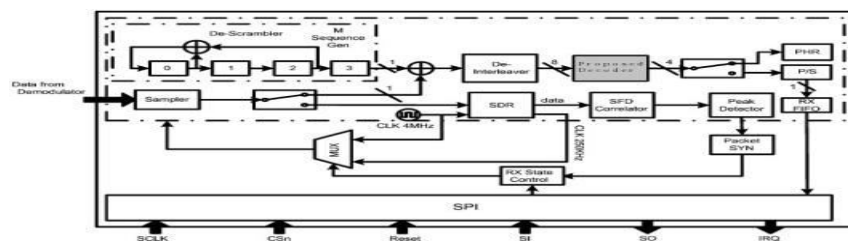


Fig.3 Block diagram of Baseband Receiver

IV.PROPOSED CODES

1.Hamming codes:

Hamming codes can detect a maximum of two errors and correct a maximum of one. Conversely, simple parity checking codes cannot correct errors and can only detect odd numbers of errors. What makes Hamming codes special is that they are perfect codes, that is, they reach the fastest with a block length and a minimum of 3. Large

computer memory (RAM) is used because Hamming codes are simple. In this case, extended Hamming code is used, usually with an additional parity bit. Extended Hamming codes have a distance of 4, which allows the algorithm to usually distinguish between cases where one is false and where two is false. In this sense, Extended Hamming codes correct an error and detect two errors, often referred to as SECDED. Bad things can be identified if there are many bug fixes in the message and different things can be configured to produce different results. There are 7 possible errors in a 7-bit message, so our error checking product not only determines that the error occurred, but also determines the cause of the bit. Hamming codes have a minimum of 3, meaning the decoder can detect and correct an error, but cannot distinguish two-bit errors in one word from an error in another word. Therefore, they can only detect two-bit errors if they don't try to fix it. To address this shortcoming, Hamming's code can be extended by adding matching elements. This increases the minimum distance of the Hamming code to 4, allowing the decoder to distinguish between one-bit errors and two-bit errors. Therefore, the decoder can detect and correct one error while detecting (but not correcting) two errors. If the decoder does not try to correct the error, it can detect up to 3 errors. This continuous Hamming code is popular in computer memory systems and is called SECDED ("One Correction, Two Observations"). Particularly popular are the short (127,120) Hamming codes plus (72,64) codes, which have an extra parity bit and have the same overhead as (9,8) parity codes.

2.LDPC codes:

The inequality detection (LDPC) code is an error correcting code, a method of sending messages over noisy transmission, and is designed to use different images. LDPC codes are capacity-based codes, meaning there is an input pattern that allows the noise level to be set very close to the maximum (Shannon limit) (even off in BEC) for symmetric memoryless channels. The noise threshold defines an upper limit on the noise channel, below which the probability of data loss can be reduced as desired. Using the confidence spread method, LDPC codes can be determined for block lengths in linear time. LDPC codes are increasingly used in applications that require high quality data and efficient transmission of bandwidth or reverse channel enhanced links in the presence of data. Although commercial use of LDPC codes lags behind other codes, especially Turbo codes, as there are no software patents, LDPC codes are more attractive than six-bit Turbo codes for some LDPC codes and become fixed codes in the new DVB-S2 standard. Not code. Digital TV satellite broadcast. LDPC type convolutional turbo codes based on FEC scheme for ITU-T G.hn standard. G.hn chose LDPC over Turbo codes because of its low resolution (especially at data rates close to 1 Gbit/s) and the proposed Turbo code shows significant errors in the need to run below the line. LDPC is also used in 10GBase-T Ethernet, which transmits data at 10 gigabits per second over twisted-pair cables. The LDPC code has been part of the Wi-Fi 802.11 standard since 2009 as part of the 802.11n High Efficiency (HT) PHY specification. For large block sizes, LDPC codes are usually generated by first learning the behavior of the decoder. Because block sizes tend to go to infinity, it can be seen that LDPC decoders have a noise level below which decisions succeed and above decisions fail. This starting point can be optimized by finding the ratio of the arcs from the drawing nodes to the arcs from the different nodes. An approximate graphical way to see this threshold is the OUTPUT chart. The generation of pseudo-random methods is based on theoretical results where for a small size the random structure provides a good decision. often uses various constraints to ensure that the desired theoretical limit of parameter size occurs in block size.

3.BCH codes:

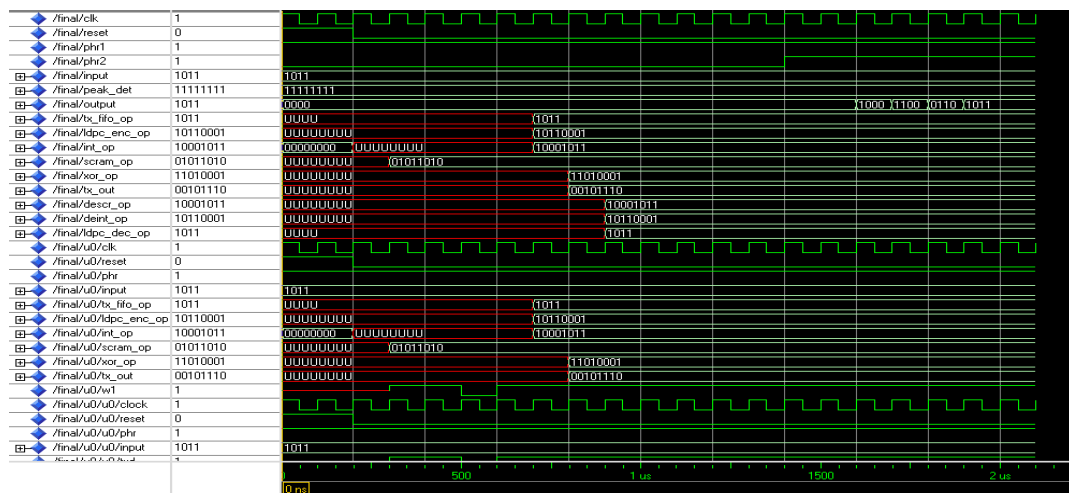
BCH codes constitute a class of parametric error correcting codes that have been the subject of intense study over the last fifty years. The BCH code was created by Hocquenghem in 1959 and himself by Bose and Ray-Chaudhuri in 1960. BCH theme contains the names of these creators. The main advantage of BCH codes is that they can be easily decoded with an elegant algebraic method called syndrome decoding. This allows very simple electronics to do the work, eliminating the need for a computer so the decision tool can be smaller and less powerful. This type of code is also very flexible, allowing to control the length of the block and its fault tolerance so that the code can be generated according to specifications. Reed-Solomon code, BCH code, used in satellite communications, compact disc . players, DVD, Disc drives and codes. Technically speaking, the BCH code is a multilevel variable

length digital error correcting code that corrects for various random errors. BCH codes can also be used with multiple levels of conversion values, as long as the level number is a prime number or a power of a prime number.

V.DESIGN IMPLEMENTATION ANDMEASUREMENT RESULTS

HAMMING CODE	Tx	35.41(μW)
	Rx	39.98(μW)
LDPC CODE	Tx	33.18(μW)
	Rx	37.98(μW)
BCH CODE	Tx	38.62(μW)
	Rx	41.81(μW)

To achieve high performance and shorten the design cycle, the proposed baseband transceiver is simulated in SYNOPSIS (DC Compiler) using 0.18 μm CMOS technology.



Tab.1 Power Consumption Chart

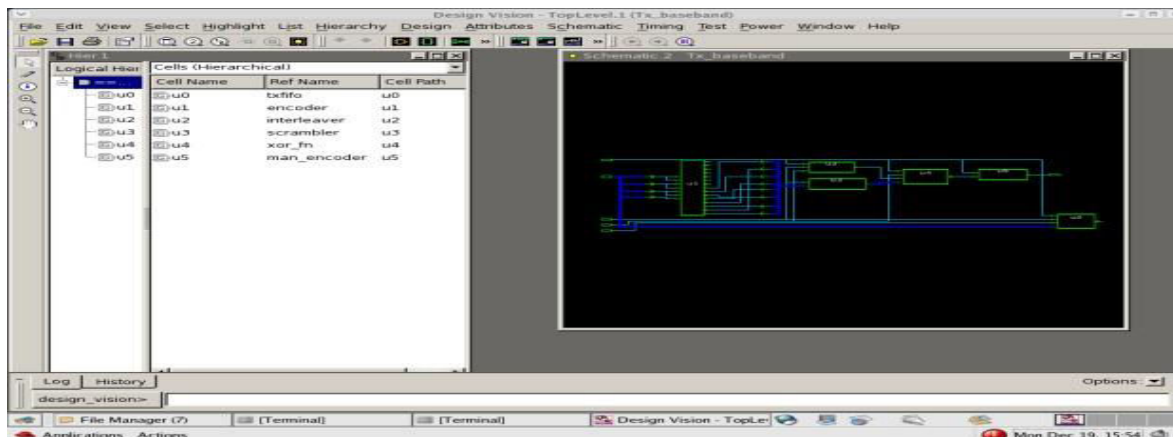


Fig.5 Schematic view of LDPC Transmitter



VI. CONCLUSION

This article presents a rare issue in the baseband PHY transceiver architecture. Depending on the design, the ultra-low power transceiver IC is used in the 0.18 μ m CMOS process. Simulated system PER performance and chip power consumption evaluate the performance of the baseband design process. Only 33 were taken for WBAN applications. 18 μ W for TX and 37.98 μ W for RX at 250 kHz clock including SPI and BCSM. The digital baseband chip can also be used for other baseband PHY communications with measurable data and power consumption.

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