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# Application of High-Speed Making Switches in Short Circuit Testing 

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#### Abstract

All the electrical devices used in transmission networks, whether its transformers, Circuit Breakers, CT's, PT'S, Distribution panels etc., in their normal lifetime are subjected to a variety of electrical, mechanical and thermal stresses. Short Circuit Currents is one of the most important and critical situations arising in any power system network that can cause severe damage to the equipment resulting from high currents produced during the fault. Due to enormous short circuits currents, high electrodynamic forces are forced on the equipment resulting in permanent damage to the protective devices and its accessories. These forces are the major cause of damaging the transmission line equipment's. The ability to withstand a short circuit is recognized as essential characteristics of any switchgear equipment installed in the power transmission or distribution network. Failures caused by short circuits are one of the major causes of outages and it depends on various circumstances, network characteristics and the equipment installed. So, keeping in mind the severe short circuits faults in any power system network, design elements must be checked by creating an intentional short circuit current which is imposed on the switchgear equipment so as to simulate the actual fault condition, in which the equipment will behave when an actual short circuit will be faced by the equipment under installation. This paper discusses the need for short circuit testing procedure and how the asymmetrical fault is generated in short circuit testing stations to simulate the actual fault conditions and difficulties involved in it.


KEYWORDS: Short circuits, Asymmetrical fault currents, PoW, Make-switch, closing time, Opening time.

## I. Introduction

The severe consequences of short-circuit currents in any transmission and distribution networks for electrical power are colossal, both for the equipment and also for the steadiness of the networks. Short circuits are not infrequent events, the ability to withstand the short-circuit is regarded as belonging to the main attributes of the equipment established. The short-circuit current must be considered at each level in the installation in view of adjudging the attributes of the equipment required to resist or break the fault current.


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Short circuit faults are most severe and commonly occurring faults in power system, they can be either a LLL short circuit fault, LL short circuit fault, LLG short circuit fault and LG short circuit fault (Figure.1) [1]. The numbers and occurrence of such external symmetrical \& asymmetrical faults on transmission lines and its associated switchgear and control-gear assemblies are most significant. Whenever such faults occur, the generated fault current from these faults will flow through the Power system (transmission \& distribution) networks resulting in huge electrodynamic forces, thermal and mechanical stresses on the equipment, these forces generated during fault conditions are transient in nature and is directly proportional to the square of instantaneous value of short circuit current. Hence the power system network along with its associated equipment's (switchgear \& control gears) must be designed and constructed to withstand the fault currents, without damage for the reliable operation of power system.

## The primary features of short circuits are:

- Time-span / period: (self-quenching, transient \& steady state) [1].
- Emergence: (Mechanical / Internal or Atmospheric Over voltages / Insulation) breakdown due to heat, humidity or corrosive environment [1].
- Place / site: Inside or outside the equipment or an electrical switchboard [1].


## Short Circuits can be:

- Phase-to-Earth ( $80 \%$ faults).
- Phase-to-Phase ( $15 \%$ faults), these faults often degenerate into three phase faults.
- Three phase (only $5 \%$ of initial faults).

These short circuit faults / currents are represented in (Figure.1). Due to increase in the short circuit power during the years, the most rigorous short circuit currents will emerge on the switchgear / control gear / Transformer equipment when its aged. These severe short circuit currents have to be withstood by the power system equipment without impairing any damage or deviation in the performance of connected equipment.

The short circuit tests are performed to verify the design characteristics of any equipment and its integrity for stresses, primarily mechanical, developed when short circuit current flows through them. The short circuit tests should be performed on a new electrical equipment ready for use in service, along with its protection accessories such as overcurrent and over voltage relays set at its maximum values or as per relevant product standards.

## II. TEST LABORATORY FEATURES

To evaluate the performance of any electrical equipment used in power system network, its performance is evaluated by artificially creating a short circuit current in the test lab so as to simulate the actual fault condition which an equipment can encounter in its actual installed condition on the grid. To perform this short circuit test, two types of sources are used in Testing Laboratories (fig.2)[11]:

1. Generator based Short-Circuit testing station.
2. On-line / Grid Short-Circuit testing station testing.
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Fig 2. Single line diagram of 1250 MVA Generator based short circuit testing lab.

At present, the author's laboratory uses 1250 MVA Generator based short circuit lab through a short circuit Generator. The power is drawn from the generator rated 1500 MVA , with an output voltage of 12.5 kV Voltage \& Short Circuit Current of 69 kA at 3000 rpm . (Fig.2) shows the single line diagram of generator based short circuit lab, in which the short circuit power is generated by using either of the two generators (one at a time). The generated power then passes this short circuit current to test object (TO) mounted in the Test cells via 36kV Master circuit breaker (MB), Source side Reactors Banks(X), Source side Resistor banks(R) and make switch (MS).

## III. DEFINITIONS

The short circuit fault created interrupts the system environment around the point of fault by giving a sudden dip in the system voltage. Whenever such severe short circuit fault occurs in the system, it has to be immediately disconnected by the action of protective devices installed in the system, so as to save the healthy part of a circuit. A typical waveform of a short circuit current is shown in (Fig.3).

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Fig. 3 Short Circuit Current Waveform.

At any given point in the system, the short circuit currents are expressed as the rms value of its AC component $\mathrm{I}_{\mathrm{SC}}$ (in $k A$ ). The maximum value of this short circuit current can have a peak value Ip in the first half cycle. This peak value $I_{P}$ is much higher than $\sqrt{ }$. Isc because of the damped DC component that is superimposed on the AC component [11].

Normally sinusoidal wave runs symmetrically with positive and negative peaks which are equidistant from the reference axis (Fig.4a). Whenever a fault is created (in testing) or occurred (naturally), this symmetrical current becomes asymmetrical in nature to the reference axis and jumps to positive or negative side i.e., positive and negative peaks are not equidistant from the reference axis depending upon the fault created time on voltage after zero crossing and lasts for few cycles (Fig.4b). That shifted asymmetrical current looks like the DC offset current with ripples. This DC offset is maximum just after the zero crossing and minimum at the $90^{\circ}$.(Fig.5)[11].


Fig. 4 (a) Symmetrical Current / Voltage Waveform.



Fig. 4 (b) Asymmetrical Current / Voltage Waveform

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This asymmetrical phenomenon or DC offset component on sinusoidal current (fig.3) occurs because of the current cannot change suddenly or instantaneously in an inductor and also current always lags voltage in the inductor [11].

This DC offset leads to jump in the peak value of the current, that peak is maximum in the first cycle and can be calculated as follows [9].

> The formula for the DC component is:

$$
i d=I d 0 e^{-R t / L}
$$

Where:
$i_{d}$ is the value of dc component at the instant $t$.
$\mathrm{I}_{\mathrm{d} 0}$ is the value of dc component at the instant taken as Time origin.
$\mathrm{L} / \mathrm{R}$ is the time constant of the circuit, in s .
t is the time, in s , taken from the initial instant.
$e$ is the base of Napierian logarithms.
The value of DC offset depends upon the:

1. Instantaneous time of voltage wave when fault created.
2. Amplitude of voltage.
3. Impedance in the circuit.
4. $\frac{X}{R}$ (Power factor) of the power system involved in the circuit (in case of Transformer).

As per relevant product standards, the value of peak currents (Ip) differs for different electrical equipment's. For switchgear and control gear assemblies as per IEC: 60947-1-2020 (ed 6.0) the values of peak currents (Ip) w.r.t to rms values (Irms) of short circuit currents are defined as per the table below [9]. Where ( $n$ ) is the ratio of Ip/Irms.

| Test Current (A) | Power <br> Factor | n |
| :---: | :---: | :---: |
| $\mathrm{I} \leq 1500$ | 0.95 | 1.41 |
| $1500<\mathrm{I} \leq 3000$ | 0.90 | 1.42 |
| $3000<\mathrm{I} \leq 4500$ | 0.80 | 1.47 |
| $4500<\mathrm{I} \leq 6000$ | 0.70 | 1.53 |
| $6000<\mathrm{I} \leq 10000$ | 0.50 | 1.70 |
| $10000<\mathrm{I} \leq 20000$ | 0.30 | 2.00 |
| $20000<\mathrm{I} \leq 50000$ | 0.25 | 2.10 |
| $50000<\mathrm{I}$ | 0.20 | 2.20 |

In case of short circuit tests on Transformers, the peak value of this short circuit current is derived from the formula as stated below. For Transformers, this value of peak short circuit current is determined as per IEC: 60076-5:2006 is as follows [8]:

The amplitude (i) of the first peak of the asymmetrical test current is calculated as follows:

$$
i=I * k * \sqrt{2}
$$

$k$ : factor for the initial offset of the test current
$\sqrt{2}$ - peak to rms value of sinusoidal wave

$$
k * \sqrt{2}-\text { peak factor }
$$

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This peak factor depends upon the DC offset
Where $\mathrm{k}=\left(1+e^{-\left(\phi+\frac{\pi}{2}\right) *\left(\frac{R}{X}\right)} * \sin \phi\right)$
$I_{\text {peak }}=\frac{V}{Z} *\left(1+e^{-\left(\phi+\frac{\pi}{2}\right) *\left(\frac{R}{X}\right)} * \sin \varnothing\right)$
$\emptyset$ - phase angle which is equal to tan $^{-}\left(\frac{X}{R}\right)$ in radians
$e$ - base of natural logarithm
As stated earlier, these short circuit currents are simulated by the testing labs to establish the actual conditions of faults which will be imposed on the equipment during its normal service conditions. The fault current depends on the system impedance.

Authors laboratory simulate this short circuit fault currents which are asymmetrical in nature, based on the needs of relevant product standards and severity as defined by the customer in line with the standards.


Fig. 5 Simplified Circuit of Short-Circuit Testing.

Fig 5. Shows the simplified test circuit diagram of authors laboratory for carrying out the short circuit test on various electrical products as per requirement of IS/IEC standards as well as that of customers, for verifying the performance of equipment under short circuit conditions, which are simulated to replicate the actual service condition of the equipment and its behaviour when a sudden short circuit current is implied on it.

As already discussed in the previous section, that these short circuit currents implied on the test samples are asymmetric in nature (as described in Fig3.), and this asymmetry is basically achieved by using specialized switches, called as Make-Switch or a Fault making device.

Fig 5. Shows that a fault current is generated by a Generator, by varying its excitation to get the desired output from the generator and this fault current travels forward through a closing command given to a master breaker through a STP (Sequential Test Processor), the output of master breaker is fed to a series combination of Reactors (X) and Resistors(R) so as to restrict the value of fault current, as per the requirement of standard and design values as calculated by the manufacturer.

## IV . POINT ON WAVE SWITCHING (PoW) OF MAKE SWITCH

As the short circuit waveforms are asymmetric in nature as described in Fig. 2 this asymmetrical phenomenon occurs because of the inductance / Reactance (X) present in the circuit as shown in Fig.5.

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To achieve these kinds of asymmetric waveforms a specialized device is used along with the STP (Sequential Test Processor) which is called as a point on wave switch (PoW) frequently called as Point on Wave Controller. It is microprocessor-based relay used for controlling switching or shifting operation (ON to OFF \& OFF to ON) of makeswitches used in short circuit testing.

Controlled switching refers to, as an open (OFF) or close (ON) of a make switch at specified location/angle on the voltage waveform. They are also known as synchronous switching controllers (SSC) and can be used as open and close of independent poles of a circuit breaker (IPO) or a Make-switch. Point on wave controller fundamentally harmonize the arbitrary closing (ON)/opening (OFF) input order so that individual or a specific pole of a make switch (MS) get close at predetermined point on reference voltage waveform to get a peak value ( $\mathrm{I}_{\mathrm{pk}}$ ) of a short circuit current (as per Fig.3) on a respective phase of current, either of the one R / Y / B.


Fig. 6 represents the schematic functioning of PoW Controller.

The above schematic (Fig.6) represents the use of PoW controller for switching operation of Make switch. It is evident that the PoW takes the following inputs. When an arbitrary (OFF) opening / (ON) closing command is issued to a Make switch through a control switch, the PoW acquires the instruction from control switch and process it for providing further command to the make switch (MS), it initiates an intentional time lapse between the issue of arbitrary command from control switch to the issue of instruction by the PoW.

In this intentional delay time period, the controller performs mandatory calculations in such a way that Make switch should close at a specific point on the reference voltage waveform. To do so, firstly the Make switch ON-OFF / operating time is examined, then only PoW initiates a command in such a manner that Make switch should close at a target point on, i.e., at voltage zero to get the maximum desired peak in the short circuit current waveform. Refer Fig.7.

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Fig. 7 Functioning of a PoW.

High power laboratories, which are performing these high faults short circuit current testing utilizes make switches along with a PoW controller to get the desired asymmetric current waveforms for ascertaining the performance of equipment under short circuit conditions.

At present the authors laboratory utilizes such high precision make switches along with sequential test processor, STP (incorporating PoW) to achieve the desired asymmetric waveforms as per the requirement of various IS/IEC standards and its magnitude \{Peak short circuit current (Ipk) \}as per the requirement of its design parameters or as specified by the manufacturer.

## V. MAKE SWITCH \& ITS IMPORTANT FEATURES

As per Fig.8, the authors laboratory has newly installed 3Nos. of these make switches from MTSA Techno power, Netherlands, 1 in each phase (R / Y / B) to cater the short circuit testing needs of customer for certification of products as per relevant IS/IEC standards. The most important characteristics of these make switches, to be used in any highpower laboratories, is that, it should be extremely fast in operation i.e., the delay time between issuing of a closing command by PoW controller and final closing of main contacts of the make switch i.e., when the current starts flowing in the power terminals, should be minimum as possible so as to achieve a target point on the voltage waveform to get the desired peak value of current to get a perfect value of asymmetry on the current waveform as per (Fig.3).

The other most important characteristics of these make switches are as follows [10]:

- Pneumatic Driven.
- Air Isolated.
- Accurate timing (Phase-angle).
- Adjustable delay unit.
- Simultaneous switching of all the 3 phases at a time.

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Fig 8. MTSA Make-Switch.
Principal electrical features of MTSA make-switches are as follows:

- Rated Voltage: 24 kV .
- Nominal Frequency: $50-60 \mathrm{~Hz}$.
- Continuous Rated Current(A)rms: 7500 $\mathrm{A}_{\text {rms }}$
- Rated Short Circuit Making Current: 300kA peak $^{\text {(Asymmetrical). }}$
- Rated Short Circuit Making Current: 100kA $\mathrm{frms}_{\text {(Symmetrical). }}^{\text {(St }}$
- Rated Duration of Short Circuit: 100kA for 3 sec .
- Power Frequency voltage withstand: 50 kV (1 minute).
- Impulse Voltage withstand ( $\mathbf{k V}_{\text {peak }}$ ): 125 kV .
- Closing Time: < 8ms.
- Precision of make-time: $<0.1 \mathrm{~ms}$.
- Required Air pressure for operation: 15-20bars.
- Power Supply: 230V AC, 50Hz.
- Power Consumption (open/close): 200W.

The above-mentioned parameters are an important requisite of the make switches to be used in high fault testing by the High-Power Laboratories, as the tests are performed at a very high value of current and voltages to simulate the actual fault conditions in the field, therefore these make switches should have sufficient capabilities to handle such enormous amount of peak currents and voltages.

As mentioned above these make switches are pneumatic driven or air operated, they require a continuous amount of pneumatic pressure for its perfect operation. These make switches operate (OPEN/CLOSE) by a pneumatic pressure of 15-20 bars. For this, these make switches are provided with an Electro-pneumatic control Cabinets (EPC) (Fig.9), which supply a pneumatic pressure of approx. 15-20bars.

This Electro-pneumatic control cabinets (EPC) consists of Pressure switches for indicating switch positions (close/open), switch ready for closing, status interlocking and controlling main pressure. Moreover, these control
cabinets also incorporate close valve, open valves, service valve, interlock valves, pressure gauges, pressure control valve with gauges and main shut off valve for compressed air (Fig.10).

Pneumatic hoses for controlling of different operations of these make switches are connected to these control cabinets for proper air flow through these valves (Fig.9).

Fig. 10 shows the inside view of electro-pneumatic control cabinets.


3 Nos. MTSA Make-switches of respective phases R/Y/B are provided with Electro-pneumatic control cabinets for its independent as well as simultaneous operation. In high fault testing generally all the 3 phases $(\mathrm{R} / \mathrm{Y} / \mathrm{B})$ are given simultaneous closing commands so as to develop a flow of short circuit current in all the 3 phases simultaneously [10].

All the 3 make switches along with its Electro-pneumatic control cabinets are inter connected with a local control cabinet (LCC) and remote-control cabinets (RCC). The local control cabinets (LCC) are connected to the Electropneumatic control cabinets by means of an electric cable \& Local (LCC) and Remote-Control cabinets (RCC) are connected to each other by means of an OFC (Optical Fibre Cable) for faster signal transfer from one end to another. The local control cabinet is placed in a nearby vicinity of the Make-switches whereas, the remote-control cabinet is placed at TCR (Test Control room) from where the command for closing is issued by the test laboratory for performing the test. (Refer Fig.11).
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Fig. 11 Schematic Overview of Control System.

The Local Control Cabinet (LCC) incorporates controls of all the 3 make switches for its individual or simultaneous operations. Controls on LCC includes Close / Open commands, status signal of make-switches (whether switch is ready for closure or not) and status signals for pneumatic or compressed air pressure for performing basic functional checks on the switches.

Fig. 12 shows the overview of different status signals and command buttons for local operation of the make switches.


Fig. 12 Local Control Cabinet (LCC)

The Remote-control cabinet (RCC) is placed in TCR (Test Control Room) electrically connected along with STP (Sequential Test Processor) to issue a closing command to these make switches by means of an Optical command

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(through OFC). Fig. 13 below shows RCC connected in a STP module from where the close / open command is issued to MTSA make-switches after correction of closing angle, so as to achieve a required asymmetry in output short circuit current waveforms.

(MTSA) Remote Control Cabinet (RCC) incorporated along with STP Module.

Fig. 13 Remote Control Cabinet (RCC) along with STP Module.

## VI. NO-LOAD TIMING TEST OF MAKE-SWITCHES \& ITS SIGNIFICANCE

As discussed in the earlier section, that these newly installed make-switches are being used in commercial short circuit testing by the authors laboratory, to cater the short circuit testing needs of the customer as per their requirement and as per IS/IEC standards. But, before being utilized in the actual testing, NO-LOAD timing of these make switches are being verified by the laboratory against the standard closing time as stated by the manufacturer (MTSA). In this case the standard closing time specified by the manufacturer is $<8.0 \mathrm{~ms}$. So, this closing time is to be verified by the test laboratory so that perfect asymmetry can be achieved by the high-power laboratory before performing the commercial test for the customer.

As discussed in earlier section of this paper, that closing time of the make-switches plays a very important role in achieving the asymmetry of output current waveform (as per Fig.3\&5), because of the PoW (Point on wave switching), which aims at closing the make switch at a pre-defined target point on the voltage waveform as shown in fig. 6 \& 7 respectively.


Fig. 14 STP incorporating a PoW controller at TCR.

The STP (Synchronous Test Processor) located at TCR (Test Control room) issues a closing command, which is corrected after a trial shot taken on the test sample and then after analysing the test waveform a corrected angle / mS (mill-second) command is issued to a make-switch for a perfect zero-closing. Fig. 14 Shows STP (incorporating a PoW) located at TCR (Test Control room), for generating a corrected (mS) CLOSE command to Make-switches.

The No-Load timing test of a Make-Switch is carried out by giving a simultaneous closing command to the Closing coil of all the 3 make-switch R/Y/B. The main power terminals of all the 3 make-switch R/Y/B are connected to a DC source or a battery. Both the commands provided to the make switches are analysed using an oscilloscope or DAS (Data acquisition system). The time difference between the issue of a closing command to the closing coil and final closure of the power terminals of make switches are recorded, which gives actual closing time of make switches as shown below in Fig15.

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Fig. 15 Waveform for Closing Time of Make-Switches ( R / Y / B).

From the above oscillogram it is evident that when a simultaneous closing command is given to the closing coils of all the 3 make-switches (refer waveform Ucl R, Ucl_Y \& Ucl_B) \& an output voltage waveform is generated which is slightly delayed in time than that of the closing command, due to mechanical design constraints of these make switches, the output voltage waveforms are generated due to a DC source or a battery connected to the power terminals of makeswitches.

## VII. RESULTS

On analysing the waveforms, it was found that the closing time of these make-switches comes out to be as follows:

1. R-Phase (Make-Switch): 7.5 milli seconds
2. Y-Phase (Make-Switch): 7.7 milli seconds
3. B-Phase (Make-Switch): 7.7 milli seconds

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From the above-mentioned closing time data, laboratory achieved the make switch closing timings of $7.5 / 7.7$ / 7.7 ms (milli seconds) as against $<8.0 \mathrm{~ms}$ (milli seconds) claimed by the manufacturer, MTSA Netherlands which clearly indicates that these switches are acceptable for use in High Power Laboratory for getting the required asymmetrical current waveforms, which is a basic requisite of high fault testing.

Similarly, opening time test of the said make-switches are also performed in the same manner. In opening time test, the make switches are already kept in an ON condition with a DC source or a battery connected to the power terminals of make-switches and an opening / tripping command is given to the opening coil of make-switches. Both the commands are analysed using an oscilloscope or a DAS (Data Acquisition System).


Fig. 16 Waveform for Opening Time of Make-Switches ( R / Y / B).

On analysing the waveforms, it was found that the opening time of these make-switches comes out to be as follows:

1. R-Phase (Make-Switch): 218.7 milli seconds
2. Y-Phase (Make-Switch): 223.1 milli seconds
3. B-Phase (Make-Switch): 218.3 milli seconds.

After completion of the above tests, trial test is carried out as shown in Fig.5.A trial fault current is generated by a Generator and is fed to these MTSA make switch through Master Breakers and series combination of Reactors (X) and

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Resistors(R), The make switch is also programmed for PoW switching by an STP to get a perfect closure of makeswitch on voltage zero or at a targeted point on the voltage waveform, to achieve highest value or peak value $\left(I_{p k}\right)$ of asymmetrical fault current(as per Fig.3) which is fed to the EUT(Equipment under test).This output fault current is analysed through current measuring shunts which is further analysed or displayed on DAS (Data Acquisition system).The waveforms of asymmetric peaks taken on all the 3 phases $(\mathrm{R} / \mathrm{Y} / \mathrm{B})$ of the output fault current is shown in Fig.17(a) / (b) / (c).


Fig. 17 (a) Asymmetric current peak in R-phase.

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Fig. 17 (b) Asymmetric current peak in Y-phase.

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Fig.17(c) Asymmetric current peak in B-phase.

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After trial test on these make-switches, commercial test was performed using these newly installed make-switches on single phase. The test current for the commercial test was set at 33 kA for 3 seconds, with an initial peak value of short circuit current (Ipk) set to $80 \mathrm{kA}_{\mathrm{p}}$, test was performed on the above said parameters and the resultant waveform is as shown in Fig. 18.


Fig. 18 Asymmetric current waveform for actual test.

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From the above waveform it is clearly evident, that actual test current waveform acquired by the DAS is the exact replica of the waveform as explained by the author in section-III (Fig. 3 \& Fig.5). Hence by the use of these make switches perfect asymmetry can achieved in the output current waveforms so as to simulate the actual fault conditions in the high fault laboratory to access the performance of any switchgear equipment in fault conditions.

## VIII. CONCLUSIONS

It is concluded that short circuit testing plays a very vital role and an important verification tool. It acts as a reliability tool for accessing the performance of any switchgear equipment in actual fault condition in the field. Failures due to the fault currents in field can be analysed in the testing labs, by creating or simulating an intentional short circuit current which is an exact replica of actual fault currents having asymmetric nature. These make- switches installed in high power laboratories plays a vital role in achieving the desired asymmetric peaks which will be imposed on the test equipment, moreover in case of failures or damages due to these peak currents on the test equipment, It can also be analysed by the test labs and the manufacturers so that modifications or R\&D can be done in the design of the switchgear equipment's by the manufacturer in such a way that, equipment can be re-designed and made more capable to handle these enormous value of peak currents during fault conditions in a power system network .

## IX. ACKNOWLEDGEMENT

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