



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 12, Issue 10, October 2023

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.423

 9940 572 462

 6381 907 438

 ijirset@gmail.com

 www.ijirset.com

Cascaded Multilevel DSTATCOM for Power Quality Improvement

M.K.NANDHINI[1], T.RAJKUMAR, M.E.,[2]

PG Student, Dept. of EEE, The Kavery Engineering College, Mecheri, Tamilnadu, India

AP/EEE, Dept. of EEE, The Kavery Engineering College, Mecheri, Tamilnadu, India

ABSTRACT: Variable reactive power compensation of nonlinear and poor power factor loads is an important issue in the modern distribution system. Excessive reactive power demand increases feeder losses and reduces active power flow capability of the distribution system where unbalancing affects the operation of transformers and generators. A Distribution STATIC compensator (DSTATCOM) is a custom power device connected in shunt with the load. DSTATCOM could be used for reactive power compensation and balanced loading in the distribution system. The performance of DSTATCOM depends on the control algorithms used for the extraction of reference current component. SRF is based on CLARK'S and PARK'S transformation in which voltage signals are processed by PLL and current signals are transferred from dq to abc and send to hysteresis based PWM signal generator for firing of switches. The proposed cascaded inverter based DSTATCOM is implemented in MATLAB.

I. INTRODUCTION

Power quality phenomenon include all possible situations in which the waveform of the supply voltage (voltage quality) or load current (current quality) deviate from the sinusoidal waveform for all three phases of a three-phase structure at rated frequency with amplitude corresponding to the rated Root Mean Square (RMS) value.

The adequate range of power quality disturbances covers sudden, short duration variations viz impulsive and oscillatory transients, voltage sags, short interruptions, as well as steady state deviations, such as harmonics and flicker. One can also differentiate, based on the cause, between disturbances associated to the quality of the supply voltage and those interrelated to the quality of the current taken by the load.

Electrical equipment susceptible to power quality or more appropriately to need of power quality would fall within an apparently boundless domain. All electrical devices are prone to failure or breakdown when exposed to one or more power quality problems. The electrical device might be an electric motor, a transformer, a generator, a computer, a printer, communication equipment or a home appliance. All of these devices and others react undesirably to power quality issues, depending on the severity of problems. However, nearly everybody accepts that it is a very important aspect of power systems and electric machinery with direct impacts on efficiency, security and reliability.

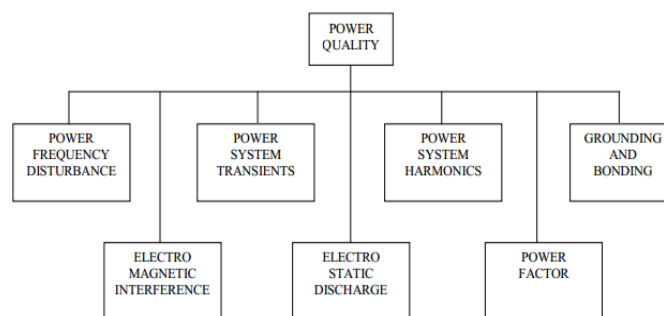


Fig 1: Power Quality Concerns

POWER QUALITY IMPROVEMENT TECHNIQUES

Nonlinear loads generate harmonic currents that can promulgate to other locations in the power system and ultimately return back to the source. Therefore, harmonic current Promulgation produces harmonic voltages throughout the power systems. Many mitigation techniques have been suggested and employed to maintain the harmonic voltages and currents within proposed levels.

1. Design of High power quality equipment
2. Cancellation of Harmonics
3. Dedicated line or transformer,
4. Capacitor banks optimal placement and sizing,
5. Derating of power system devices and
6. Harmonic filters (passive, active and hybrid) and custom power devices such as active power line conditioner (APLC), DVR, DSTATCOM and Unified Power Quality Conditioners.

The DSTATCOM consists of a current-controlled VSI which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor. The transient response of the DSTATCOM is very significant while compensating ac and dc loads. In some of the electric power consumers, such as the telecommunications industry, power-electronics drive applications, etc., there is a constraint for ac as well as dc loads. The telecommunication industry uses several parallel-connected switch-mode rectifiers to support dc bus voltage. Such an arrangement draws nonlinear load currents from the utility. This causes reduced power factor, more losses and less efficiency. Obviously, there are Power Quality issues, such as unbalance, poor power factor, and harmonics produced by telecom equipment in power distribution networks. Therefore, the functionalities of the conventional DSTATCOM should be increased to mitigate the above mentioned PQ problems and to supply the dc loads from its DC Link as well.

II. PROPOSED SYSTEM

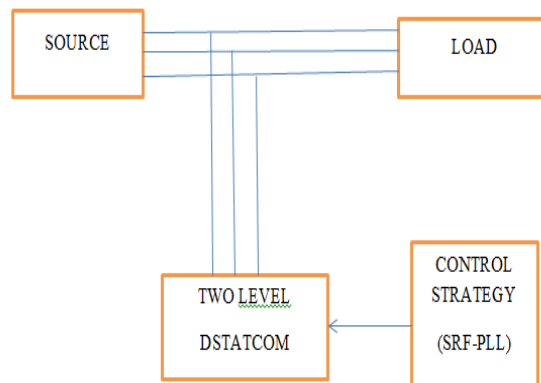


Fig 2: Proposed system

In this work the cascaded two level DSTATCOM with gate control from Synchronous reference frame and Phase locked loop is used. The DSTATCOM consists of a current-controlled VSI which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor. The SRF theory explains about the conversion of abc to dq0 transformation and then from dq0 to abc transformation i.e Clarke and park transformation. The reference from SRF is given to hysteresis controller for PWM generation which is given as gate signal for DSTATCOM.

Need of Power Quality

There is an increased concern of power quality due to the following reasons

1. New-generation loads that uses microprocessor and microcontroller based controls and power electronic devices, are more sensitive to power quality variations than that equipments used in the past.
2. The demand for increased overall power system efficiency resulted in continued growth of devices such as high-efficiency adjustable-speed motor drives and shunt capacitors for power factor correction to reduce losses. This is resulting in increasing harmonic level on power systems and has many people concerned about the future impact on system capabilities.
3. End users have an increased awareness of power quality issues. Utility customers are becoming better informed about such issues as interruptions, sags, and switching transients and are challenging the utilities to improve the quality of power delivered.
4. Most of the networks are interconnected these days. Integrated processes mean that the failure of any component has much more important consequences.

D-STATCOM

When used in low-voltage distribution systems the STATCOM is normally identified as Distribution STATCOM (D-STATCOM). It operates in a similar manner as the STATCOM (FACTS controller), with the active power flow controlled by the angle between the AC system and VSC voltages and the reactive power flow controlled by the difference between the magnitudes of these voltages. As with the STATCOM, the capacitor acts as the energy storage device and its size is chosen based on power ratings, control and harmonics considerations. The D-STATCOM controller continuously monitors the load voltages and currents and determines the amount of compensation required by the AC system for a variety of

BASIC CONFIGURATION OF D-STATCOM

The DSTATCOM is a shunt device. It should therefore be able to regulate the voltage of a bus to which it is connected. The operating principle of a DSTATCOM in this mode has been termed as the DSTATCOM in voltage control mode. This report shows that even though the structure of DSTATCOM used in both current control and voltage control modes is the same, its operating principle is different. In the current control mode it is required to follow a set of reference currents while in the voltage control mode it is required to follow a set of reference voltages. This paper discusses the reference voltage generation scheme and the control of DSTATCOM in the voltage control mode.

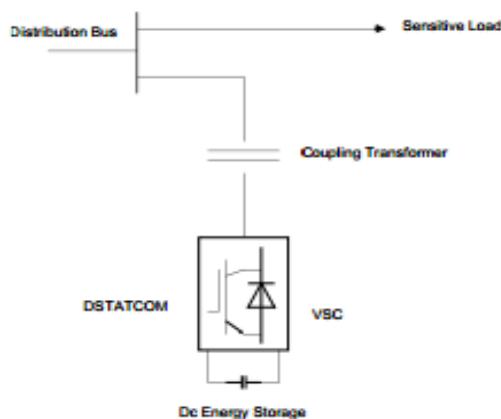


Fig 3: Basic Configuration of D-STATCOM

In its most basic form, the DSTATCOM configuration consists of a VSC, a dc energy storage device, a coupling transformer connected in shunt with the ac system, and associated control circuits. Fig. 1, shows the basic configuration of DSTATCOM.

HYSTERESIS CURRENTCONTROLLER

The hysteresis is basically an instantaneous feedback current control method of PWM where the actual current continually tracks the command current within a specified hysteresis band.

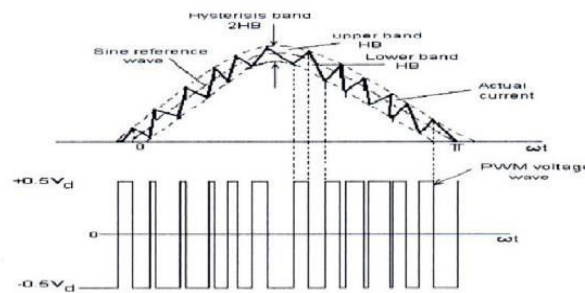


Fig 4: Principle of hysteresis band current control

The Figure above explains the operation principle of HBPWM for a half bridge inverter. The control circuit generates the sine reference current wave of desired magnitude and frequency, and it is compared with the actual phase current wave. As the current exceeds a prescribed hysteresis band, the upper switch in the half-bridge is turned off and the lower switch is turned on. As a result the output voltage transitions from +0.5V to -0.5V, and the current starts to decay. As the current crosses the lower band limit, the lower switch is turned off and the upper switch is turned on. The actual current wave is thus forced to track the sine reference wave within the hysteresis band by back- and-forth (or bang-bang) switching of the upper and lower switches. The inverter then essentially becomes a current source with peak to peak current ripple, which is controlled within the hysteresis band irrespective of v_d fluctuation. The hysteresis band inverter control method is shown in the Figure below. The inputs to the HBPWM controller are three phase current errors and the outputs are the switching patterns to the PWM inverter. K in the Figure represents the normalization factor and is used for the purpose of scaling the current error input to the HBPWM controller. PS is the pulse separation circuit for the separation of pulses to the IGBTs in the upper and lower leg of the inverter.

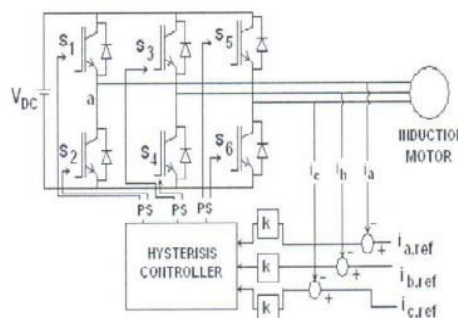


Fig 5: Conventional hysteresis inverter control method

The hysteresis current controller gives output pulses to the inverter according to [14];
 $|i_{m,ref} - i_m| < \epsilon$ keeps the output pulse at the same state, $i_{ref} - i_m > \epsilon$ let output pulse = 1 (high). , $i_{ref} - i_m < -\epsilon$, let output pulse = 0 (low), where $m = a, b, c$ phase meanwhile ϵ is the hysteresis band.

The algorithm for this scheme is:

$$i_{m,ref}(t) = i_{m,ref} \sin(\omega t)$$

$$\text{Upper band } i_u = i_{m,ref}(t) + \Delta i \quad (2.2)$$

$$\text{Lower band } i_l = i_{m,ref}(t) - \Delta i \quad (2.3)$$

Where Δi = hysteresis band limit.

If $i_m > i_u$, $V_{mo} = -V_{dc} / 2$ (2.4)

If $i_m < i_u$, $V_{mo} = V_{dc} / 2$ (2.5)

Else, maintain the same state. Where $m = a, b, c$ phases, i is load current and V_{dc} is the link voltage of the inverter.

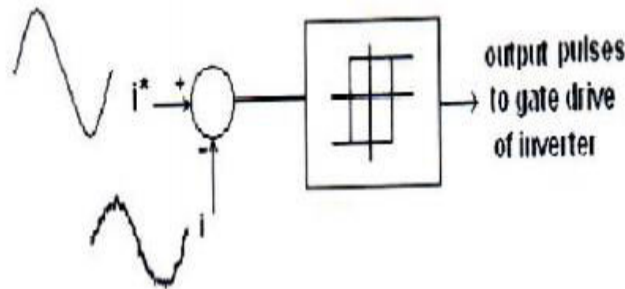


Fig 6: Control block diagram for HBPWM

SYNCHRONOUS REFERENCE FRAME(SRF)

Principle of Synchronous Reference Frame Method

The Synchronous Reference Frame method (SRF) is based on the fact that harmonics change their frequency in a rotating reference frame, and so they are better isolated with high pass filters. In this method the measured load currents are transformed into the rotating reference frame (d-q frame) that is synchronously rotating at the line voltage frequency using (1) and (2)

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{pmatrix} \cos\omega_s t & -\sin\omega_s t \\ \sin\omega_s t & \cos\omega_s t \end{pmatrix} \begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix}$$

The line frequency components of the load currents become DC quantities and the harmonic components are frequency shifted by ω_s in the d-q reference frame. A high pass filter in the d-q frame, with a cutoff at the line frequency can be used to extract the DC components. If the phase of the d-axis current is locked to the phase voltage, e_a , of the a-b-c coordinates with a phase locked loop (PLL), and then the component represents the fundamental real current and represents the fundamental reactive component. By subtracting these quantities from I_{ld} and I_{lq} , the harmonic content is obtained as shown in (3) and (4).

$$i_{dh} = I_{ld} - I_d^{dc}$$

$$i_{qh} = I_{lq} - I_q^{dc}$$

These quantities can then be used to develop the compensating quantities for the active filter by transforming back to α - β coordinates and then to a-b-c coordinates using (5) and an inverse transformation (6).

$$\begin{bmatrix} i_{\alpha} \\ i_{\beta} \end{bmatrix} = \begin{pmatrix} \cos\omega_s t & -\sin\omega_s t \\ \sin\omega_s t & \cos\omega_s t \end{pmatrix} \begin{bmatrix} i_{dh} \\ i_{qh} \end{bmatrix}$$

The compensating line currents can be obtained using

$$\begin{bmatrix} i_{ac}^* \\ i_{bc}^* \\ i_{cc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i_{ca}^* \\ i_{c\beta}^* \end{bmatrix}$$

One of the most important characteristics of this method is that the reference currents are derived directly from the real load currents without considering the source voltages. The generation of the reference signals is not affected by voltage unbalance or voltage distortion, therefore increasing the compensation robustness and performance. Reference frame rotates synchronous with fundamental currents. Therefore, time variant currents with fundamental frequencies would be constant after transformation. However, harmonics with different speeds remain time variant in this frame. Thus, currents would be separated simultaneously to DC and AC parts. AC part of d axis and whole current in q axis are used for harmonics elimination and VAR compensation. Zero current is produced due to a three-phase voltage imbalance or waveform distortions which have not been considered in this paper. Finally, compensatory currents are determined by adverse Park transformation on d and q axis to be injected to the network after tracing and reconstruction.

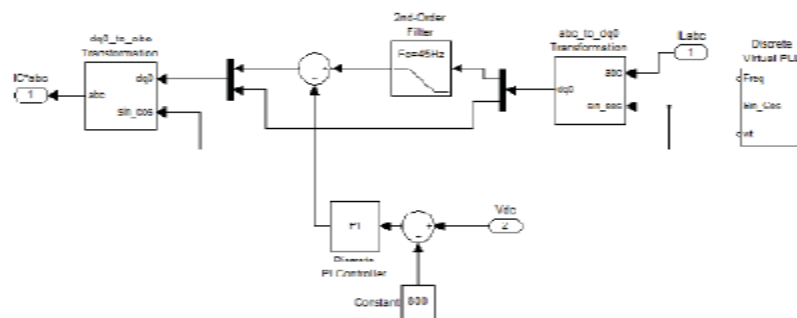


Fig 7: Simulation model of SRF theory

III. MATLAB SIMULATION

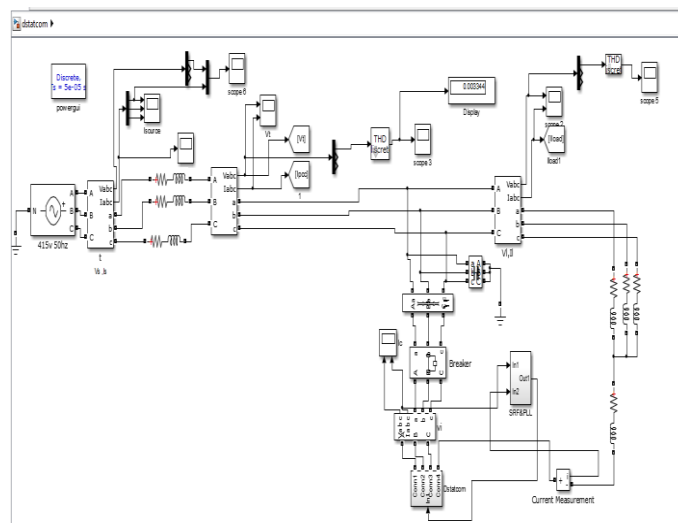


Fig 8: Cascaded two level DSTATCOM

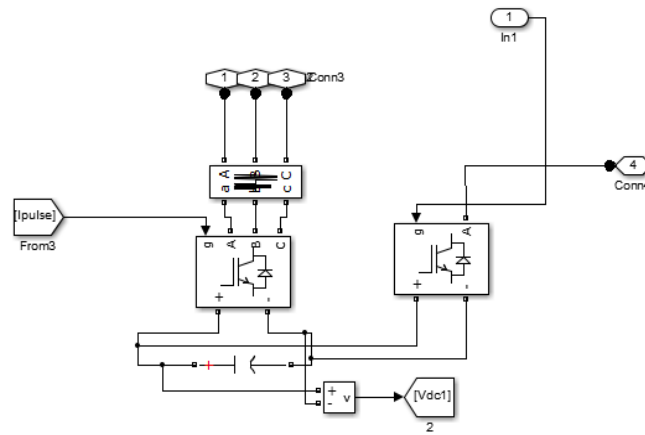


Fig 9: Simulation diagram of DSTATCOM

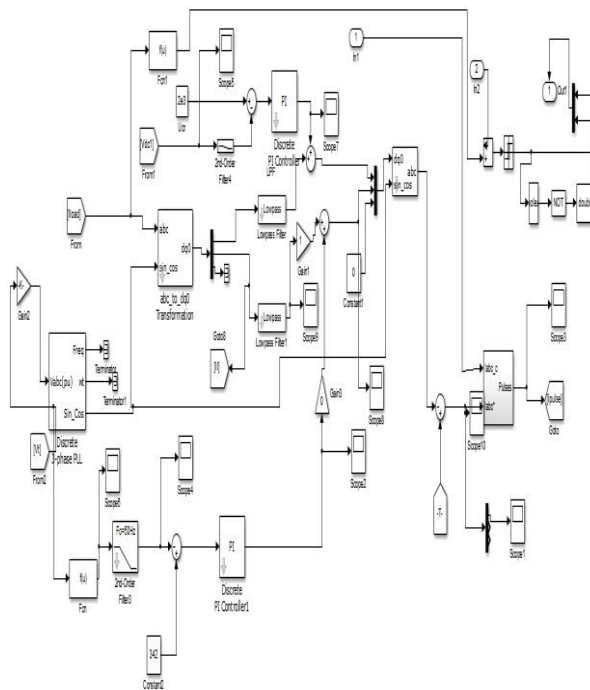


Fig 10: Simulation diagram of SRF and PLL

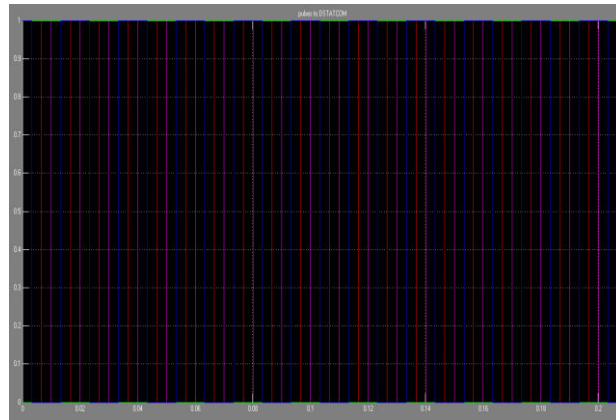


Fig 11: Pulses to DSTATCOM

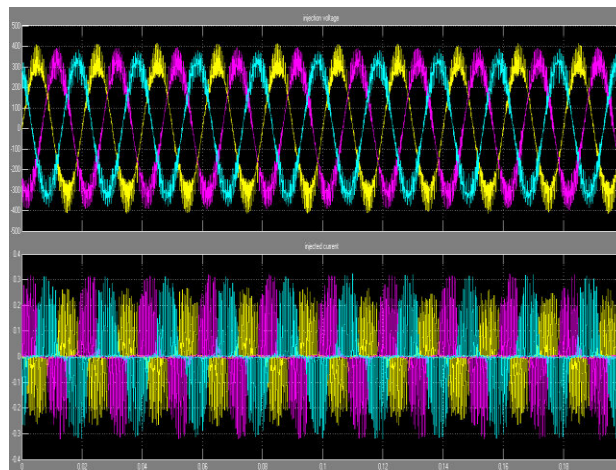


Fig 12: DSTATCOM Injecting voltage and current

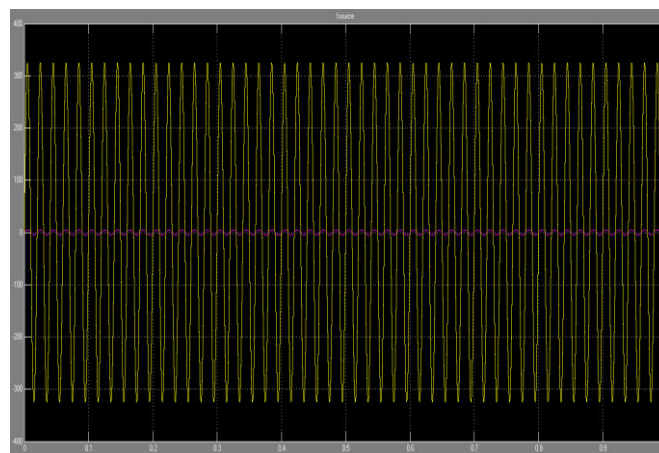


Fig 13: Source voltage and current

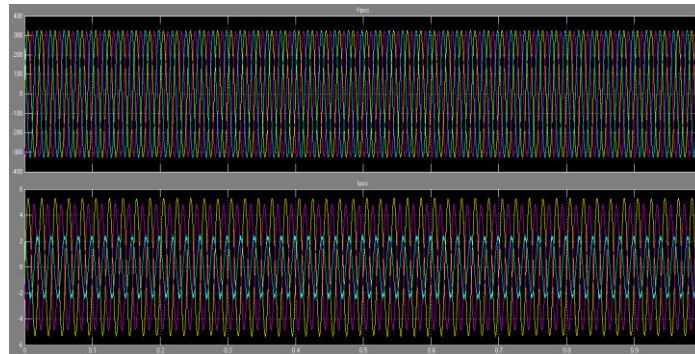


Fig 14: Point of common coupling voltage and current

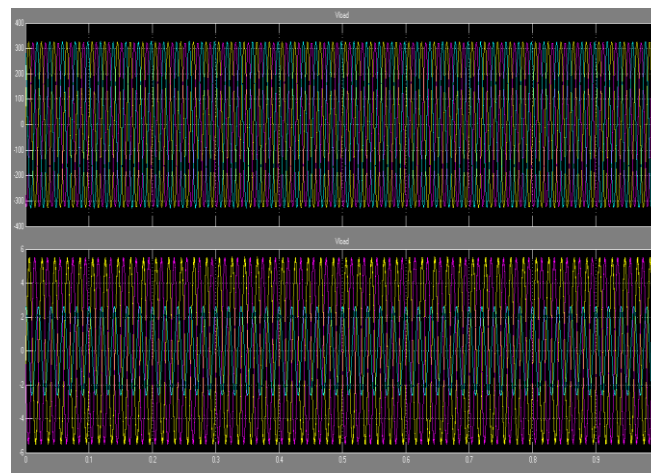


Fig 15: Load voltage and current

IV. CONCLUSION

A simple varcompensating scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation under balanced and unbalanced voltage conditions. When used in low voltage distribution system, the static compensator (STATCOM) is identified as Distribution STATCOM (DSTATCOM). This work evaluates power balance control algorithm for extracting reference source currents for voltage regulation at PCC (Point of Common Coupling) for DSTATCOM. The voltage source converter (VSC) is used with DC link capacitor as a DSTATCOM. The SRF theory is used to generate the reference voltage required to compensate the voltage sag/swell. This technique converts coordinates from a-b-c stationary coordinate system to o-d-q rotating coordinate system. Signals are converted in o-d-q frame because it is easy to control and process on signals in d-q frame. Then again these signals are converted in a-b-c coordinate system. In the proposed work the DSTATCOM for reactive power compensation and power factor correction with Improve power factor, Reduces THD is used and simulated using MATLAB.

REFERENCES

1. H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V 10-kVA laboratory model," IEEE Trans. Ind. Appl., vol. 44, no. 2, pp. 672–680, Mar./Apr. 2008.
2. Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, "Small signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based STATCOM," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2259–2269, Jun. 2009.

3. D. Kalyankumar, Dr. V. Kirubakaran, “D- STATCOM Based Voltage Regulation and Harmonic Damping”, International Journal of Computer Applications (0975 – 8887), Volume 7– No.4, September 2010.
4. H. P.MohammadiandM.T. Bina, “A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters,” IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1534–1545, May 2011.
5. Bhattacharya Sourabh, “Applications Of DSTATCOM Using MATLAB/Simulation In Power System” ISSN 2277 – 2502, Vol. 1(ISC-2011), 430-433,2012.
6. AlpeshMahyavanshi, M. A. Mulla, R. Chudamani,” Reactive Power Compensation by Controlling theDSTATCOM”ISSN 2250-2459, Volume 2, Issue 11, November 2012.
7. AmalaKadari,K.ravisankar,DurgamKumaraswamy, “Synchronous-Reference – Frame based control method for UPQC under different load conditions”,ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.418-429.
8. RahulPawar, Dilip G. Borse, Sawata R. Deore, GovindKedar,SantoshKaware, “Simulation of cascaded h-bridge multilevel inverter based DSTATCOM for power quality improvement withswitching modulation index”, 7th IRF International Conference, 27th April-2014, Pune, India, ISBN: 978-93-84209-09-486.



INNO SPACE
SJIF Scientific Journal Impact Factor
Impact Factor: 8.423



ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

9940 572 462 **6381 907 438** **ijirset@gmail.com**



www.ijirset.com

Scan to save the contact details