



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 12, Issue 10, October 2023

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.423

9940 572 462

6381 907 438

ijirset@gmail.com

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Multi-level Inverter Topology with Variable Load Condition: A Review

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ABSTRACT: Multilevel inverters (MLIs) have been widely accepted as a potential solution for high-efficiency electric power-electronic conversion systems by both research and industry community. The inherent features of MLIs like reduced dv/dt , high-quality output waveform, lower switching frequency, etc., are the key reasons for the usage of MLIs in a variety of fields including motor drives, renewable energy sources integration, locomotives, to name a few. The basic MLIs are cascaded H-bridge (CHB), neutral point clamped, and flying capacitor inverters. The topology does not use an input bridge rectifier, common in similar applications. The current in the two input inductors can therefore, flow in both directions. Consequently, the different topology equally distributes the current by the four-bridge transistors that provide four input parallel boost power factor correctors (PFCs). The use of the four bridges permitting the accurate simultaneous regulation of output voltage and input current is hereby described.

KEYWORDS: Multi-level Inverter, PWM, Boost Factor

I. INTRODUCTION

In modern technology, power electronics and processor plays a vital role in the field of motor control, light control, heat control, power supplies, vehicle system, HVDC, FACTS and renewable applications. The philosophy focuses on preserving the energy and meeting the power demand accurately and the power modulator pertaining to inverter / converter technology fulfills the requirements and this attracts the researchers to explore in the inverter field. The above-mentioned applications work in the range of medium power, high power at a higher voltage. With the help of semiconductor device technology, power converters are to be designed with higher operating voltage. As a single device fails to support such high voltages, a number of devices need to connect in series to meet the voltage rating. Another challenge in the industrial sector is the requirement and maintenance of the sinusoidal power supply with variable voltage and frequency. The above demerits are overcome by the introduction of Inverters. The series connected switches in the inverters and through control mechanism, the voltage stress with respect to high voltage rating is shared among the series switches and also the losses are minimized. Due to advantage of minimum losses, inverters is also used for medium voltage applications. The classical square wave inverter operating at higher voltage introduces the dominant harmonics, thereby the performance on the load side and on the front end of the inverter has a large impact and the performance is affected. Though the solution is sought through the passive filters, the loss are increased and occupies more space. The alternative path is provided by Multilevel Inverters (MLI) [1, 2]. MLI generates sinusoidal voltage waveform in the form voltage steps through switching sequence. The other advantages of MLI are reduced electromagnetic interference, reduced current distortion, good quality voltage waveform, good current waveform. The basic types of MLI are neutral point clamped MLI, flying capacitor MLI and cascaded H- bridge MLI. To synthesize nearly sinusoidal voltage, higher number of levels needs to be generated with the help of more number of switches, more number of sources and more number of gate drivers [3, 4]. Due to this, the efficiency decreases as more number of switches is utilized in the conduction path.

II. LITERATURE REVIEW

Theertha K. P. et al. [1], the presentation of a five level single stage trans-formerless lift inverter for matrix tied activity is examined in this work. This seven switch conspire with an increase of two is a changed rendition of HERIC

geography with changed diodes and drifting capacitors to accomplish supporting element. Three unique PWM plans are viewed as reasonable for this framework to give steady well known mode voltage to lessen spillage current which is an additional benefit. To enable the utilization of sustainable assets, sun oriented PV with MPPT is additionally utilized. Recreation based investigation is finished to evaluate the presentation of the Stage locked loop(PLL) conspire with relative integral(PI) control for the matrix tied activity. THD is viewed as good. The plan is viewed more productive than traditional inverters since there is no inward energy misfortunes and additional part costs.

D. Vijayakumar et al. [2], this paper presents a two-stage help five-level T-Type inverter for PV applications. The proposed model is worked with the mixes of three-level lift converter and five-level T-Type inverter for single-stage framework. The total situation of the lift converter and T-Type inverter for level age is introduced. The presentation of the proposed model was assessed in a MATLAB/Simulink climate for an extensive variety of information voltage changes as well as burden changes. The significance of the level age as far as %THD has likewise been talked about for various regulation records. Besides, an examination is likewise made to feature the benefits of the proposed model opposite other five-level inverter geographies.

Sangeeta Kumari et al. [3], exchanged capacitor based staggered inverters (MLIs) definitely stand out enough to be noticed inferable from their capacity to voltage supporting and self-adjusting nature of SCs. In any case, these geographies experience because of high current spikes coming about because of the equal association of SCs with dc source. This article presents a five-level (5L) SC-based inverter to take care of this issue while rationing the useful highlights of SCs. The proposed geography has a devoted circuit involving one inductor and two power switches for guaranteeing a delicate charging of the SC. The activity of the proposed geography is itemized. To validate the benefits of the proposed 5L geography, it has been completely contrasted and other existing SC-MLIs geographies. The proposed geography is confirmed under both the consistent and dynamic stacking conditions, and the outcomes are introduced.

M. Abarzadeh et al. [4], in this work, the near-state pulse width modulation (NSPWM), adjusted to be utilized as a part of dual-voltage source inverter (VSI) fed open-end load, is acquainted essentially pointing with obviously limit the voltage add up to harmonic distortion (THD). Inside the framework of the proposed strategy, the active time of pulses at the second inverter is moderately balanced inside switching interim (contrasted with the principal VSI). The phase voltage harmonics are detailed for dual-inverter regulated by NSPWM; at that point, ideal change is distinguished by means of a three-dimensional bend of phase voltage THD versus modulation file (MI) and phase edge displacement (PAD). Because of the restriction of MI in NSPWM, the coveted yield voltage is orchestrated with altering MI as well as PAD between references of two VSIs. Moreover, NSPWM naturally exploits better productivity contrasted with traditional space vector modulation because of switching just two phases inside an interim (by clipping one phase to positive/negative dc-rail). The dual-VSI provided by two isolated dc sources is amassed in the lab to tentatively assess the THD diminishment highlight of the proposed technique; additionally, the simulation comes about acquired by methods for a MATLAB/Simulink condition indicates close concurrence with exploratory information.

Y. P. Siwakoti et al. [5], in this investigation, the near-state pulsewidth modulation (NSPWM), adjusted to be actualized in dual-voltage-source inverter (VSI) fed open-end engine, is proposed with the point of relieving low-arrange harmonics (which prompt current aggregate harmonic distortion (THD) minimization). The accompanying two proposed techniques are examined in detail: 1) settling phase edge displacement (PAD) between two VSIs to 120° while altering the modulation record (MI); and 2) settling MI to the foreordained esteem (wherein low-arrange harmonics are profoundly relieved) while modifying PAD. Besides, the proposed approaches improve effectiveness by restricting the quantity of replacements inside the switching interim. The examination likewise displays the numerical approaches to accurately decide low-arrange harmonic segments and switching losses for dual-VSI structure. The exploratory setup, including dual-VSI and open-end induction engine, is collected in the lab to assess execution of the proposed technique. At long last, the simulation comes about, completed in the MATLAB/Simulink condition, are observed to be in close concurrence with exploratory information.

A. K. Yadav et al. [6], in this examination work, angular modulation list (AMI) actualized through an altered space vector modulation for the dual voltage source inverters (VSI) is proposed with the fundamentally meaning to lessen switching losses. The coveted voltage across the load is blended by applying suitable phase-point displacement between space vector references. The proposed approach maintains a strategic distance from the utilization of a dc/dc boost converter (which forces loss and weight/value punishment to copy the dc-connect voltage) and results to be especially appropriate for electrical/mixture vehicle applications. In particular, the use of sparing energy to continue

driving has been distinguished as real concern. Thus, this work centers around the system to improve proficiency. The standards of the proposed controlling strategy and switching loss, which is decreased at any rate by half, are hypothetically assessed. This work proposes a spearheading scientific approach to effectively decide add up to harmonic distortion (THD) estimation of the voltage/current for the dual-VSI structure. Moreover, simulation and exploratory outcomes demonstrate that the proposed technique safeguards benefits as far as normal mode voltage, THD of the voltage, and switching loss decrease. The dual-VSI model providing 1.5-kW induction engine is gathered in the research center to tentatively assess execution of the proposed technique. Likewise, the simulation comes about helped out through MATLAB/Simulink condition are given to affirm execution of this simple to-actualize and high-proficient technique.

W. Li et al. [7], a four-level five-phase open-end winding (OeW) drive topology is presented in this investigation. The drive involves a five-phase induction machine with open-end stator windings, provided utilizing two-level voltage-source inverters with isolated and unequal dc-interface voltages, in the proportion 2 : 1. The topology offers the benefits of a measured structure with less semiconductor segments and has a more noteworthy potential for fault tolerance, as contrasted and a comparable single-sided four-level drive. Because of the extensive number of switching states, advancement of a reasonable space vector pulsewidth-modulation (PWM) strategy can be testing. Subsequently, this work looks at the execution of two-level-moved transporter based PWM strategies. The impact of dead time on the drive execution is talked about, and it is demonstrated that synchronous PWM switching of the two inverters can prompt debased yield phase voltage waveforms. Nitty gritty investigation of this wonder is introduced, an answer is proposed, and the changed modulation systems are joined in a trial setup, at first in conjunction with V/f control. Once the verification of idea has been given, full field-situated control is executed in this OeW drive topology out of the blue; definite exploratory testing is directed, and comes about are accounted for.

III. MULTI LEVEL INVERTER

Figure 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM. Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [5, 6]:

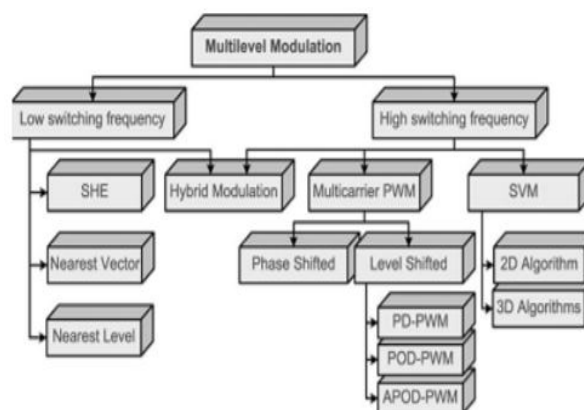


Figure 1: Multilevel converter modulation methods

Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [7]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [8, 9]. Figure 2 shows the LS-PWM carrier arrangements.

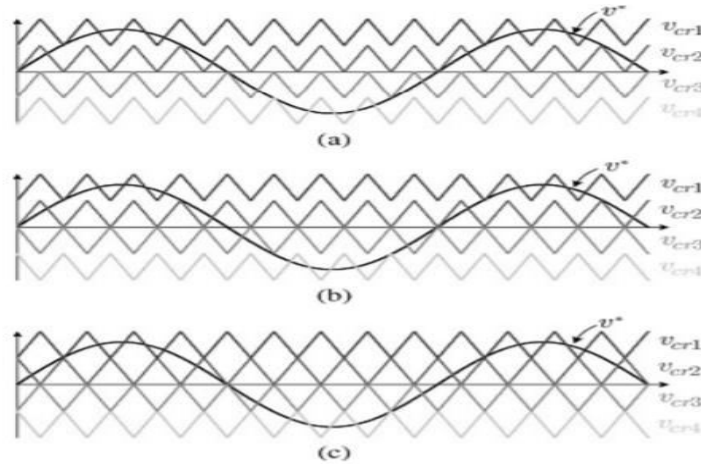


Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

Phase Shift Pulse Width Modulation

PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width [10]. There is one beat of settled extent in each PWM period. In any case, the width of the beats changes from period to period as indicated by a regulating signal. At the point when a PWM flag is connected to the entryway of a power transistor, it causes the turn on and kills interims of the transistor to change starting with one PWM period then onto the next PWM period as indicated by the same regulating signal and thus working of converter begins. The recurrence of a PWM flag must be substantially higher than that of the regulating signal, the major recurrence, with the end goal that the vitality conveyed to the heap depends generally on the tweaking signal. The control of yield voltage is done utilizing beat width balance [11, 12].

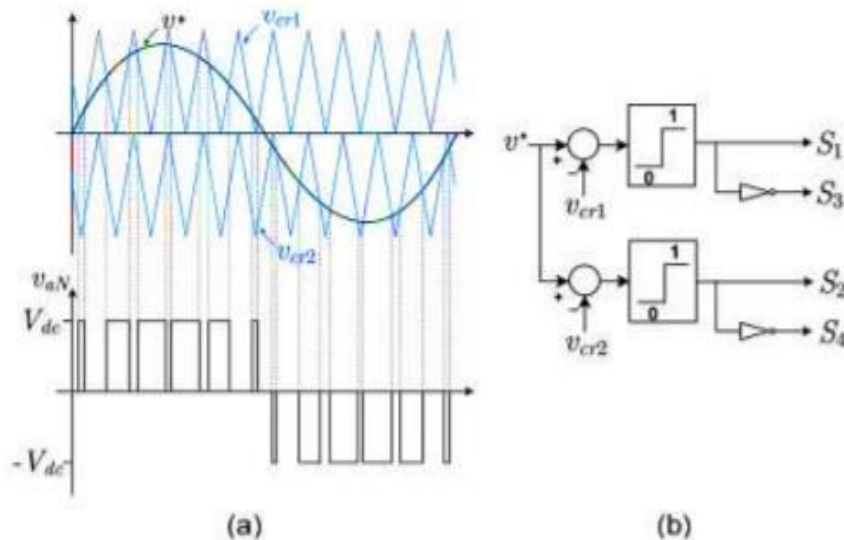


Figure 3: Phase Shift PWM

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by 90° . Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal [13].

Total Harmonic Distortion

The total harmonic distortion (THD or THDi) is a measurement of the harmonic distortion present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Distortion factor, a closely related term, is sometimes used as a synonym.

In audio systems, lower distortion means the components in a loudspeaker, amplifier or microphone or other equipment produce a more accurate reproduction of an audio recording.

In radio communications, devices with lower THD tend to produce less unintentional interference with other electronic devices. Since harmonic distortion tends to widen the frequency spectrum of the output emissions from a device by adding signals at multiples of the input frequency, devices with high THD are less suitable in applications such as spectrum sharing and spectrum sensing [14, 15].

In power systems, lower THD implies lower peak currents, less heating, lower electromagnetic emissions, and less core loss in motors.

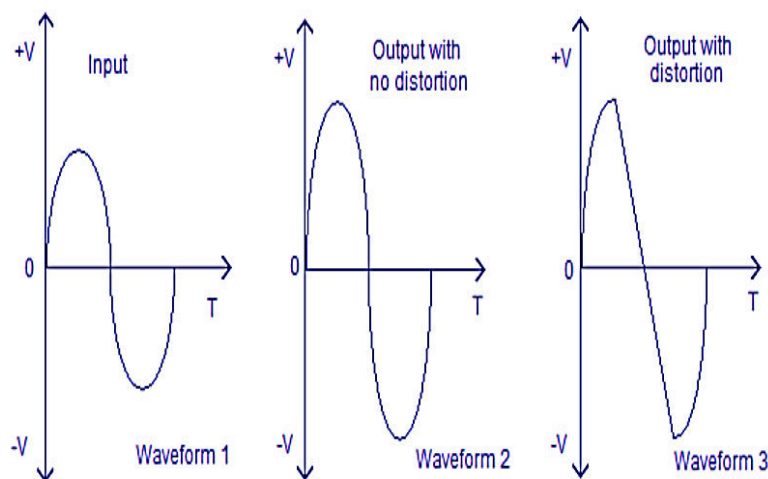


Figure 4: Output Waveform of Distortion

IV. CONCLUSION

The presented research work has been focused on the construction of variable amplitude sinusoidal voltage using the different topologies. The first effort has been related to the development of new MLI topology using diodes and switching devices under symmetric and asymmetric mode. The advantage of the topology articulates any desired voltage level with a reduced total number of devices and sources over basic and similar topology. A boost type 13L inverter with a voltage gain of six is review in this paper. The devised topology consists of 13 switches, two diodes, and three capacitors. The voltages of the SC are naturally balanced owing to the self-balancing ability of the proposed topology. A simple series-parallel based technique is used to maintain the SC voltages without the need for any voltage/current sensors. The operating principle and the simple modulation method were discussed. The operability and feasibility of the proposed topology are validated through detailed experimental studies and the results are presented.

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