



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 13, Issue 4, April 2024

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.423

9940 572 462

6381 907 438

ijrset@gmail.com

www.ijrset.com

High Speed Gate Level Synchronous Full Adder Designs

V. Shanmuka Srinivas, V. Yugandhar Reddy, P. Bhanu Prakash Reddy, Y. Raghupathi Naidu,
Jaffar Ali Syed

B. Tech student, Dept. of ECE, Annamacharya Institute of Technology & Sciences, Kadapa, India

B. Tech student, Dept. of ECE, Annamacharya Institute of Technology & Sciences, Kadapa, India

B. Tech student, Dept. of ECE, Annamacharya Institute of Technology & Sciences, Kadapa, India

B. Tech student, Dept. of ECE, Annamacharya Institute of Technology & Sciences, Kadapa, India

Assistant Professor, Dept. of ECE, Annamacharya Institute of Technology & Sciences, Kadapa, India.

ABSTRACT: Addition forms the basis of digital computer systems. Three novel gate level full adder designs, based on the elements of a standard cell library are presented in this work: one design involving XNOR and multiplexer gates (XNM), another design utilizing XNOR, AND, Inverter, multiplexer and complex gates (XNAIMC) and the third design incorporating XOR, AND and complex gates (XAC). Comparisons have been performed with many other existing gate level full adder realizations. Based on extensive simulations with a 32-bit carry-ripple adder implementation; targeting three process, voltage and temperature (PVT) corners of the high speed (low V_t) 65nm STMicroelectronics CMOS process, it was found that the XAC based full adder is found to be delay efficient compared to all its gate level counterparts, even in comparison with the full adder cell available in the library. The XNM based full adder is found to be area efficient, while the XNAIMC based full adder offers a slight compromise with respect to speed and area over the other two proposed adders.

I. INTRODUCTION

A binary full adder is often found in the critical path of microprocessor and digital signal processor data paths, as they are fundamental to almost all arithmetic operations. It is the core module used for many essential operations like multiplication, division and addresses computation for cache or memory accesses and is usually present in the arithmetic logic unit and floating-point units. Hence, their speed optimization carries significant potential for high performance applications.

A 1-bit full adder module basically comprises of three input bits (say, a , b and cin) and produces two outputs (say, sum and $cout$), where ' sum ' refers to the summation of the two input bits, ' a ' and ' b ', and cin is the carry input to this stage from a preceding stage. The overflow carry output from this stage is labeled as ' $cout$ '.

Many efficient full custom transistor level solutions for full adder functionality have been proposed in the literature [1] – [10], optimizing any or all of the design metrics viz. speed, power and area. In this paper, our primary focus is on realizing high performance full adder functionality using readily available off-the-shelf components of a standard cell library [11]. Hence, our approach is semi-custom rather than being full custom. This article primarily focuses on the novel design of full adders at the logic level and also highlights a comparison with many other existing gate level solutions, from performance and area perspectives. The inferences from this work may be used for further improvement of full adder designs at the transistor level. Apart from this, this article is also intended to provide pedagogical value addition.

The remaining part of this paper is organized as follows. Section 2 describes the various existing gate level realizations of a 1-bit binary full adder. The three newly proposed full adder designs are mentioned in section 3. Section 4 gives details about the simulation mechanism and results obtained. Finally, we conclude in the next section.

II. LITERATURE SURVEY

STMicroelectronics CORE65LPLVT_1.10V Version 4.1 Standard Cell Library, User Manual and Databook, July 2006.

C.Senthilpari, A.K. Singh and K. Diwakar, Design of A Low-Power, High-Performance, 8×8 Bit Multiplier Using A Shannon-Based Adder Cell, Microelectronics Journal, Vol. 39, No. 5, May 2008, pp. 812-821.

S. Goel, A. Kumar and M.A. Bayoumi, Design of Robust, Energy-Efficient Full Adders for Deep Sub micrometer Design Using Hybrid CMOS Logic Style, IEEE Trans. on VLSI Systems, Vol. 14, No. 12, December 2006, pp. 1309-132.

Y. Jiang, A. Al-Sheraidah, Y. Wang, E. Sha and J.-G. Chung, a Novel Multiplexer-Based Low-Power Full Adder, IEEE Trans. on Circuits and Systems – II: Express Briefs, Vol. 51, No. 7, July 2004, pp. 345-348.

III. PROPOSED METHOD

PROPOSED SYSTEM

This study introduces three distinct full adder designs. The initial design utilizes exclusively XNOR gates and 2:1 multiplexers (MUXes), with one of the two non-inverting 2:1 MUXes featuring an inverted input. This configuration is illustrated in fig and is referred to as the XNM-based full adder. The second design incorporates XNOR, AND, NOT, an inverted input 2:1 MUX, and complex gates, as depicted in fig, and is known as the XNAIMC-based full adder. The complex gate utilized is the AO12 cell, which executes the function $f = xy + z$, where 'x' and 'y' are the inputs to the AND logic, and 'z' is the separate input to the OR logic. The final adder design is an enhancement of the full adder design discussed, characterized by the substitution of the AND gate in the second half adder module and the OR gate related to the carry output with a single complex gate, the AO12 cell.

Fig 4.1: Proposed XNM based full adder

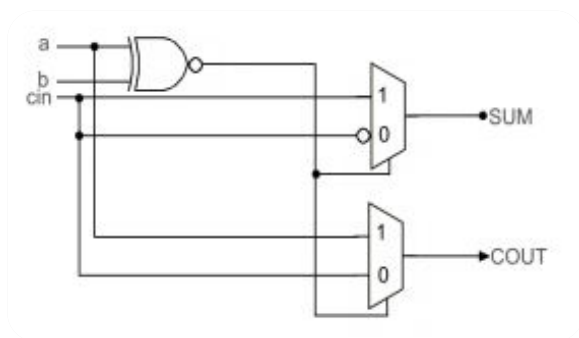


Fig 4.2: Proposed XNAIMC based full adder

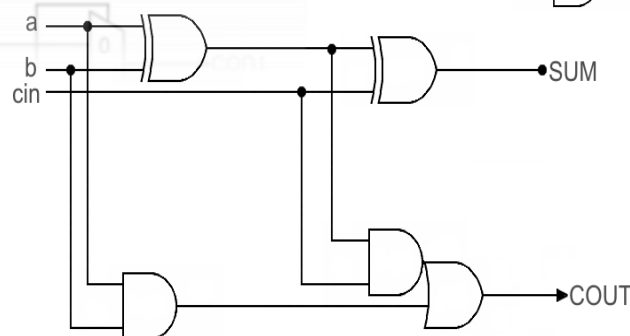
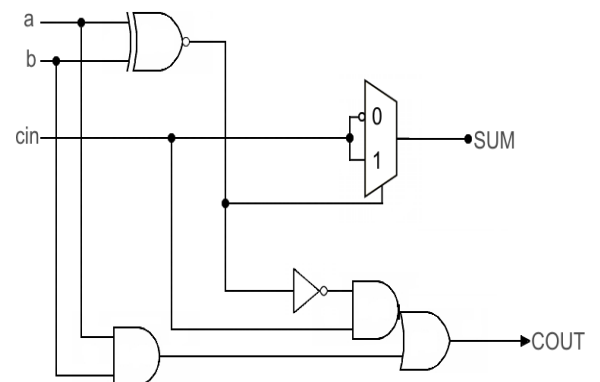


Fig 4.3: Proposed XAC based full adder

- This study emphasizes the crucial role of addition in digital computer systems and introduces three innovative gate-level full adder designs. These designs are crafted using components from a standard cell library:
- The first design utilizes XNOR and multiplexer gates (XNM).
- The second design integrates XNOR, AND, Inverter, multiplexer, and complex gates (XNAIMC).
- The third design employs XOR, AND, and complex gates (XAC).

These designs are compared with numerous existing gate-level full adder implementations. Through comprehensive simulations with a 32-bit carry-ripple adder implementation, targeting three process, voltage, and temperature (PVT) corners of the high-speed (low Vt) 65nm STMicroelectronics CMOS process, it was determined that the XAC-based full adder exhibits superior delay efficiency compared to all other gate-level counterparts, including the full adder cell from the library. The XNM-based full adder was identified as area-efficient, whereas the XNAIMC-based full adder showed a moderate balance between speed and area efficiency compared to the other two designs.

IV. ADVANTAGES

1. **Improved Performance:** High-speed gate-level synchronous full adder designs can perform addition operations quickly, reducing overall latency in digital systems. This is crucial in applications such as high-speed data processing, signal processing, and digital communication systems where rapid computation is essential.
2. **Reduced Propagation Delay:** These designs are optimized to minimize propagation delay through the circuitry, allowing data to propagate through the adder more quickly. This results in faster operation and improved overall system performance.
3. **Enhanced Throughput:** By minimizing propagation delay and maximizing operating speed, high-speed gate-level synchronous full adder designs can process a higher number of operations per unit time, leading to increased throughput in digital systems.
4. **Lower Power Consumption:** While not always the case, efficient high-speed designs can often achieve lower power consumption compared to slower alternatives. This can be advantageous in battery-powered devices or applications where power efficiency is critical.
5. **Compact Design:** High-speed gate-level synchronous full adder designs are often optimized for area efficiency, resulting in compact layouts that occupy less silicon real estate on integrated circuits. This is beneficial for dense designs with limited space constraints.
6. **Compatibility with High-Speed Interfaces:** In applications involving high-speed interfaces such as DDR memory interfaces, PCIe, or Ethernet, having a high-speed adder design ensures compatibility with the data rates and timing requirements of these interfaces.
7. **Reduced Clock Skew:** Synchronous designs synchronize operations to a clock signal, which helps to reduce clock skew and ensure that all parts of the circuit operate in unison. This results in more predictable and reliable behavior, especially in high-speed systems.
8. **Ease of Integration:** High-speed gate-level synchronous full adder designs can be easily integrated into larger digital systems, allowing for seamless integration with other components and subsystems.

V. SOFTWARE

Tanner EDA (Electronic Design Automation) is a suite of software tools primarily used for the design and simulation of integrated circuits (ICs) and other electronic systems. It's developed by Tanner Research, Inc., which was acquired by Mentor Graphics, a Siemens business, in 2015. The tools provided by Tanner EDA cater to various stages of the IC design process, including schematic capture, simulation, layout, and verification.

Here are some key features and components of Tanner EDA:

1. **Schematic Capture:** Tanner EDA offers tools for creating electronic circuit schematics, where designers can draw and connect electronic components such as resistors, capacitors, transistors, and integrated circuits.
2. **Simulation:** It includes simulation tools that enable designers to analyze the behavior of their circuits under different conditions. This helps in verifying the functionality and performance of the designed circuits before moving to the fabrication stage.
3. **Layout Design:** Tanner EDA provides tools for designing the physical layout of integrated circuits. This involves arranging and connecting components on a silicon substrate according to the specifications derived from the schematic design.

4. **Verification:** The suite includes verification tools to ensure that the designed circuits meet the required specifications and standards. This involves checking for design rule violations, electrical integrity, and other factors.
5. **Process Design Kits (PDKs):** Tanner EDA supports various semiconductor process technologies through Process Design Kits. These kits provide information and models necessary for designing circuits specific to a particular semiconductor fabrication process.
6. **Analog/Mixed-Signal Design:** Tanner EDA is particularly well-suited for analog and mixed-signal IC design, where both analog and digital components are integrated into a single chip.
7. **Custom IC Design:** It is commonly used for custom IC design projects, where designers need flexibility in designing and optimizing circuits for specific applications.

Schematic Designs:

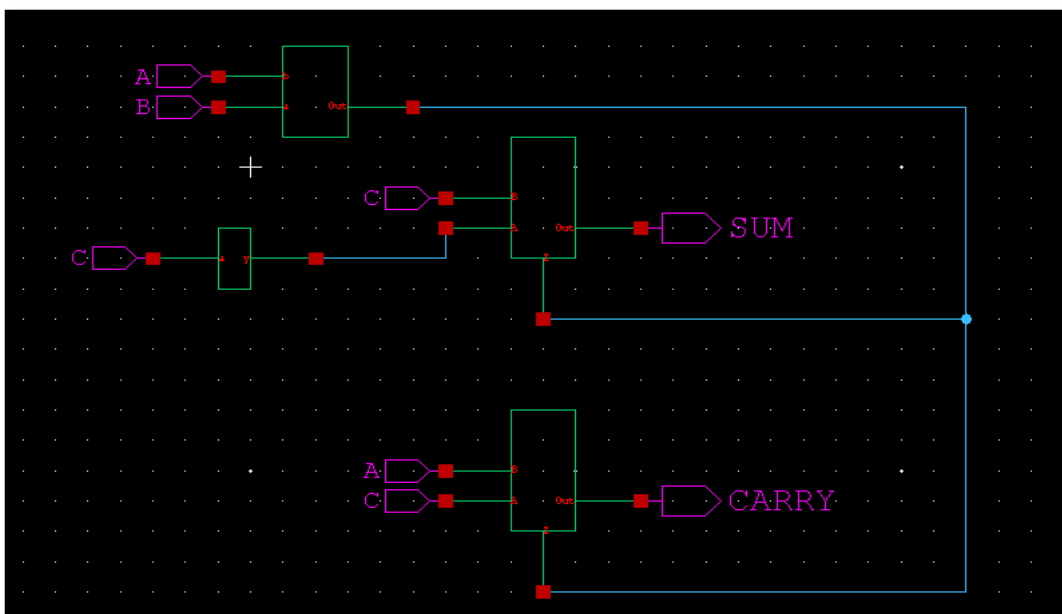


Fig: Schematic of Proposed XNAIMC based full adder

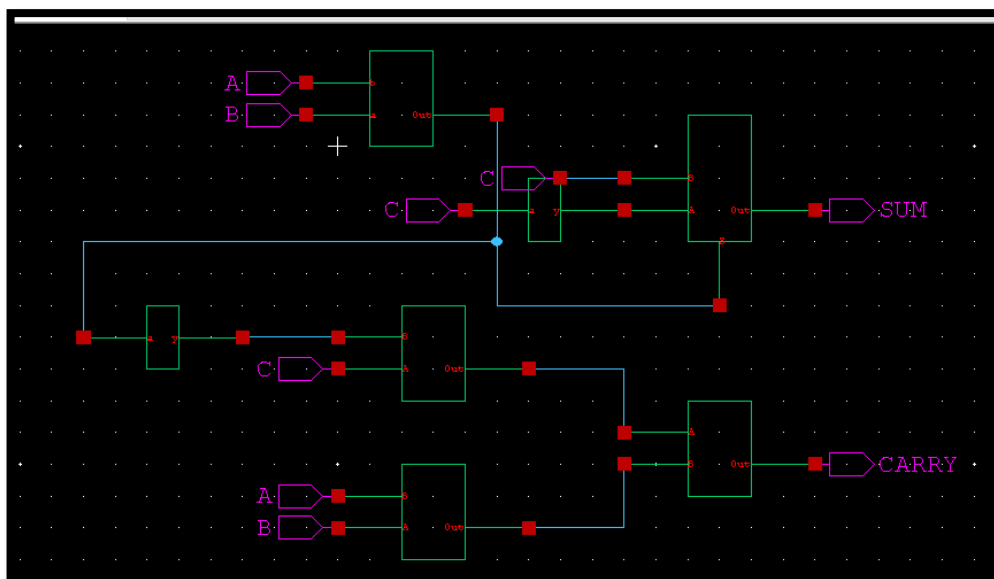


Fig : Schematic of Proposed XAC based full adder

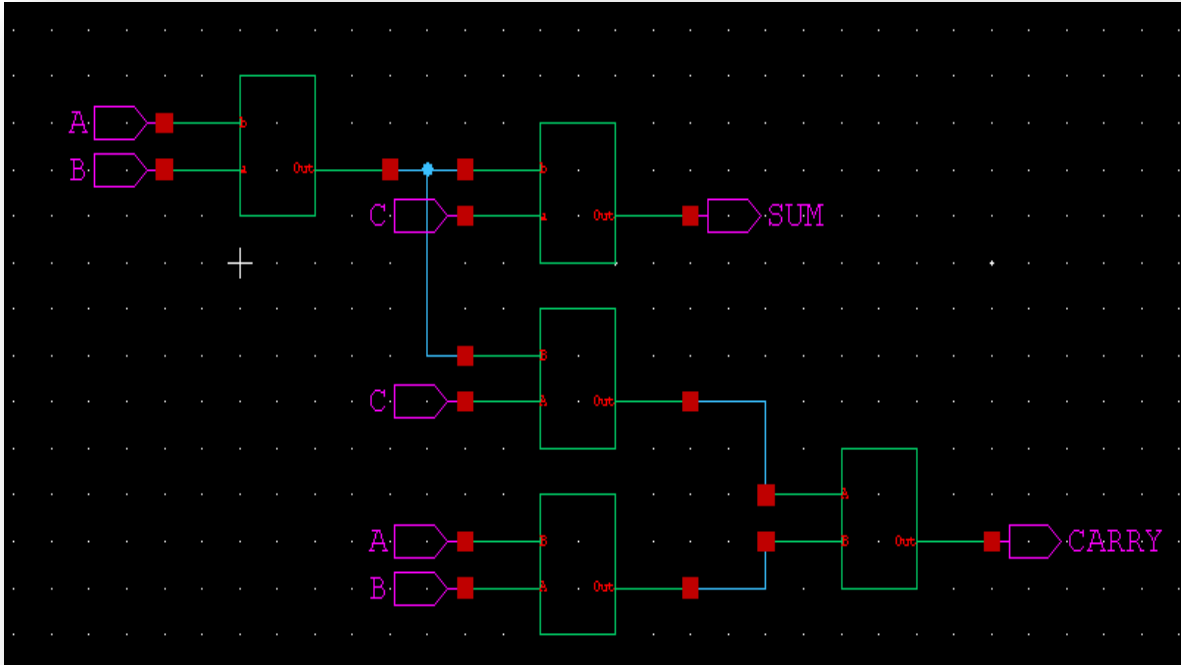
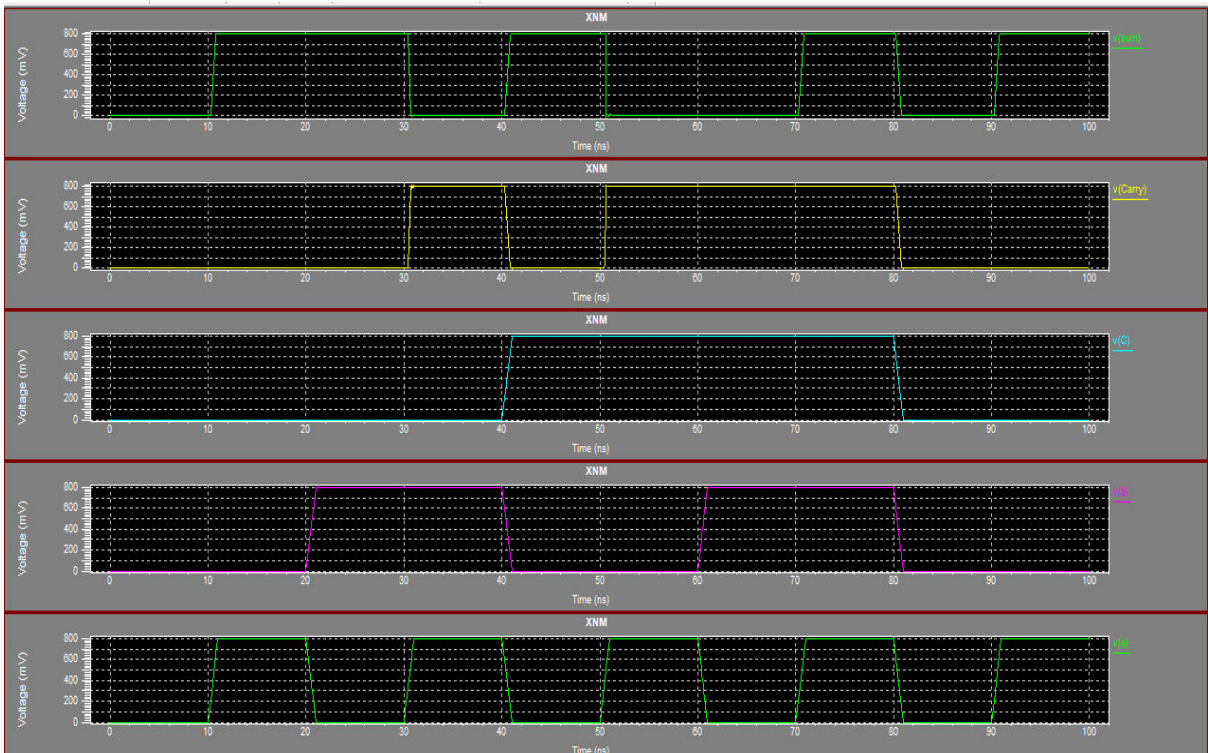


Fig : Waveform of Full adder



COMPARISION TABLE: EXISTING SYSTEM OUTPUT VALUES

DESIGN	AREA (TRANSISTOR COUNT)	DELAY (ns)	POWER (uw)
AND OR based Logic	74	0.159	46.66
Using half adders	46	0.159	6.25
Using 2:1 MUXes	64	20.03	137.5
Centralized	50	20.05	7.39
Shannon's theorem	72	0.159	17.5

PROPOSED SYSTEM OUTPUT VALUES

DESIGN	AREA (Transistors count)	DELAY (ns)	Power (uw)
XAC	46	0.159	5.62
XNM	38	0.032	3.907
XANMIC	46	0.159	5.616

VI. CONCLUSION

This study introduces three innovative gate-level full adder designs: XNM, XNAIMC, and XAC. Among these, the XAC-based full adder exhibits the fastest speed, whereas the XNM-based full adder is the most space-efficient. The XNAIMC-based adder closely matches the XAC-based adder in terms of delay. Notably, the XAC-based full adder outperforms even the full adder cell found in a commercial standard cell library, showcasing its superior performance.

REFERENCES

1. N. Zhuang and H. Wu, A New Design Of The CMOS Full Adder, IEEE Journal of Solid-State Circuits, Vol. 27, No. 5, May 1992, pp. 840- 844.
2. N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI Design – A Systems Perspective, 2 nd Edition, Addison-Wesley Publishing, MA, USA, 1993.
3. R. Shalem, E. John and L.K. John, A Novel Low-Power Energy Recovery Full Adder Cell, Proc. ACM Great Lakes Symposium on VLSI, pp. 380-383, 1999.
4. M. Margala, Low-Voltage Adders For PowerEfficient Arithmetic Circuits, Microelectronics Journal, Vol. 30, No. 12, December 1999, pp. 1241-1247.
5. A.M. Shams, T.K. Darwish and M.A. Bayoumi, Performance Analysis Of Low Power 1-Bit CMOS Full Adder Cells, IEEE Trans. on VLSI Systems, Vol. 10, No. 1, February 2002, pp. 20-29.
6. M. Zhang, J. Gu, C.H. Chang, A Novel Hybrid Pass Logic With Static CMOS Output Drive Full Adder Cell, Proc. IEEE Intl. Symposium on Circuits and Systems, pp. 317-320, 2003.



7. Y. Jiang, A. Al-Sheraidah, Y. Wang, E. Sha and J.-G. Chung, a Novel Multiplexer-Based Low-Power Full Adder, IEEE Trans. on Circuits and Systems – II: Express Briefs, Vol. 51, No. 7, July 2004, pp. 345-348.
8. S. Goel, S. Gollamudi, A. Kumar and M. Bayoumi, On The Design Of Low-Energy Hybrid CMOS 1-Bit Full Adder Cells, Proc. 47th IEEE Intl. Midwest Symposium on Circuits and Systems, vol. II, pp. 209-212, 2004.
9. S. Goel, A. Kumar and M.A. Bayoumi, Design of Robust, Energy-Efficient Full Adders for Deep Submicrometer Design Using Hybrid CMOS Logic Style, IEEE Trans. on VLSI Systems, Vol. 14, No. 12, December 2006, pp. 1309-1321.
10. C. Senthilpari, A.K. Singh and K. Diwakar, Design Of A Low-Power, High-Performance, 8×8 Bit Multiplier Using A Shannon-Based Adder Cell, Microelectronics Journal, Vol. 39, No. 5, May 2008, pp. 812-821.
11. STMicroelectronics CORE65LPLVT_1.10V Version 4.1 Standard Cell Library, User Manual and Databook, July 2006.
12. R.K. Brayton, A.L. Sangiovanni-Vincentelli, C.T. McMullen and G.D. Hachtel, Logic Minimization Algorithms for VLSI Synthesis, Kluwer Academic Publishers, MA, USA, 1984.
13. M. Morris Mano, Digital Design, 3rd Edition, Prentice-Hall Inc., NJ, USA, 2002.
14. J.P. Uyemura, CMOS Logic Circuit Design, 1st Edition, Springer, 1999.



INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  ijirset@gmail.com



www.ijirset.com

Scan to save the contact details