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Low Power High Accuracy Approximate Multiplier Using High Order Compressors

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ABSTRACT: To reduce the power consumption, the design of approximate multiplier appears as a promising solution for formally error-resilient applications. In this paper, we propose a low-power high-accuracy approximate 8 x 8 multiplier design. The proposed design has two main features. First, according to the significance, different weights utilize different compressors (in different levels of accuracy) to accumulate their product terms. As a result, the power consumption can be saved with as small error. Second, for the middle significance weights, we use high order approximate compressors (e.g., 8:2 compressor) to reduce the logic of carry chains. To our knowledge, the proposed design is the first work that successfully uses high-order approximate compressors in the approximate multiplier design. Compared with an exact multiplier (Dadda tree multiplier), experimental results show that the proposed approximate multiplier can achieve both low power and high accuracy.

KEYWORDS: -approximate computing; arithmetic circuits; logic design ;low-power design ;partial product reduction.

I. INTRODUCTION

Nowadays, the demand for low power, high performance portable devices has been greatly increased. The growing market of portable electronic systems demands microelectronics circuits design with low power dissipation. Multipliers play an important role in today's digital signal processing and various other applications.

With advances in technology, many researchers have tried and are trying to design multipliers which offer high speed, low power consumption and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power VLSI implementation network overloading by intelligent circuit modifications [8]. EPTL flip flops are contention free and are expected to operate at wide range of operating voltages. You et.al, recently proposed a contention free low power EPTL flip flop that is completely void of any redundant pre-charge and discharge operations which can save 80 % power consumption when compared to conventional TGFF under 10 % data activity [11]. The present manuscript analyzes the power consumption features of the EPTL D flip flop using 18nm technological node. The analysis at 18nm technological node attests to the small circuit layout of the flip flop that is compatible with present lithographical tools yielding reliable devices for nominal operation.

II. LITERATURE SURVEY

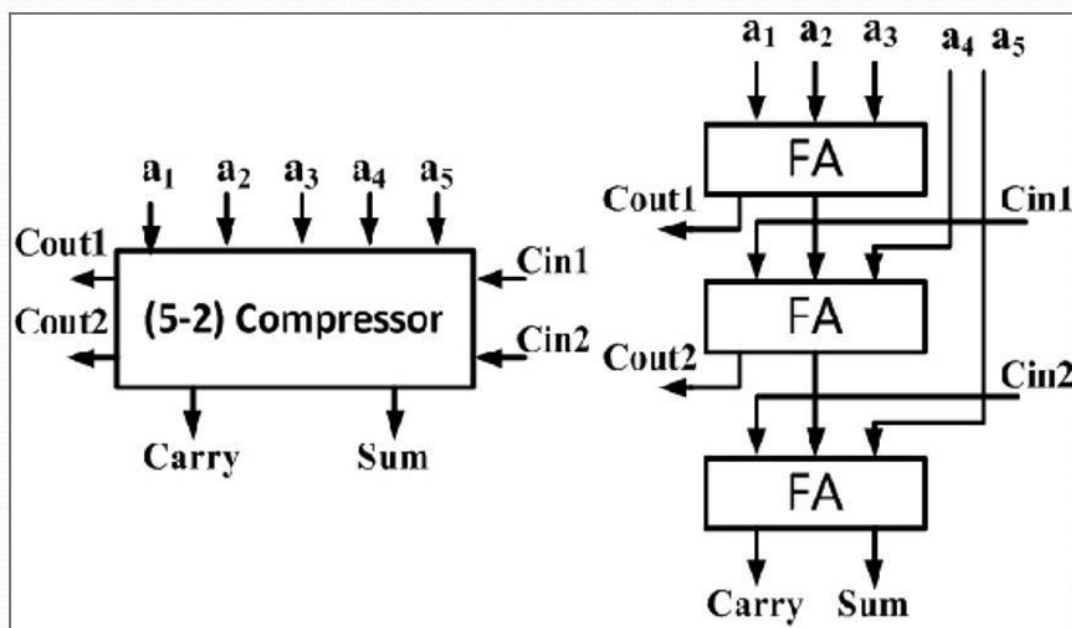
"Approximate Compressor for Error-Resilient Multiplier Design", Approximate circuit design is an innovative paradigm for error-resilient image and signal processing applications. Multiplication is often a fundamental function for many of these applications. In this paper, three approximate compressors are proposed with an accuracy constraint for the partial product reduction (PPR) in a multiplier. Both approximation and truncation are considered in the approximate multiplier design. An image sharpening algorithm is then investigated as an application of the proposed multiplier designs. Extensive simulation results show that the proposed designs achieve significant reductions in area and power while achieving a high signal-to-noise ratio (SNR > 35 dB), compared to their exact counterparts as well as other approximate multipliers.

III. PROPOSED SYSTEM

Multipliers are important components that dictate the overall arithmetic circuits' performance. The most critical components of multipliers are compressors.

A new 5:2 compressor architecture based on changing some internal equations is proposed. In addition, using an efficient full-adder (FA) block is considered to have a high-speed compressor.

The proposed architecture is compared with the best existing designs presented in the state-of-the-art literature in terms of power, delay and area.



IV. ADVANTAGES OF PROPOSED SYSTEM

- Re-silent errors are reduced.
- Power consumption reduced.
- Delay is reduced

V. DEVELOPMENT PROCESS

- Frontend Development Tools: While the project is focused on backend development, it requires programming..
- XILINX ISE 14.5v.
- Verilog code is used.

VI. RESULT AND DISCUSSION

- Approximate computing can decrease the design complexity with an increase in performance and power efficiency for error resilient applications.
- Data compression has a major role in multimedia and image processing applications to encode the information in a compact size. In those applications, reducing area, power and delay are the most important requirements.
- In this paper two new 5:2 exact compressor are designed to analyse the booth multiplier based on area, power consumption, delay with error distance.



VII. CONCLUSION

Utilizing a 5:2 Multiplier instead of a 4:2 Multiplier minimizes both the power consumption and the overall delay and also the accuracy will be increased.

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