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VLSI Implementations of High-Speed Adaptive Filter Structure for Speech Enhancement

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ABSTRACT: Implementing a high-speed adaptive filter structure in VLSI design for speech enhancement is the primary emphasis of this study. This paper presents a precise analysis of the critical path of the least-mean-square (LMS) adaptive filter for deriving its architectures for high-speed and low-complexity implementation. There is a need for efficient and low-power digital signal processing techniques due to the rising demand for improved speech quality in a wide range of applications, including telecommunication and voice recognition systems. The suggested adaptive filter structure works to improve voice signal quality by lowering noise levels and raising clarity standards. Using very large-scale integration (VLSI) methods, we optimize the adaptive filter for speed, power consumption, and silicon area. For the real-time hardware assessment, we use a Virtex FPGA board to run our Verilog HDL code generated in the Xilinx ISE environment. We also carry out the ASIC design implementation and acquire the measurements of power consumption and area utilization from the chip's core design. The findings prove that the proposed adaptive filter structure, when implemented in VLSI design, is capable of successfully handling the difficulties inherent in speech enhancement software.

I. INTRODUCTION

Signals carry important information about the behavior of the system under study. Real-time processing of data needs a better capability of any system under study. Signal processing is therefore necessary to handle the data. There are two subfields available in signal processing namely, analog signal processing and digital signal processing. Advanced technological development in the area of digital circuit design is the key to the growth of Digital Signal Processing (DSP). Representation of a signal in terms of samples is done in DSP. Real-world analog signals are measured, processed, and compressed by DSP systems. They are preferred due to low cost, flexibility, reliability, and accuracy being a small device. DSP systems have a variety of applications which include audio and speech signal processing, sonar and radar signal processing, sensor array processing, spectral estimation, statistical signal processing, digital image processing, signal processing for communications, control of systems, biomedical signal processing, seismic data processing and so on.

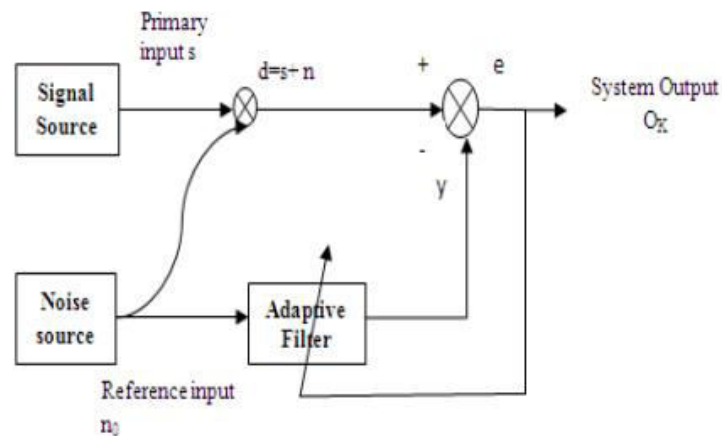
In the last decade, the noise level has increased 14624anifold, especially in urban areas. Noisy environments are now part of urban life and unavoidable. Major causes of ever-increasing noise levels are rapid industrialization, exposure to many electronic gadgets such as TV, music systems, mobile phones, and household electrical equipment like air conditioners, exhaust fans, mixer grinders, coolers, and washing machines. All these types of noises generated from different noise sources affect the quality of communication between people when they are exposed to noisy environments. When a signal is transmitted from one point to another, different types of noises distort the desired speech signal. The noise may be background noise present at the source or channel noise. These noises are due to time-varying physical processes which are mostly unknown and unpredictable in advance. Since most of the time the variations.

II. NEED FOR ADAPTIVE SIGNAL PROCESSING

Digital filter design needs well-prescribed specifications. Sometimes, the specification of the signal may not be available or the signal may be time-varying. In such situations, instead of a fixed filter, a digital filter with adaptive coefficients is employed. To update the coefficients, the algorithm needs extra information which is given as the reference signal to the system. The adaptive filter can be defined as a filter that adjusts its transfer function according to

an optimizing algorithm. In it, coefficients are updated at each iteration until they converge. An adaptive filter has an algorithm to monitor the environment and to vary the filter transfer function accordingly to obtain optimal performance. Adaptive noise cancellation is an important application of adaptive filter that has been used in a range of digital signal processing systems. They include noise reduction from ECG signals noise reduction from speech signals, etc. are unknown, only adaptive filters can track and diminish the noise from the desired signal.

The Primary input 'd' consists of the original signal 's' and the noise signal 'n' which is uncorrelated. The input 'n0' is fed to the adaptive filter as reference and is correlated with the noise 'n'. The output of the adaptive filter is designated as 'y' which is similar to 'n0'. The filter output obtained is thus subtracted from the contaminated signal to get the output 'OK' or $e = s + n - y$. The adaptive algorithm operates on this signal to update the coefficients, thereby improving the performance of the system.



III. EXISTING SYSTEM

The direct-form LMS adaptive filter is often believed to have a long critical path due to an inner product computation to obtain the filter output. This is mainly based on the assumption that an arithmetic operation starts only after the complete input operand words are available/generated.

EXISTING SYSTEM ALGORITHM:
Direct-form LMS adaptive filter.

EXISTING SYSTEM DRAWBACKS:
Low speed, low throughput.
High Area.

Various systolic architectures have been implemented using the DLMS algorithm. They are mainly concerned with the increase in the maximum usable frequency Problem with these architectures was they involved a large adaptation delay. This delay is of $\sim N$ cycles for filter length N , which is quite high for large-order filters.

DISADVANTAGES
The computational complexity of this Design is very high.
Throughput is low compared to the proposed system.

IV. PROPOSED SYSTEM

There are two main computing blocks in the direct-form LMS adaptive filter, namely, i) the error-computation block and ii) the weight-update block. Most of the area-intensive components are common in the error-computation and weight-update blocks: the multipliers, weight registers, and tapped-delay line.

PROPOSED ALGORITHM

Direct-form and transpose-form DLMS adaptive filters.

DIRECT-FORM AND TRANSPOSE-FORM DLMS ADAPTIVE FILTERS

The Direct-form and transpose-form DLMS adaptive filters during the nth iteration are updated according to the following equations:

$$w_{n+1} = w_n + \mu \cdot e_n \cdot x_n \quad (1a)$$

Where;

$$e_n = d_n - y_n \quad y_n = w_n^T \cdot x_n \quad (1b)$$

where the input vector x_n and the weight vector w_n at the nth iteration are, respectively, given by

$$x_n = [x_n, x_{n-1}, \dots, x_{n-N+1}]^T$$

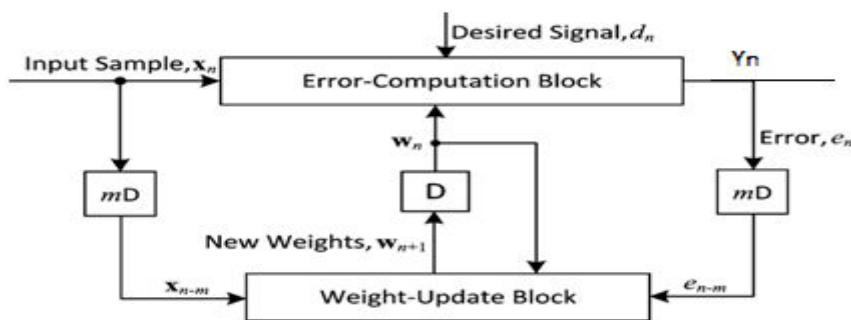
$$w_n = [w_n(0), w_n(1), \dots, w_n(N-1)]^T,$$

Assuming that the latency of computation of error is n_1 cycles, the error computed by the structure at the nth cycle is e_{n-n_1} , which is used with the input samples delayed by n_1 cycles to generate the weight-increment term. The weight-update equation of the modified DLMS algorithm is given by

$$w_{n+1} = w_n + \mu \cdot e_{n-n_1} \cdot x_{n-n_1} \quad (3a)$$

Where $e_{n-n_1} = d_{n-n_1} - y_{n-n_1}$ (3b) and $y_n = w_n^T \cdot x_n$. (3c)

We notice that, during the weight update, the error with n_1 delays is used, while the filtering unit uses the weights delayed by n_2 cycles.

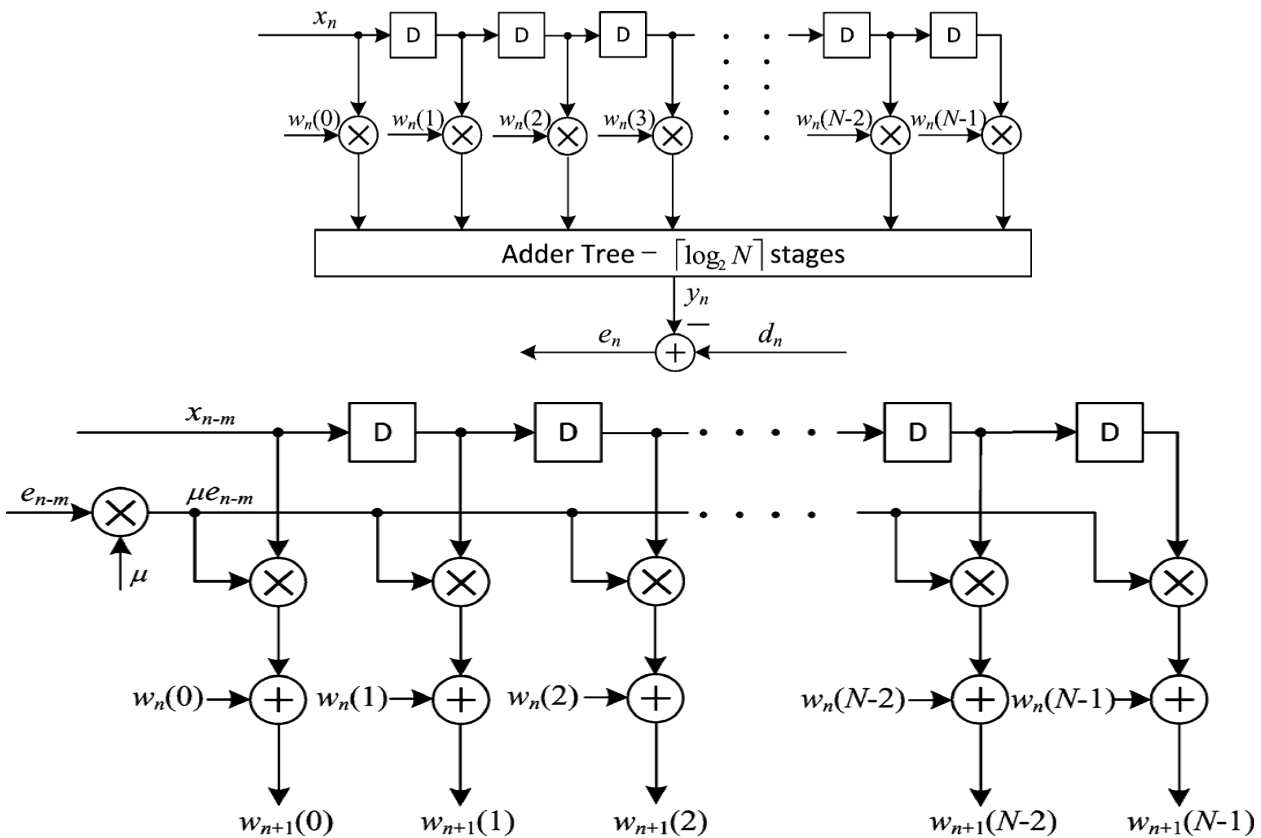


Generalized block diagram of direct-form DLMS adaptive filter.

There are two main computing blocks in the direct-form LMS adaptive filter, namely, the error-computation block and the weight-update block. It can be observed in that most of the area-intensive components are common in the error-computation and weight-update blocks: the multipliers, weight registers, and tapped-delay line.

The adder tree and subtract or and the adders for weight updating, which constitute only a small part of the circuit, are different in these two computing blocks. For the zero-adaptation-delay implementation, the computation of both these blocks is required to be performed in the same cycle. Moreover, since the structure is of the non-pipelined type, weight updating and error computation cannot occur concurrently. Therefore, the multiplications of both these phases could be multiplexed by the same set of multipliers.

A generalized block diagram of direct-form DLMS adaptive filter. It consists of an error-computation block and a weight-update block. The number of delays shown in corresponds to the pipeline delays introduced due to pipelining of the error-computation block.



V. SYSTEM STUDY

INTRODUCTION TO MODELSIM

ModelSim is a useful tool that allows you to stimulate the inputs of your modules and view both outputs and internal signals. It allows you to do both behavioural and timing simulation, however, this document will focus on behavioural simulation. Keep in mind that these simulations are based on models and thus the results are only as accurate as the constituent models. ModelSim /VHDL, ModelSim /VLOG, ModelSim /LNL, and ModelSim /PLUS are produced by Model Technology™ Incorporated. Unauthorized copying, duplication, or other reproduction is prohibited without the written consent of Model Technology. The information in this manual is subject to change without notice and does not represent a commitment on the part of Model Technology. The program described in this manual is furnished under a license agreement and may not be used or copied except in accordance with the terms of the agreement. The online documentation provided with this product may be printed by the end-user. The number of copies that may be printed is limited to the number of licenses purchased. ModelSim is a registered trademark of Model Technology Incorporated. Model Technology is a trademark of Mentor Graphics Corporation. PostScript is a registered trademark of Adobe Systems Incorporated.

MODELSIM SE BENEFITS

- High-performance HDL simulation solution for FPGA & ASIC design teams
- The best mixed-language environment and performance in the industry
- Intuitive GUI for efficient interactive or post-simulation debugging of RTL and gate-level designs
- Merging, ranking, and reporting of code coverage for tracking verification progress
- Sign-off support for popular ASIC libraries
- All ModelSim products are 100% standards-based. This means your investment is protected, risk is lowered, reuse is enabled, and productivity is enhanced
- Award-winning technical support

VI. SYNTHESIS TOOL

XILINX

Xilinx is a supplier of programmable logic devices. It is known for inventing the field programmable gate array (FPGA) and as the first semiconductor company with a fables manufacturing model. Founded in Silicon Valley in 1984, the company is headquartered in San Jose, California, U.S.A.; Dublin, Ireland; Singapore; and Tokyo, Japan. The company has corporate offices throughout North America, Asia and Europe.

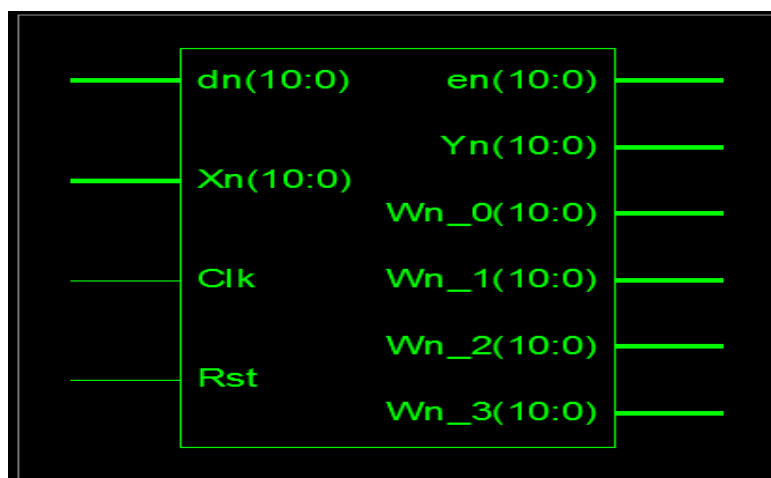
TECHNOLOGY

Xilinx designs, develops and markets programmable logic products including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs programmable logic devices for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing. Xilinx's FPGAs have been used for the ALICE (A Large Ion Collider Experiment) at the CERN European laboratory on the French-Swiss border to map and disentangle the trajectories of thousands of subatomic particles.^[29] Xilinx has also engaged in a partnership with the United States Air Force Research Laboratory's Space Vehicles Directorate to develop FPGAs to withstand the damaging effects of radiation in space for deployment in new satellites, which are 1,000 times less sensitive to space radiation than the commercial equivalent. The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families are focused on system-on-chip (SoC) designers because they include up to two embedded IBM PowerPC cores. Some members of the Virtex-II Pro, Virtex-4 and Virtex-5 FPGA families contain PowerPC processor blocks. Xilinx FPGAs can run a regular embedded OS (such as Linux or Vs Works) and can implement processor peripherals in programmable logic. Xilinx's IP cores include IP for simple functions (BCD encoders, counters, etc.), for domain specific cores (digital signal processing, FFT and FIR cores) to complex systems (multi-gigabit networking cores, Micro Blaze soft microprocessor, and the compact Picoblaze microcontroller). Xilinx also creates custom cores for a fee.

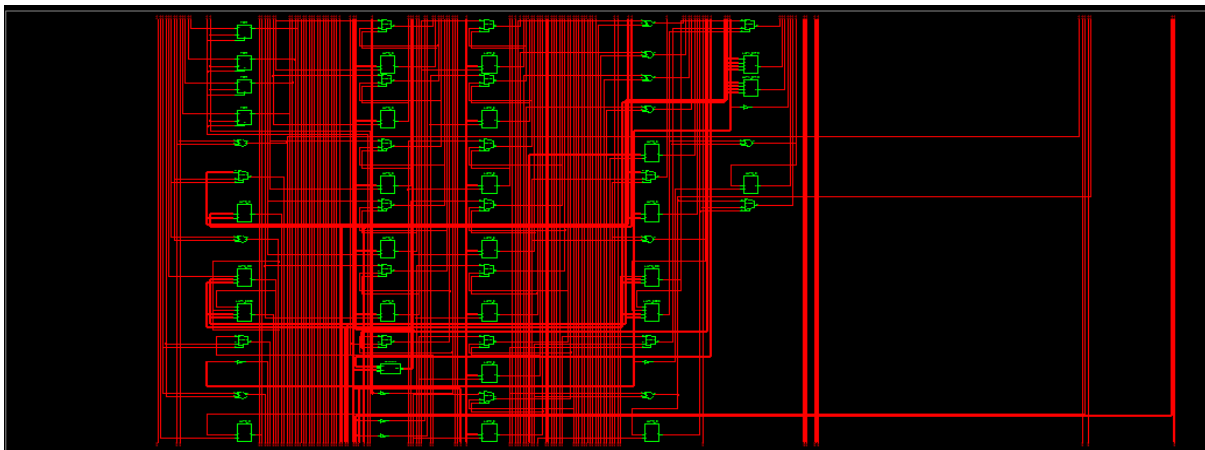
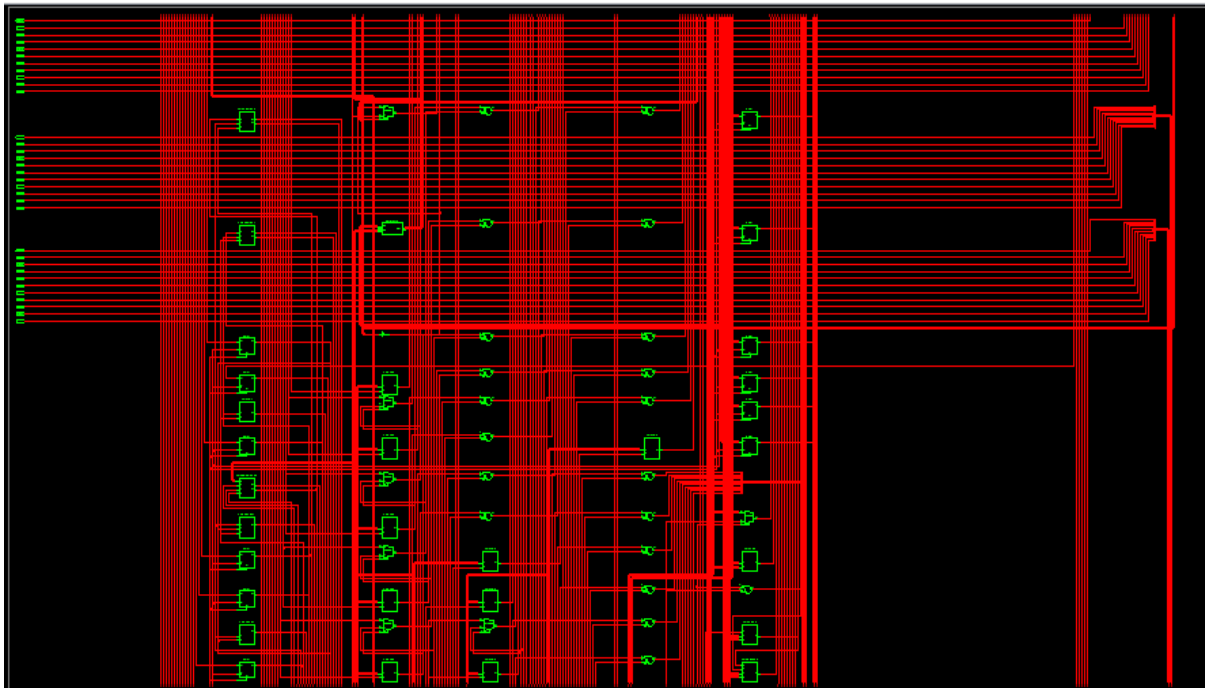
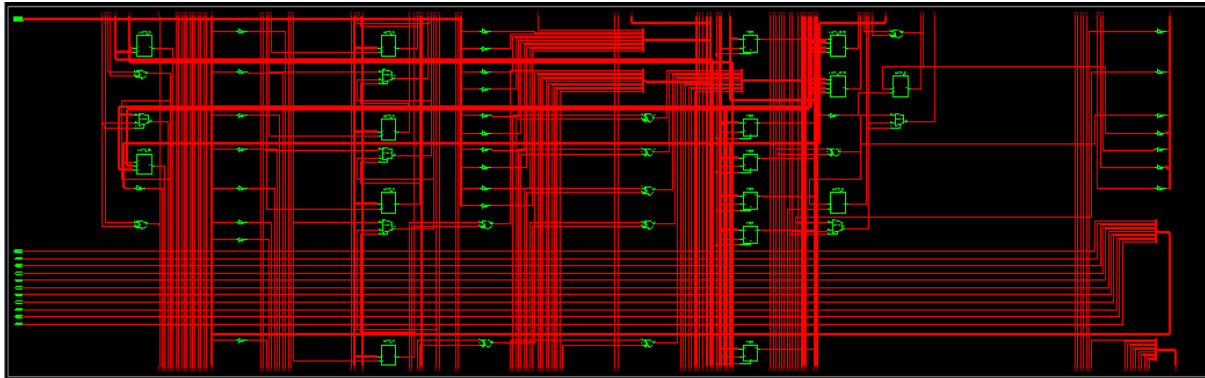
Xilinx SRAM-based FPGAs

The basic structure of Xilinx FPGAs is array-based, meaning that each chip comprises a two-dimensional array of logic blocks that can be interconnected via horizontal and vertical routing channels. An illustration of this type of architecture was shown in Figure. Xilinx introduced the first FPGA family, called the XC2000 series, in about 1985 and now offers three more generations: XC3000, XC4000, and XC5000. Although the XC3000 devices are still widely used, we will focus on the more recent and more popular XC4000 family.

RTL SCHEMATIC FOR UNRETIMED DF-LMS



TECHNOLOGY SCHEMATIC FOR UNRETIMED DF-LMS



COMPARISON TABLE

S.No	Method Name	Area		Delay		
		Slices	LUT	Max Delay	Gate Delay	Path Delay
1.	Transpose form retimed delayed LMS (TF-RDLMS)	77	167	21.005ns	13.869ns	7.136ns
2.	Unretimed DF-LMS	33	110	23.303ns	16.855ns	6.448ns
3.	Retimed DF-RDLMS	99	99	17.251ns	13.018ns	4.233ns

VII. CONCLUSION

Based on a precise critical-path analysis, we have derived low-complexity architectures for the LMS adaptive filter. We have shown that the direct-form and transpose-form LMS adaptive filters have nearly the same critical path delay. The direct-form LMS adaptive filter, however, involves less register complexity and provides much faster convergence than its transpose-form counterpart since the latter inherently performs delayed weight adaptation. We have proposed three different structures of direct-form LMS adaptive filter with i) zero adaptation delay, ii) one adaptation delay, and iii) two adaptation delays. Proposed Design 1 does not involve any adaptation delay. It has the minimum of MUF among all the structures, but that is adequate to support the highest data rate in current communication systems. Finally, the LMS Adaptive FIR Filter is implemented using Verilog language and dumped into the FPGA Spartan Series Device.

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