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Performance Analysis of Multilevel Inverter Based on SVPWM for Renewable Energy Sources

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ABSTRACT: To decrease Total Harmonic Distortion, the Pulse Modulated Switching Cascaded H-bridge Multilevel Inverter (PM-SCHM) is recommended. In the PM-SCHM approach, a multi-level inverter is structured in an H-bridge Cascaded way. With in contrary way, a shunt Active Power Filter (APF) would indeed be employed to compensate for current harmonic intensity. The PM-SCHM technology, which uses a Linear Quadratic Regulator to organise constituents, is given a pulse modulation approach (LQR). In the established LQR method, a load is being used to balance for source voltage. This study focused on 5th order harmonics with a relatively high frequency as a starting point. The comparative analysis of simulation results exhibited that the proposed Pulse Modulated Switching based Cascaded H-bridge Multilevel Inverter PM-SCHM scheme exhibits significant performance rather than the conventional technique.

KEYWORDS: Multilevel Inverter, Total Harmonic Distortion, Shunt Active power filter, Linear Quadratic Regulator.

I. INTRODUCTION

In elevated electrical systems, the output voltage waveform has harmonic information that must be suppressed to decrease grid disruption and achieve optimal energy efficiency[1]. The existence of temperature loss in certain electrical applications represents the maximum duty cycle to a few hundred hertz. Multilevel converters are used in electrical applications to tolerate maximal switching[2]. The performance of a few multilayer power converters for high voltage applications has been investigated [3]. Moreover, a suitable manipulation and filter mechanism based on grid integrity should be established at the point of connection. In typical, electric utilities have a 50th of their total harmonic distortion (THD) harmonic capacity. Given the complex stability and high cost, attenuators are utilised in power system systems to eliminate harmonic distortion in grid systems.

Utilizing compensatory mechanisms, a variety of recognised methods for establishing a local or global control scheme for harmonic or voltage imbalance have proven to be successful. Nonetheless, those systems are exposed to a wide range of restrictions due to the issues of strong propensity and decentralized capacity dispersion, which causes significant harmonic distortion and voltage unbalance in a distributed network. In a distributed system, temporary network topology and propagation scheme distribution, as well as local governance models, need not result in improved node effectiveness [4].Further, system parameters such as source distribution and intensity and line impedance require a control model through global optimization for harmonic distortion or voltage unbalance. Due to the penetration of massive signal generation and loads in power electronics results in complicated and changeable environment factor in a distributed network environment. The network intensity and distribution are difficult for identification those can be determined through a randomness of the Distributed Grid (DG) output power and uncertainty of location in electronic loads [5]. Meanwhile, errors in-line parameters are observed with an increase in network expansion, change in a branch, and cable aging [6].

In hybrid asymmetrical cascade inverter topology, the main concept is obtaining better inverter performance with the concept of hybridizing with the inclusion of various cells and switches. In a hybrid inverter, a combination of slow switches, features of high blocking voltage, and relative conduction losses are obtained for better equivalent switches

that exhibit faster switching capability, minimal conduction losses, and minimal switching losses [7]. For the operation of high-voltage cells with the minimum switching frequency, the concept of Pulse Width Modulation (PWM) is utilized.

Through designing and controlling inverter topology, it is possible to modulate all pairs of low-voltage cells with adjacent level switching characteristics [8]. The concept of that multi-level inverter topology is the reduction of switching losses rather than optimized and generalized single-phase inverters with the introduction of optimized transition with switching - state space[9], in three-phase inverters concept of modulation domain, is evolved[10]. The reduction of THD in multi-inverter network topology with a reduction of switching in the network. The section presented existing literature focused on improving the performance of multilevel inverter for the application of high-power applications. Researcher [11], suggested a topology with consideration of basic units arranged in cascade order. The designed topology consists of both unidirectional and bidirectional switches with two dc voltage sources. The constructed network topology includes two parts such as level-generation and polarity generation parts. In the level-generation part, two power switches are included those are arranged in the unidirectional platform and common emitter configuration consists of bidirectional blocking switches. In traditional network topology, several isolated DC voltage sources are equal to several power switches for reduction of voltage drop, topology volume, and cost compared with CHB multilevel inverter topology network.

From another methodology presented in[12], PM-SCHM offered two separate elements level generation and polarity generation. The circuit configuration of the MLM multilevel inverter includes 4 dc input sources. This architecture can lower the quantity of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels grows. The inability to operate in an asymmetric arrangement is a disadvantage of this design. This design is used in applications with a large number of dc voltage sources that require good power quality. [13] created a cross-connected source-based multilevel inverter (CCSMLI) with two isolated input sources in each cell as part of an experiment. The Input voltages are linked by including a higher pole terminal with the upstream source and a lower pole terminal with the source acting downstream via switches, and vice versa. In comparison to typical MLI, this new topology has a small number of switches. Furthermore, this architecture works well with isolated DC sources that are readily accessible.

In [14], focused on the location of the space vector in multilevel inverter arranged in fractal structure, with the inclusion of the SVPWM algorithm. The proposed PM-SCHM approach focused on sector identification without any lookup tables. In [15], constructed a novel MLI as Mokhberdorán Topology. The constructed network topology consists of two symmetric DC voltage sources, six switches, and eight diodes. The developed network topology exhibits significant advantages rather than traditional MLI topologies. From the analysis, it is observed that Mokhberdorán topology exhibits an effective choice of multilevel inverters for high power application performance scenarios. In [16] developed a new topology defined as "reversing voltage" MLI (RV-MLI) topology. This designed topology consists of two stages for the effective generation of the output voltage. In level-generation stages based on the positive polarity, levels are generated while the polarity-generation stage produces alternate voltage for the network[17 - 19]. Those topologies are duplicated based on the number of levels provided in the middle stage. Therefore, it can be suitable for three-phase applications for redundant and flexible sequence switching. Those topologies are not able to perform effectively for various DC source magnitudes with additive and subtractive combination of DC sources in the network [20].

This paper proposed a PM-SCHM scheme for the reduction of THD in high power electronic applications with improved efficiency. The proposed PM-SCHM scheme utilizes Pulse Switching Modulation Scheme integrated with Shunt Hybrid Filters (SHF). Through the incorporation of SHF frequency loss of the electrical network can be reduced. Further to reduce harmonics in the electrical network LQR is used which consists of load, phase voltage, and controller for effective maintenance of voltage flow within the circuit. The designed 3-phase circuit is arranged for the reduction of THD. The simulation of the proposed PM-SCHM scheme is comparatively examined with the existing approach stated that the proposed scheme provides significant performance rather than the conventional technique.

The organization of the paper is as follows: section 1 provides a general introduction and gives a detailed survey of existing modulation, harmonic distortion techniques. Then, in section 2 proposed PM-SCHM methodology is explained with some equations. Section 3 gives a detailed analysis of some parameters. Finally, the paper is concluded in section 4.

II. PROPOSED PM-SCHM FOR REDUCTION OF THD

This paper, presented about Pulse modulated switching based H-bridge multilevel inverter with Linear Quadratic Regulator for reduction of THD in the network. In Fig.1, presented about the flow of proposed PM-SCHM approach which includes diodes, capacitors, and switches. The constructed multilevel cascade inverter integrates several voltage levels and generates a sinusoidal voltage waveform. For the constructed inverter single-phase full-bridge is utilized for the generation of phases. A single-phase multilevel cascade Inverter topology is considered an essential component for the identification of phase legs located in a series-chain of H-bridge inverter, which generates various output voltage waveforms.

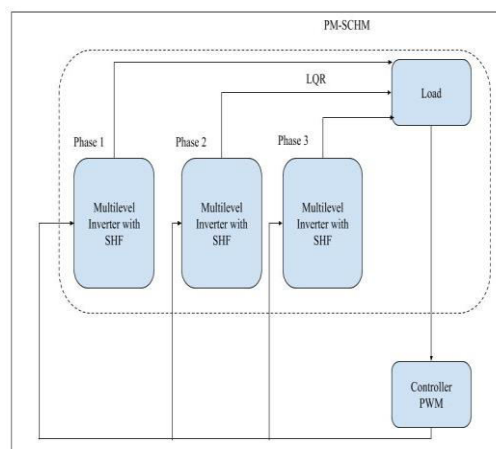


Fig.1. An overview of proposed PM-SCHM architecture

Those characteristics are difficult to achieve in other voltage source control topologies with DC link. In this topology, power conversion cells are arranged in series, hence voltage and power level can be measured easily. Within full-bridge inverter, DC link supply is provided individually, and this can be achieved through diode rectifiers without any single-phase transformer. The topology of the converter is arranged based on the series connection with a single-phase inverter with separate DC sources resulted in the synthesis of phase voltage with the addition of voltage generated by various power conversion cells.

2.1 Load balancing using Shunt Hybrid power filter

In Fig.2, illustrated about shunt APF scheme applied for three-phase four-wire system. In the system, load is provided in unbalanced linear and balanced linear voltage sources. The below equation (1), (2) and (3) provides the current measurement for both balanced and unbalanced load condition in the network.

$$i_{fa}^*(t) = i_{la}(t) - \frac{2(P_T + P_{loss})}{U_T} \sin(\omega t + \phi_{a1}) \tag{1}$$

$$i_{fb}^*(t) = i_{lb}(t) - \frac{2(P_T + P_{loss})}{U_T} \sin(\omega t + \phi_{a1} - \frac{2\pi}{3}) \tag{2}$$

$$i_{fc}^*(t) = i_{lc}(t) - \frac{2(P_T + P_{loss})}{U_T} \sin(\omega t + \phi_{a1} + \frac{2\pi}{3}) \tag{3}$$

where $i_{fk}^*(t)$ is represented as filtering current for phase k, $i_{lk}(t)$ is the phase of line current k. The developed system utilizes both balanced and unbalanced load conditions, hence load current incorporates both linear unbalanced load current and load current of rectifier; the subscript k represents the phases a, b or c, respectively. The total active power delivered to the load is denoted as P_T ; source voltage u_k with peak value sum is represented as U_T , load phase voltage components with phase angle a_1 has phase of a, and ω is denoted as angular speed fundamental frequency 'f' as 60Hz.

After the generation of reference current, it is applied to the hysteresis-band current controller for a control signal from the voltage source inverter (VSI) and performs actual current filtering that applied to APF electrical system. In the designed circuit C1 and D1 utilized for energy storage and applied to capacitors for where voltage fluctuates instantaneously due to the presence of harmonics. In the electrical system, at the terminals of inverter constant DC voltage U_{dc} is applied. The loss generated by switching and capacitor variation in voltage needs to be applied to the source, a controller power loss P_{loss} are summed at Pr. In the designed compensation scheme, harmonic cancellation and reactive power are not included in the Shunt APF compensation mechanism. Through these assumptions shunt APF or reference current generator are not utilized by the control algorithm. The shunt APF suggest to include the use of capacitor bank with with the advanced the load component, and hence the load current is sense with the site of the shunt capacitor bank.

The proposed PM-SCHM multilevel inverter utilizes the LQR method for controlling complex electrical systems with effective network performance. The designed PWM scheme utilizes an optimal controller with a minimization of the cost function. The cost function utilized for the proposed PM-SCHM multilevel inverter utilizes two matrices such as Q and R. Further, the designed network consists of weight assigned with state vector and input system. In this research, to reduce harmonic distortion LQR switching controller is designed for control signal generation of inverter voltage source applied for shunt APF and SHF compensation scheme. The functionality of the proposed PM-SCHM LQR-switching controller involved in the improvement of harmonic ripple current in the electrical system with SHF compensation.

2.2 Pulse-switching controller with LQR method

In an electrical system, Pulse-based switching controller is constructed for optimal controlling of signal for reduction of performance index using the following equation (4):

$$J = \int_0^{\infty} \{ (w - w_{ref})^T Q (w - w_{ref}) + u^T R u \} dt \quad (4)$$

In the above equation (4), the state vector is denoted as w and w_{ref} are represented as the desired reference of state vector; a semi-definite matrix symmetric or Hermitian matrix is denoted as Q and symmetric positive definite matrix as R.

In some scenarios, R is in scalar form, and sets are included in network control. With the use of optimal control law stated in equation (5), the cost function is reduced through the feedback control form. In the below equation (5) T is the network transpose vector and m is denoted as an optimal control law.

$$m = -K(w - w_{ref}) \quad (5)$$

With gain matrix K solution is obtained by steady-state Riccati equation with suitable gain matrix and switching control.

$$m = -hys(K(w - w_{ref})) \quad (6)$$

In above equation (6), the term hys is represented as follows equation (7) and equation (8) by,

$$\text{if } K(w - w_{ref}) > \frac{\Delta_i}{2} \text{ then } hys(K(w - w_{ref})) = 1 \quad (7)$$

$$\text{elseif } K(w - w_{ref}) < \frac{\Delta_i}{2} \text{ then } hys(K(w - w_{ref})) = -1 \quad (8)$$

Based on the above equation the proposed PM-SCHM model is utilized for switching and tracking control and selection of Di involved in switching frequency concerning reference tracking. The proposed PM-SCHM equivalent circuit incorporates hybrid filter compensation with the inclusion of both linear and nonlinear loads arranged in the RL series circuit arrangement of the load. In the below equation (9) and equation (10) state vector x related to state-space equation are presented.

$$x = [i_1 i_2 i_3 i_4]^T \quad (9)$$

$$\dot{x} = \begin{bmatrix} -\frac{R_s}{L_s} & 0 & 0 & -\frac{1}{L_s} \\ 0 & -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} \\ 0 & 0 & -\frac{R_{eq}}{L_{eq}} & -\frac{1}{L_{eq}} \\ \frac{1}{C_f} & \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} x + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_s + \begin{bmatrix} 0 \\ \frac{V_{dc}}{L_s} \\ 0 \\ 0 \end{bmatrix} m \quad (10)$$

For estimation equation (11) and equation (12), the state vector x is converter into new state vector w , which is based on local variables and control variables with filtering current c_f and capacitor current as i_c , the capacitor voltage terminal as U_c and load current i_l .

$$w = \begin{bmatrix} i_f \\ i_c \\ u_c \\ i_l \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 \\ -0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ u_c \end{bmatrix} = V_x \quad (11)$$

$$A = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & -\frac{1}{L_f} & 0 \\ \frac{R_s}{L_s} - \frac{R_f}{L_f} & -\frac{R_f}{L_s} & -\frac{1}{L_s} - \frac{1}{L_f} - \frac{1}{L_{eq}} & -\frac{R_s}{L_s} + \frac{R_f}{L_f} \\ 0 & \frac{1}{C_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_{eq}} & -\frac{R_{eq}}{L_{eq}} \end{bmatrix}; \gamma_1 = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}; \gamma_2 = \begin{bmatrix} U_{dc} \\ L_f \\ U_{dc} \\ 0 \end{bmatrix} \quad (12)$$

Based on the control law presented in equation (12), it is assumed that the network involved in full control over m for pulse switching and switching controller involved in linear multiple state combinations illustrated in Fig 3(c).

Through the utilization of the LQR switching controller current complexity of the network is reduced with the generation of inverter switching commands those are similar to hysteresis controller band current, this has been utilized in shunt active power filter applications. However, the challenges related to weighting matrices Q are selected for appropriate network performance. Mostly, controller states are presented by the weighted matrix Q and select appropriate value R for system control effect for achieving regulator convergence finite time. Alternatively, tuning decisions of weighted matrices are examined with a system step response for measuring steady-state of controller Q and R with the application of LQR design. After, the inclusion of LQR algorithm feedback matrices is estimated for measuring changes in the circuit and load circuit.

III. RESULT AND DISCUSSION

In this section, presented about results obtained for the proposed PM-SCHM pulse width modulation scheme with H-bridge cascaded network. The analysis of the proposed PM-SCHM model illustrated that it consists of three components such as (i) Pulse Width Modulation scheme, (ii) Shunt Hybrid Filter (SHF), and (iii) Linear Quadratic Regulator. The simulation parameters are listed in table 1.

Table 1. Simulation Setting for PM-SCHM

Parameters	Values
Simulation Software	MATLAB 2019a
RAM memory	4 GB
Processor	Intel core i7 processor
Modulation	Pulse Width Modulation
Input Voltage	300V
Phase Voltage	350V

3.1 Simulation Analysis

The performance of the proposed PM-SCHM system involved in PWM voltage measurement, phase voltage, the line-to-line voltage, and Total Harmonic Distortion (THD). The PM-SCHM involved in the construction of 7-levels with regulator design for measuring line to line voltage, phase voltage, and THD. In Fig 4, input voltage applied for proposed PM - SCHM scheme is presented.

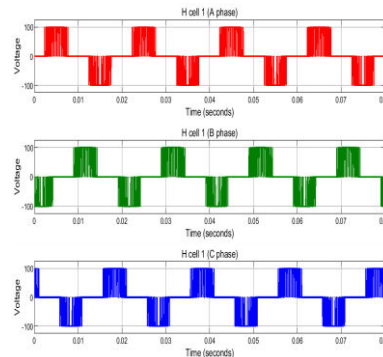


Fig. 2. Measurement of Voltage Using the Proposed PM-SCHM

The proposed PM-SCHM uses a pulse modulation scheme with the inclusion of a 3-phase electrical circuit arranged in 7-levels. Through the application of Pulse switching the load applied to the system converts an analog signal into a step signal. In Fig 4 voltage measured for constructed 3-phase circuit network are presented concerning A phase, B phase, and C phase. From Fig 2, it is observed that voltage all 3-phases utilizes a voltage value of 100 volts for the time period of 0 to 0.08 seconds. In three-phase electrical circuit phase voltage and phase, current exhibits significant performance for transmission of a signal from source to voltage. Generally, phase voltage is represented as a voltage measured between single components located in the three-phase circuit source or load. In Fig 4 voltage measured is 100 volts in square shape waveform.

3.2 Measurement of Total Harmonic Distortion

To understand the THD related to the phase change between carrier signals, the V-I activation signal graph was analyzed. Also, the conduction and short-circuit sequence were established for each instant of turning ON and OFF the V-I converter. In the proposed PM-SCHM, aimed to minimize the THD of the electrical network. To evaluate the performance of proposed PM-SCHM scheme for multi-level inverter THD of input signal and THD in line voltage are measured those are presented in fig 8 respectively.

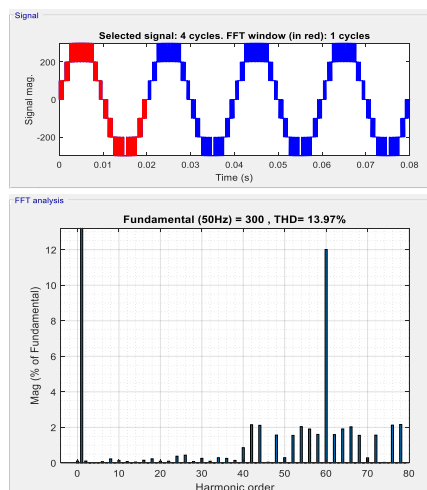


Fig. 3. THD of the input signal

In Fig 3, presented about Total Harmonic Distortion (THD) measured for input step signal. The THD analysis of the input step signal stated that Fast Fourier Transform (FFT) analysis of. The average percentage reduction of PM-SCHM scheme with existing technique line voltage THD reduction average of 74.3795% rather than existing technique.

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In table 2 presented about parameters measured for the proposed PM-SCHM scheme and in table 3 shows comparative analysis of THD reduction is presented with existing technique.

Table. 2 PM-SCHM Measured Values

Parameters	Measured	THD Measured
Input Voltage (V) in 3-phase	100	13.97
Line Voltage (V)	600	5.33
Phase Voltage (V)	250	5.31
Phase Current	2.25	16.49

Table. 3. Comparative analysis of THD with ref 12 and 13

Parameters	Optimization [13]	Vsi Topology Based_ Dstatcom [12]	THD of PM-SCHM	Average % Reduction in THD of proposed PM-SCHM
Input Voltage (V) in 3-phase	18.49	25.0	13.97	24.446
Line Voltage THD	16.45	28.29	5.33	67.599
Phase Voltage THD	10.78	6.67	5.31	50.74
Phase Current THD	26.78	-	16.49	38.4242

IV. CONCLUSION

THD degrades overall performance of electrical system with reduced efficiency. To overcome THD in multi-level inverter this research developed a PM-SCHM scheme. The proposed scheme integrates H-bridge inverter assembled with linear quadratic regulator (LQR) design. The designed multi-level inverter is assigned in cascaded design for reducing THD at 5th harmonics. The designed PM-SCHM scheme performance is measured in terms of THD phase voltage and phase current. Comparative analysis of simulation results stated that proposed PM-SCHM scheme exhibits significant reduction in THD. The average reduction in THD for input voltage, line voltage, phase current and phase voltage of 44.12%, 24.446%, 35.57% and 16.49% respectively. The arrangement of components in LQR with shunt filter design reduces the ripple current which in turns minimizes THD of the multilevel inverter. In the future, this research can be applied to the power grid for resolving optimization and harmonic distortion.

REFERENCES

1. R. Gunasekaran & C. Karthikeyan, "Nonlinear Transformational Optimization (NTO) technique based Total Harmonics Distortion (THD) reduction of line-to-line voltage for multi-level inverters", *Microprocessors and Microsystems*, 74, 102998, 2020.
2. M.S. Manoharan, A. Ahmed & J.H Park, "A PV power conditioning system using nonregenerative single-sourced trinary asymmetric multilevel inverter with hybrid control scheme and reduced leakage current", *IEEE Transactions on Power Electronics*, 32(10), 7602-7614, 2016.
3. A. Narendran & R. Sureshkumar, "Hysteresis-controlled-landsman converter based multilevel inverter fed induction-motor system using pic", *Microprocessors and Microsystems*, 103099, 2020.
4. M.N. Hamidi, D. Ishak, M. Zainuri & C.A. Ooi, "An asymmetrical multilevel inverter with optimum number of components based on new basic structure for photovoltaic renewable energy system's", *Solar Energy*, 204, 13-25, 2020.
5. S. Chitra & K. Valluvan, "Design and implementation of cascaded H-Bridge Multilevel Inverter Using FPGA With Multiple Carrier Phase Disposition Modulation Scheme", *Microprocessors and Microsystems*, 103108, 2020.
6. B.P. Reddy & S. Keerthipati, "A multilevel inverter configuration for an open-end-winding pole-phase-modulated-multiphase induction motor drive using dual inverter principle", *IEEE Transactions on Industrial Electronics*, 65(4), 3035-3044, 2017.
7. A. A Stonier & B. Lehman, "An Intelligent-Based Fault-Tolerant System for Solar-Fed Cascaded Multilevel Inverters", *IEEE Transactions on Energy Conversion*, 33(3), 1047-1057, 2017.
8. M.M. Hasan, A. Abu-Siada & A.S Dahidah, "A three-phase symmetrical DC-link multilevel inverter with reduced number of DC sources", *IEEE Transactions on Power Electronics*, 33(10), 8331-8340, 2017.
9. P.L Kamani & M.A. Mulla, "Middle-level SHE pulse-amplitude modulation for cascaded multilevel inverters", *IEEE Transactions on Industrial Electronics*, 65(3), 2828-2833, 2017.
10. S.S Lee, M. Sidorov, N.R.R Idris & Y.E. Heng, "A symmetrical cascaded compact-module multilevel inverter (CCM-MLI) with pulse-width modulation", *IEEE Transactions on Industrial Electronics*, 65(6), 4631-4639, 2017.
11. K. Haghdar & H.A. Shaya far, "Selective harmonic elimination with optimal DC sources in multilevel inverters using generalized pattern search", *IEEE Transactions on Industrial Informatics*, 14(7), 3124-3131, 2018.
12. T.S. Kumar, D.K.M Sahu & C.K. Rao, Total "Harmonic Distortion Analysis of Three-Phase Nonlinear Load Using H-Bridge Vsi Topology Based_ Dstatcom", *Int. Journal of Engineering Research and Applications*, 1, 2014.
13. K. Omirzakhov & A. Ruderman, "Time-domain optimization of voltage and current THD for a three-phase cascaded inverter with three H-bridges per phase", *International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) & 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP)*, 765-770, 2017.
14. B.G Shivaleelavathi, "A novel implementation of digital control strategy for multilevel inverters using FPGA Wave controller", *IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 1-6, 2017.
15. S. Rajalakshmi & P.Rangarajan, "Investigation of modified multilevel inverter topology for PV system", *Microprocessors and Microsystems*, 71, 102870, 2019.
16. T.A. Ahmed, E.E. Mohamed, A.R. Youssef, A.A. Ibrahim, M.S. Saeed & A.I. Ali, "Three-phase modular multilevel inverter-based multi-terminal asymmetrical DC inputs for renewable energy applications", *Engineering Science and Technology, an International Journal*, 2020.
17. K. Eguchi, A. Shibata, W.Do, & Y. Harada, "An inductor-less step-up/step-down multilevel inverter with a single input source", *Energy Reports*, 6, 146-152, 2020.

Volume 13, Issue 8, August 2024

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18. R. Choupan, S. Golshannavaz, D. Nazarpour, & M. Barmala, "A new structure for multilevel inverters with fault-tolerant capability against open circuit faults", *Electric Power Systems Research*, 168, 105-116, 2019.
19. V.F. Pires, A. Cordeiro, D. Foito & J.F. Silva, "Three-phase multilevel inverter for grid-connected distributed photovoltaic systems based in three three-phase two-level inverters", *Solar Energy*, 174, 1026-1034, 2018.
20. G. Ramya, V. Ganapathy & P. Suresh, "Comprehensive analysis of interleaved boost converter with simplified H-bridge multilevel inverter based static synchronous compensator system", *Electric Power Systems Research*, 176, 105936, 2019.



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