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DACA: Dynamic Accuracy-Configurable Adders for Energy-Efficient Multi-Precision Computing

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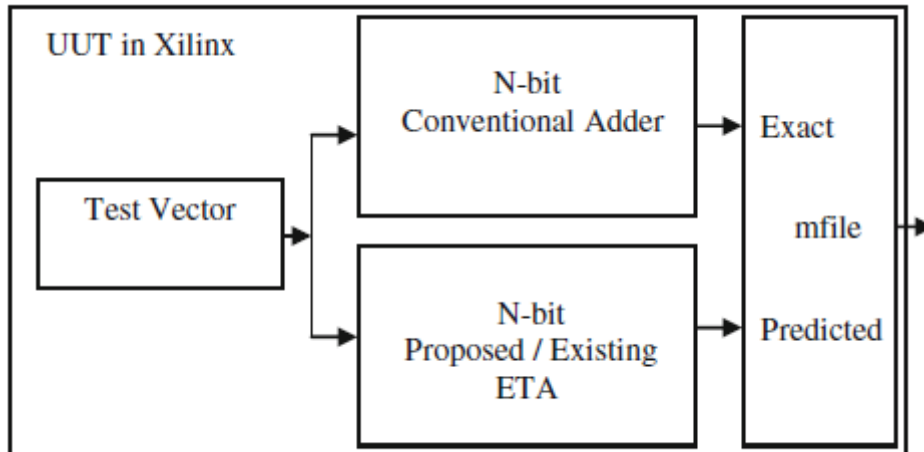
ABSTRACT: An accuracy-configurable adder (ACA) meets various requirements in energy efficiency and accuracy of many applications. However, it suffers from problems such as a large hardware cost for performing configurations. In this article, we propose two energy-efficient transistor-level accuracy-configurable full adders, referred to as a positive ACA (PACA) and a negative ACA (NACA). Each design uses only two transistors as switches driven by an enable signal to configure the accurate and approximate modes. Dynamic accuracy-configurable adders (DACAs) are further developed by cascading the PACAs or NACAs. The DACA design realizes a remarkable trade-off between accuracy and performance by switching between different degrees of approximations. This Proposed System Implemented using Verilog HDL and Simulated by Modelsim 6.4 c and Synthesized by Xilinx tool. The proposed system implemented in FPGA Spartan 3 XC3S 200 TQ-144.

I. INTRODUCTION

Today's technology revolution in portable electronic devices extensively requires high performance Very Large Scale Integration (VLSI) architecture in a processor design. The constraints involved with high performance are counter balanced to provide high accuracy, high speed, low power and area efficiency. The performance of the processor core has increased, which depends on the configuration, design parameters and effective utilization of the data path architectures. The elementary structure of the data path design for basic digital operations such as addition, subtraction, multiplication and division is a combination of conventional full adders. Many scientific and engineering problems are computed using accurate, precise and deterministic algorithms. However, in many applications involving signal/image processing and multimedia, exact and accurate computations are not always necessary, because these applications are error tolerant and produce results that are good enough for human perception. In these error resilient applications, reduction in circuit complexity, and thus, area, power and delay is very important for the operation of a circuit. Hence, approximate computing can be used in error tolerant applications by reducing accuracy, but still providing meaningful results faster and/or with lower power consumption. Addition and multiplication are often used in these applications. For addition, full adders have been analyzed in detail and a number of approximate designs have been proposed. In several new metrics are proposed and comparison is made among some of the adder designs. The error distance (ED) is defined as the arithmetic distance between an erroneous and the correct outputs for a given input. The mean error distance (MED) and normalized error distance (NED) are then proposed. Recently, approximate multipliers have also gained significance because of their importance in arithmetic operations.

OBJECTIVE: The Main Objective is Design a High-performance DACA- POSITIVE & NEGATIVE based 8-bit Error Tolerant Adders DACA To achieve high accuracy in an 8-bit proposed DACA- POSITIVE & NEGATIVE, CFA based structure is employed in the most significant accurate part (4-bit AP) and the DACA- POSITIVE & NEGATIVE based structure is proposed in the least significant Inaccurate Part (4-bit IP).

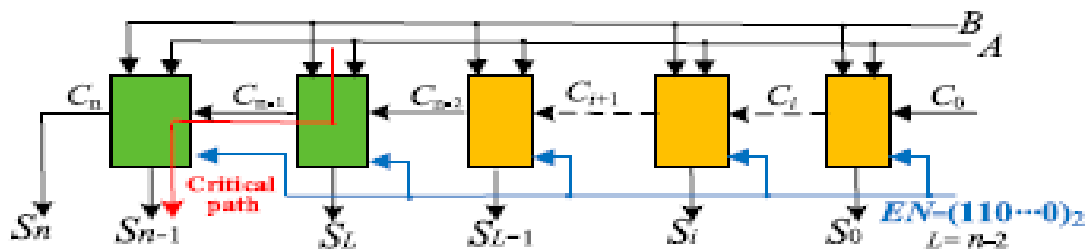
II. ARCHITECTURE OF DESIGN VERIFICATION SYSTEM



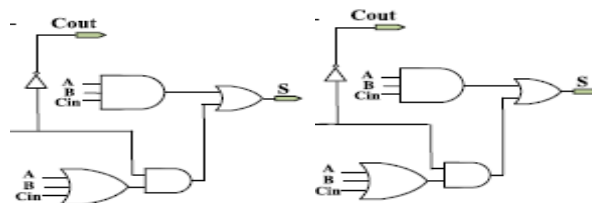
III. PROPOSED SYSTEM

The proposed DACA- POSITIVE & NEGATIVE has the PCL and SSL unit which are shown in Fig. 1. The PCL unit has structural regularity of two AND-OR logic blocks. The SSL unit has a 2:1 multiplexer logic. The logic functions of AND-OR gate block comprises 2-input AND gate and 2-input OR gate. It show the functional behavior of the AND-OR gate blocks. The optimized gate level logic of the DACA- POSITIVE & NEGATIVE design has approximated carry and sum outputs. In the SSL unit, O02 is the OR-ed output of all inputs which is applied as one of the multiplexer input (M_0) and the product of two inputs (Ao1) is applied as another input (M_1) to the multiplexer. Finally will make Proposed DACA- POSITIVE & NEGATIVE will implement 8 bit Adder Design and Error verification done by Conventional Designs.

IV. PROPOSED ETA 8 BIT DESIGN



V. PROPOSED ARCHITECTURE OF DACA- POSITIVE & NEGATIVE



Structures of the proposed PACA and NACA

VI. SOFTWARE REQUIREMENTS

- Verification Tool
- Modelsim 6.4c
- Synthesis Tool
- Xilinx ISE 13.2

VII. ARCHITECTURAL OVERVIEW

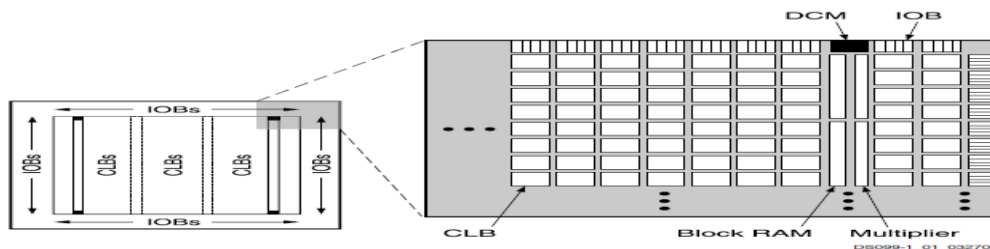
The Spartan-3 family architecture consists of five fundamental programmable functional elements:

Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.

Input/output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.

Block RAM provides data storage in the form of 18-Kbit dual-port blocks

Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.



SPARTAN-3 Family Architecture

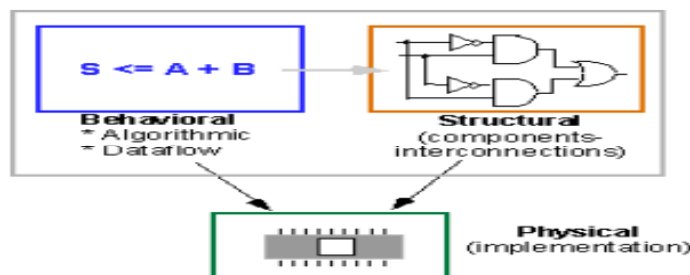
Ordering Information

Spartan-3 FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

VIII. SIMULATION IMPLEMENTATION

LEVELS OF REPRESENTATION AND ABSTRACTION

A digital system can be represented at different levels of abstraction [1]. This keeps the description and design of complex systems manageable. Figure 1 shows different levels of abstraction.



Behavioral, Structural and Physical

IX. CODE IMPLEMENTATION

```
module Design_Verification_System_16 (Clk,Rst,S,Error);

input Clk,Rst;
output reg [15:0]S;
output Error;

wire [15:0]Test_Vector,Test_Vector1;
wire [15:0]Sum_Conventional,Sum_Proposed;

Test_Vector TV (.Clk(Clk),.Rst(Rst),.Out(Test_Vector));
assign Test_Vector1={Test_Vector[15:8],~Test_Vector[7:4],~Test_Vector[3:0]};

Conventional_CSA16 M0 (
.A(Test_Vector),
.B(Test_Vector1),
.So(Sum_Conventional)
);

Proposed_ETA_DACA- POSSITVE & NEGATIVE 1 M1 (
.A(Test_Vector),
.B(Test_Vector1),
.S(Sum_Proposed)
);
//Error detection

assign Error = (Sum_Proposed==Sum_Conventional)?1'b0:1'b1;

always @ (Sum_Proposed,Sum_Conventional,Error)
begin
if(Rst)
S=16'd0;
else if (Error)
S=Sum_Conventional;
else
S=Sum_Proposed;
end

endmodule
```

X. XILINX RESULTS

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	17	7,168	1%	
Logic Distribution				
Number of occupied Slices	10	3,584	1%	
Number of Slices containing only related logic	10	10	100%	
Number of Slices containing unrelated logic	0	10	0%	
Total Number of 4 input LUTs	17	7,168	1%	
Number of bonded IOBs	24	97	24%	
Total equivalent gate count for design	105			
Additional JTAG gate count for IOBs	1,152			

POWER RESULTS

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		463
Vccint 1.20V:	354	425
Vccaux 2.50V:	15	38
Vcco25 2.50V:	0	0
Inputs:	264	317
Logic:	30	36
Outputs:		
Vcco25	0	0
Signals:	41	50
Quiescent Vccint 1.20V:	19	23
Quiescent Vccaux 2.50V:	15	38

COMPARISON REPORT FOR MULTIPLIER:

METHOD NAME	AREA IN NUMBER OF LUT			pOWER mW	DELAY		
	LUT	GATE COUNT	SLICES		DELAY	GATE OR LOGIC DELAY	PATH OR ROUTE DELAY
DEVICE NAME Spartan 3s200 tq144-4							
Conventional CSA 16 Bit	28	174	18	463	16.769ns	9.841ns	6.928ns
Proposed_ETA_DACA- POSSITIVE & NEGATIVE 16 Bit	30	183	21	321	29.245ns	14.249ns	14.996ns

XI. CONCLUSION

The proposed high performance DACA- POSSITIVE & NEGATIVE and 8-bit DACA- POSSITIVE & NEGATIVE s for 8-bit pixel depth grayscale image processing applications. The PDP and ADP of the DACA- POSSITIVE & NEGATIVE are less than the existing conventional RCA approach. Moreover, the proposed DACA- POSSITIVE & NEGATIVE 1 offers a savings ADP than the existing conventional RCA. The proposed 8-bit DACA- POSSITIVE &

NEGATIVE 1 shows better quality and design metrics with respect to the existing ETA approaches. Future research extension for the proposed method can be directed towards integrating and analyzing these designs in a multi-core environment for real-time 8-bit pixel depth grey-scale images and colour plane image processing applications.

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