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Design A Full Adder with XNOR -XOR Based Double Pass Transistor Logic

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ABSTRACT: Many arithmetic circuits depend on the XNOR-XOR circuit. This study presents a 4T XNOR-XOR circuit and an 8T full-adder circuit. The size and power consumption are incredibly low because of the suggested circuits' extremely low output capacitance and little short-circuit power dissipation. The suggested full adder is developed at an intricate transistor level for quantitative comparison with less transistors. With double pass transistor logic, an optimized simultaneous XNOR-XOR circuit is used in the suggested full adder design framework. 45nm CMOS technology is used in MICROWIND EDA TOOL to model the design. The results show that, in comparison to conventional approaches with optimal design, the proposed design uses less area and electricity.

KEYWORDS: XNOR-XOR, Full adder, double pass transistor logic, microwind eda tool

I. INTRODUCTION

One of the main issues in recent years has been the exponential growth of portable technology. The main problem with the VLSI system is power because most portable devices run on batteries. Performance restrictions apply to all application-specific integrated circuits (ASIC) processors. Electronics are permeating practically every area of daily life. Digital circuits, including microprocessors, digital signal processors, and digital communication devices, make up the majority of electronic systems. As the scale of integration increases, the utility of circuits is limited by rising power and area consumption.

The efficiency of various arithmetic circuits, such as divisions, adders, and multipliers, is important for digital application performance. Numerous efforts have been undertaken to examine efficient adder topologies, including carry choose, carry skip, conditional sum, and carry look-ahead adders, due to the significance of addition in all mathematical operations. The main focus is on the Full Adder (FA), which is the fundamental component of these architectures. As the scale of integration increases, the utility of circuits is limited by growing power and area consumption. Since addition is required for all mathematical operations, numerous studies into effective adder designs have been conducted.

The primary focus of interest is the full adder (FA), which serves as the foundation for these inventions. Full-swing and non-full-swing FA circuits are distinguished by the output voltage magnitude. The complementary pass-transistor logic (CPL), transmission gate (TG), transmission function 14T (14 transistors), and hybrid pass logic with static CMOS output drive full adder (HPSC) FAs are the most well-known full-swing families. TenT, NineT, and EightT are the three non-full-swing categories. A hybrid FA is made up of two modules: a 2:1 and a 2-input XOR-XNOR gate. multiplier. The primary FA cell gate is the XOR-XNOR gate energy user. Consequently, the power consumption of the FA cell may be reduced by building the XOR-XNOR gate as efficiently as possible. There are several different types of digital circuit designs that use the XOR-XNOR gate. Many circuits have been proposed to build the XOR-XNOR gate. The conventional full adders used in ALUs use about 28 transistors, which raises the area, output delay, and power consumption. Consequently, developing efficient full adders is essential to a system's proper operation. The improvement includes reduced transistor count, reduced power usage, and faster operation. The following formulas [8] are used to realize the outputs Cout and Sum of the conventional CMOS complete adder architecture with the inputs A, B, and Cin.

$$Cout = A.B + Cin.(A+B)$$

$$\text{Sum} = A.B.C_{in} + C_{out}.(A+B+C_{in})$$

By utilizing both NMOS and PMOS transistors, Double Pass Transistor Logic (DPL) gates improve circuit performance at lower supply voltages. Because DPL gates are symmetric, the load in any DPL gate is dispersed equally among the inputs. The symmetry of the DPL XOR/XNOR gate is perfect. According to the DPL gates' expected high efficacy in wave pipelined circuits, the twin transmission feature and the symmetrical arrangement. For every set of inputs, a dual current path is made utilizing transistors, namely PMOS and NMOS, yielding the lowest comparable resistance for DPL gates in relation to alternative logic kinds. The complementary pass-transistor logic (CPL) problems of noise margin and speed loss at low supply voltages are addressed by PMOS transistors. are integrated using NMOS transistors in parallel. Furthermore, Basic DPL logic gates ought to have consistent propagation delays, allowing for their time-equalized application. uses such as wave pipelining. A lot of scientists are emphasizing the significance of circuit performance with the fewest transistors possible. The XOR-XNOR circuit is the basic building block of the F-A circuit. The F-A design's enhanced performance can significantly enhances an XNOR-XOR circuit's performance. There are several advantages to different logic systems, depending on the dimensions, power usage, speed, and wiring of the circuit complexity.

This essay is divided into multiple pieces. Sections 2 and 3 analyze the current technique and the suggested methodology, and the findings and conclusion are discussed as a whole in sections 4 and 5, then references.

II. EXISTINTG METHOD

A. XOR-XNOR Circuit:

The two modules that comprise hybrid FAs are a 2-to-1 multiplexer (2-1-MUX) gate and a 2-input XOR/XNOR gate. The XOR/XNOR gates in the FA cell are the primary energy consumers. As a logical extension, by refining the XOR-XNOR design gate, the FA cell's power usage will be kept to a minimum. XOR-XNOR gates are essential when creating digital circuit designs. The XOR-XNOR has been implemented using multiple circuits. gate. The concurrent XOR-XNOR circuit has witnessed a great deal of applicability in more contemporary hybrid FA designs. Signals XOR-XNOR are commonly sent to the 2:1 MUX's inputs as select lines in hybrid football teams. For the FA output nodes to remain error-free, two . It is necessary to provide simultaneous signals with the same latency. The nonfull-swing XOR-XNOR circuit has good power and latency architecture. This work presents the optimized XOR-XNOR and describes the circuit shown in Fig. 1. gate to deal with the problem of output voltage drop with a single logical input value. This structure generates a full swing for every possible combination of inputs. The suggested XOR/XNOR gate on the circuit's crucial route does not have any NOT gates. Consequently, there will be reduced delay and improved the ability to drive. Given that one ought to be linked to the one to the diffusion of a nMOS and the other to the input of NOT gates transistor, the XOR circuit's input A and B capacitances are not balanced. Furthermore, in the best of situations, The input capacitances of transistors N2 and N3 are different from mutually (minimum PDP).

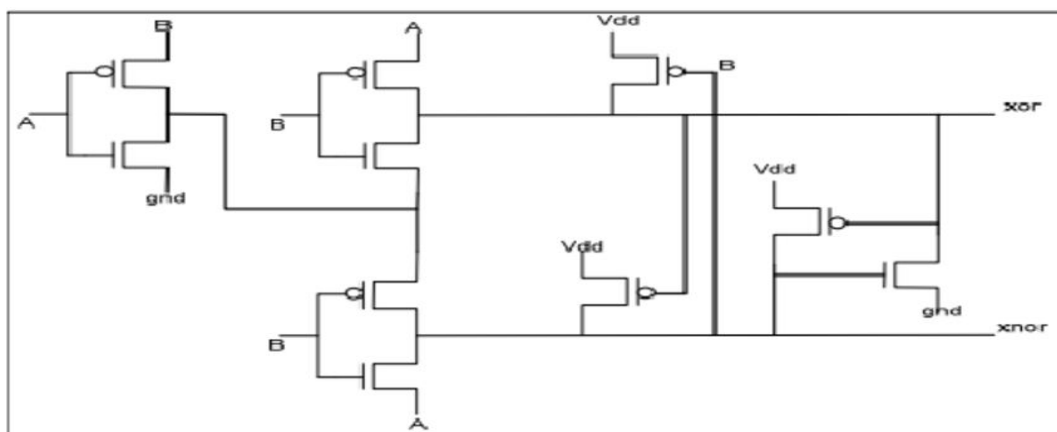


Fig . 1 . XOR-XNOR Gate

Moreover, the operation of the circuit is unaffected by the sequence in which the input connections are made to transistors N2 and N3. The transistor whose input capacitance was lower. Consequently, it need to be linked to input A, which is similarly connected to the gates of NOT. Thus, the input capacitances are higher. symmetrical, and the circuit's power usage and latency are reduced.

B. Existing Full Adder:

The alternative XNOR or XOR signal can be produced using an XOR/XNOR gate and a NOT gate, which will lower the FA structures' power consumption. The XOR gate from Figure 1 was used to create the hybrid FA cell (HFA-17T) seen in Figure 2. This system contains 17 transistors. Due to the addition of NOT gates to the critical route, which are required to convert the XOR signal into the XNOR signal, the HFA-17T exhibits a notable delay. The HFA-17T should use less power as a result of having fewer transistors.

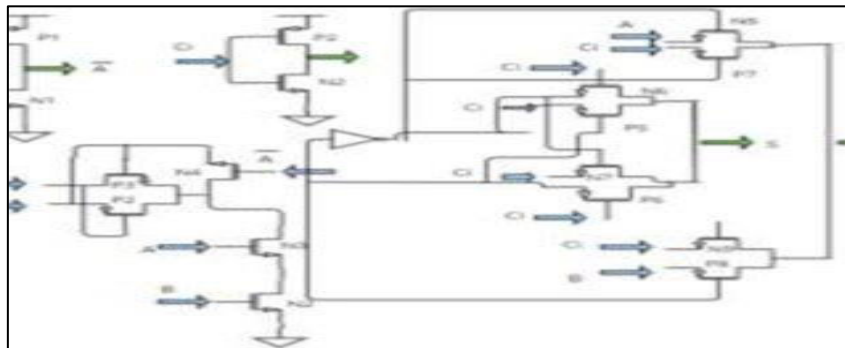


Fig . 2 . HFA-17T

Additionally, the circuit's critical route NOT gate raises the short circuit power. Consequently, there is no discernible reduction in the HFA-17T's power dissipation. Additionally, the NOT gate will help the circuit drive outputs a little bit better. As previously indicated, a buffer must usually be used at the output of a circuit, particularly if the output capacitance of each stage is considerable. The driving capability of the VLSI circuit actually declines with time because of the growth of parasitic capacitors and resistors as well as the rising threshold voltage of transistors, even though the output buffer improves this condition [11]. The HFA-17T circuit was created using the least amount of transistors possible.

III. PROPOSED METHOD

Reducing the power consumption of the traditional F-A circuit is the main goal of the recently developed F-A circuit that makes use of the XNOR-XOR circuit.

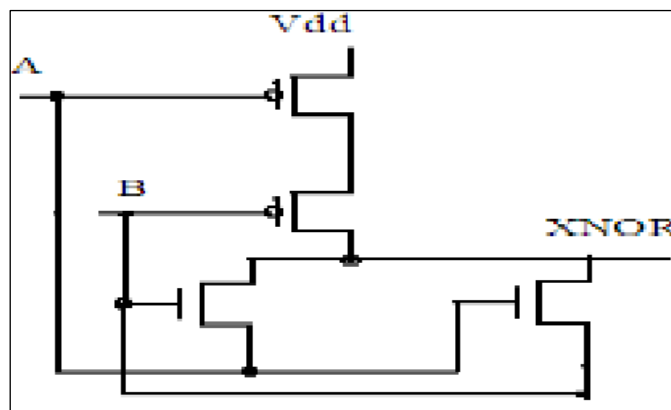


Fig . 3 . 4T XNOR-XOR GATE

A. Circuits of XOR-XNOR:

In order to fix the aforementioned mistakes, an XNOR-XOR circuit was rebuilt. The logic of a double pass transistor (DPL) is utilized to put the intricate design into practice. The XNOR-XOR circuit combination shown in Table I is indicated by the reasoning below: These are the reasoning for formulae for the circuitry that was designed:

$$\begin{aligned}
 A \oplus B \oplus C &= (A \oplus B) \oplus C \\
 &= (AB' + AB) \oplus C \\
 &= (A'B + AB')Z' + (X'Y + XY')Z \\
 &= A'BC' + AB'C' + (A'B)'(AB)'Z
 \end{aligned}$$

Table I. The Function of Xnor/Xor Gate

A	B	C	XOR	XNOR
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

B. Proposed Full Adder

The following mathematical formula results in the suggested F-A cells using the proposed XNOR-XOR circuit: Additionally, the outputs Sum and Carry are calculated with three inputs.

$$\text{Sum} = A \oplus B \oplus \text{Cin} \dots\dots\dots (4)$$

$$\text{Carry} = A \oplus B + \text{ACin} \dots\dots\dots (5)$$

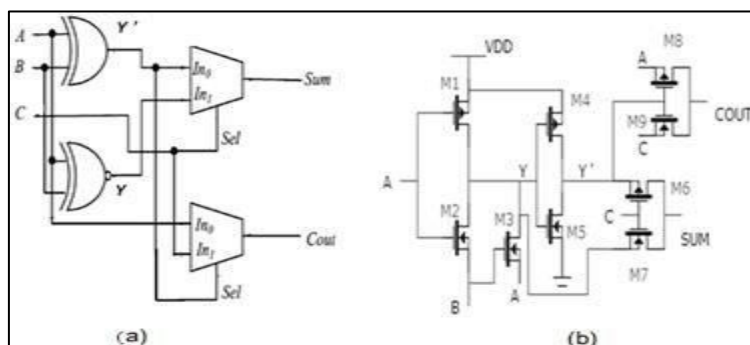


Fig.4. Proposed Full Adder using XNOR-XOR

The suggested XNOR-XOR circuit is depicted in Figure 3. Unfortunately, this XNOR-XOR circuit produces poor high output logic for some input combinations. To fix these problems and get the desired result again, the width-length ratios of the pmos and nmos transistors are changed. The recommended F-A circuit was made up of two modules: a series of multiplexers and an XNOR-XOR circuit. The 4T XNOR-XOR circuit is introduced to improve the efficiency of the current F-A. The XNOR-XOR circuit is a vital component of the F-A, as demonstrated by equations (3) and (4) above. To lower the traditional F-A circuit's power usage, a recently the XNOR-XOR circuit is used to create a designed F-A circuit. A overview of the planned circuit operation is shown in Table II below.

TABLE II. THE TABLE BELOW PROVIDES A SUMMARY OF HOW THE PROPOSED CIRCUIT OPERATES

S.NO	Inputs			Transistors								Outputs	
	Cin	B	A	M1	M2	M3	M4	M5	M6	M7	M8	SUM	CARRY
1	0	0	0	ON	OFF	OFF	ON	ON	OFF	OFF	ON	0	0
2	0	0	1	ON	ON	ON	OFF	ON	OFF	ON	OFF	1	0
3	0	1	0	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	1	0
4	0	1	1	OFF	ON	OFF	ON	ON	OFF	OFF	ON	0	1
5	1	0	0	ON	OFF	OFF	ON	OFF	ON	OFF	ON	1	0
6	1	0	1	ON	ON	ON	OFF	OFF	ON	ON	OFF	0	1
7	1	1	0	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	0	1
8	1	1	1	OFF	ON	OFF	ON	OFF	ON	OFF	ON	1	1

IV. SIMULATION RESULTS AND COMPARISONS

This study compares the power consumption of the suggested architecture using double pass transistor logic to that of conventional full adders with XOR-XNOR based combinations. complete adders based on XOR-XNOR. The XOR-XNOR above Microwind eda tool simulates based structures, which are shown in figs. 5 and 8 below.

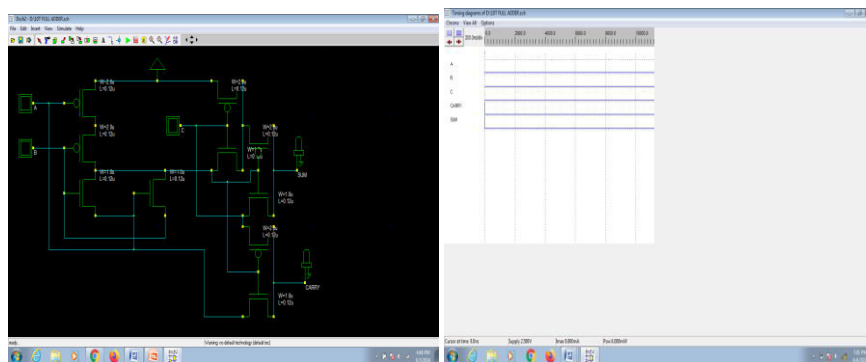


Fig. 5. Implementation Of Existing Circuit Fig. 6. Timing Diagram Of Existing Circuits

TABLE III. COMPARATIVE RESULTS OF EXISTING METHOD AND

Voltage	Existing Power	Proposed Power
1.2V	319.203μW	11.3492nW
2.5V	2.3708mW	683.1026μW

The accompanying table compares the circuit power for two different supply voltages using the suggested approach and the present method. One had 2.5V, whereas the other 1.2V. The current method's power consumption at 1.2V is 319.203uW as opposed to 11.3492nW in the suggested technique. Within the In a similar vein, the proposed method uses 683.1026nW of power at 2.5V, while the current method uses 2.3708mW. Consequently, the The cases listed above show that there is a substantial reduction of power consumption with fewer transistors.

V. CONCLUSION

This study offers a double pass transistor logic based 8T XNOR-XOR complete adder. Two operating voltages of 1.2V and 2.5V are used to simulate the design. The assessment of the design simulated in cadence shows a notable power minimization with the use of transistor logic with double pass in contrast with traditional techniques. The resulting graph of power analysis, DC, and transient response show that DPL provides the fastest operating speed that is similar to conventional reasoning. Pipelining to the smallest grain is possible with it minimal power, space, and delay overhead as opposed to conventional techniques.

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