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Efficient SoC Integration with High Performance and Minimal Leakage Using Multi-Vt Technology

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ABSTRACT: This paper proposes a total power and delay optimization flow at synthesis stage and CTS (Clock Tree Synthesis) stage of VLSI Design flow. Multiple Vt design approach is required for reducing leakage current. In this Paper, two combinations of Vt are used: 1. High Vt and 2. Low Vt for the same logic function. The third type is nominal Vt is optional in this flow, Implementation flows use different approaches to use mixture of different flavors of cells in the design to make trade-off between leakage and performance targets. In this paper RTL synthesis and logic optimization will be performed using LVT cells to optimize timing with high speed cells for meeting the timing target. Then once the delay is met, the leakage power optimization will be implemented with target slack of zero and leakage power optimization will be done with only HVT cells.

KEYWORDS : Synthesis, skew, Insertion delay, Latency, Clock Tree Synthesis (CTS), System on Chip (SoC), Slack

I. INTRODUCTION

When a CMOS cell output is stable in SoC, ideally only the PMOS section or the NMOS section is conducting and in principle no current flows from supply to ground. However, a small amount of current does leak through the non-conducting section. One effect of advanced technologies is that leakage current is becoming Significant, and might even be a major contributor to power consumption. Silicon foundries are now providing multiple-threshold-voltage (multi-Vt) libraries, which allow designers to reduce power consumption due to leakage current.

As the design size is shrinking to the ultra-deep sub microns and density is increasing to millions of gates in a system on chip, large power dissipation in the chip due to sub-threshold leakage is becoming uncontrollable in the practical world. It is taking more importance as it is becoming dominant component for the overall power in the chip. There have been many researches going on recently to extend the battery life as the hand held mobile devices are densely packed with multiple functionalities.

The delay of logical gates increases with the increase in threshold voltage (High Vt), whereas the static power decreases with the increase in threshold voltage. This can be represented by a simple gate delay equation:

$$\text{Delay, } T_d = (CLV_{dd}) / (V_{dd} - V_t) \alpha$$

In the equation, T_d represents the propagation delay, CL is the load capacitance, V_{dd} is the supply voltage and V_t is the threshold voltage for the transistor. α is the coefficient and represents the effect due to shortening of the device channel length (scaling down technology).

The leakage current of a MOS transistor can be approximated as follows:

$$I_{\text{leak}} = A e^{q(V_{gs} - V_{th})/nkT} (1 - e^{-qV_{ds}/kT})$$

where, $A = \mu_0 C_{ox} (W_{\text{eff}}/L_{\text{eff}}) (kT/q)^2 e^{1.8}$

C_{ox} = Gate oxide capacitance per unit area

V_{th} = Threshold voltage

Leakage exponentially varies with threshold voltage.

Lower-Vt devices are needed to cater the performance targets Engineers to make right trade-off between leakage power Vs performance targets.

All the above factors that are being discussed are needed to be considered carefully at each level of design abstraction for the deep sub-micron SoC designs. In this paper, I have proposed a total power and delay optimization flow at synthesis stage and CTS stage. At Synthesis stage I have proposed flow using multi-Vt library (Swapping of cells) which uses HVT (High threshold voltage), LVT (Low Threshold Voltage) and RVT (Regular Threshold voltage) cells. To build a clock tree I have proposed a flow using multi-Vt library which includes pure HVT, pure RVT and pure LVT cells.

II. MULTIPLE Vt LIBRARIES FOR LEAKAGE AND SPEED OPTIMIZATION

Multiple Vt design approach is required for reducing leakage current. Multiple Vt design is one of the important methods to design the deep submicron circuits in the power constrained era. Multi-Vt Library consists of different standard cells with different threshold devices.

- HVT cells – High Threshold Voltage cells
- RVT cells – Regular Threshold Voltage cells
- LVT cells – Low Threshold Voltage cells

A. Multi-Vt Library Profiling

I_{dsat} and I_{off} values of different threshold voltage transistors to be studied to understand the impact of leakage values of different flavors of cells. I_{off} values are indicators of leakage numbers and they varied as following:

HVT – 1X

NVT – ~20X

LVT – ~50X

I_{dsat} values are the indicators of device performance.

Sequential cells shown comparatively less variation than combinational cells but sequential cells contributed maximum leakage due to large number of devices. Selective use of NVT/LVT cells reduces leakage power while still meeting the same performance targets

In this flow, two combinations of Vt are used: 1. High Vt and 2. Low Vt for the same logic function. The third type is nominal Vt is optional in this flow. This is the minimum requirement in the technology library in order to pursue the leakage power optimization. No other changes in the design procedures are required as the technology mapping handles them in order to utilize the multiple Vt technology.

Combinations of high Vt and low Vt can be used to characterize the complex Vt cells in the library apart from just high Vt and just low Vt cells. The library size would be reasonably larger in this kind of characterized libraries. One more important thing to note is that the constant leakage power in the library would slowly go away as the constant models are not accurate for 90 nm and below.

B. Design Flow

Implementation flows use different approaches to use mixture of different flavors of cells in the design to make trade-off between leakage and performance targets. Here in this design flow (Fig. 1) shows that, Once the data is available, RTL synthesis and logic optimization will be performed using LVT (low threshold voltage cells) to optimize timing with high speed cells for meeting the timing target first because LVT cell has less delay but it has more leakage power. Then once the delay is met, the leakage power optimization will be implemented with target slack of zero and leakage power optimization will be done with only HVT cells (which has low leakage power but it has more delay). So, it is necessary to swap HVT Cells with LVT cells. The path which is timing critical in that path only LVT cells are used so it reduces the delay.

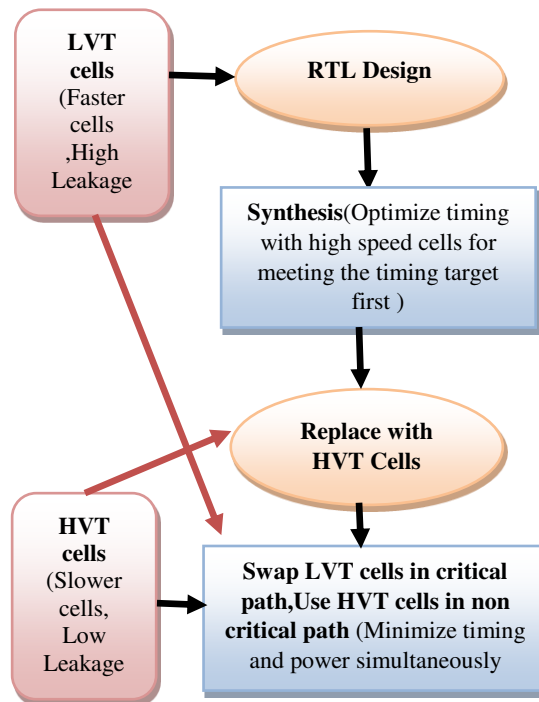


Fig 1. Shows the design flow for swapping of LVT to HVT to LVT

C. Normalized delay and leakage current for a cell with different threshold voltages in 90nm Technology:

TABLE 1:

NORMALIZED DELAY AND LEAKAGE CURRENT FOR A CELL WITH DIFFERENT THRESHOLD VOLTAGES IN 90NM TECHNOLOGY

Cell	HVT	RVT	LVT
Delay	663.6 ps	463.3 ps	374.9 ps
Leakage Power	1.7 nW	9.2 nW	23.8 nW

This Table 1 introduces the delay and leakage power for 90 nm technology for HVT, RVT, LVT cells. It shows that the delay of HVT cell is maximum and leakage power of HVT cells is minimum compared to other cells, and the delay of LVT cell is minimum and leakage power of LVT cell is maximum.

III. DESIGN EXPERIMENTS WITH MULTI-VT LIBRARIES

A. Design experiments with multi-Vt libraries at Synthesis stage

- **Synthesis:** Translation + Mapping + Optimization



- **Translation:** It is Process that generates a gate-level netlist for an IC design that has been defined using a Hardware Description Language (HDL)
- **Mapping:**It maps to particular technology library
- **Optimization:** It is Step in the synthesis process that attempts to implement a combination of library cells that best meet the functional, timing, and area requirements of the design

Table 2 shows the experiment done at synthesis stage using multivt library.

This table 2 shows the results of gate count, slack and leakage power using pure HVT, pure LVT and pure RVT and using all three cells at synthesis stage

From this table 2, Three Vt’s add one more dimension to performance/power optimization, Leakage power can be saved, Silicon area is also improved. So, at synthesis stage best option is to use HVT and LVT cells, because using that we can meet the timing, slack is positive and leakage power is also controlled. So best way is to use the swapping of HVT and LVT cells (Use HVT cells in timing non critical path and use LVT cells in timing critical path. This Table2is the results from the multivt design flow.

TABLE II
DESIGN EXPERIMENTS WITH MULTI-VT LIBRARIES AT SYNTHESIS STAGE

Cell	Pure HVT cells	Pure RVT cells	Pure LVT cells	LVT and HVT cells			LVT,RVT and HVT cells		
				LVT	RVT	HVT	LVT	RVT	HVT
Gates	99197	111617	100089	52889		58617	44569	39121	49516
Gate Count	99197	111617	100089						
Slack	-267ps	-100ps	>0ps	0ps			0ps		
Leakage Power	456uw	561uw	768uw	296uw			321uw		

B.Design experiments with different threshold voltage cells at CTS Stage (Clock Tree Building).

CTS develop the interconnect that connect the system clock to all the cells in the chip. Goals of CTS:

- Minimizing Clock skew
- Minimizing Insertion delay
- **Skew** is the difference in arrival of clock at two consecutive pins of a sequential element.
- **Insertion Delay:** The delay from the clock definition point to the clock pin of the register

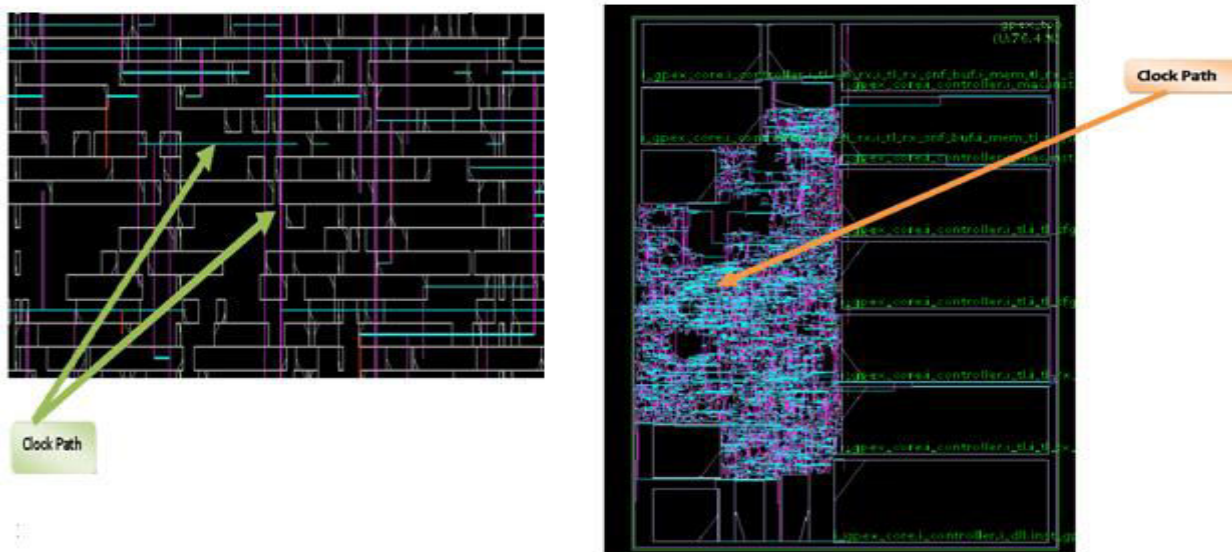


Fig.2.clock tree synthesis stage

TABLE III

RESULT OF SLACK ,SKEW ,LATENCY ,LEAKAGE POWER,INSERTION DELAY AT CTS STAGE.

Cell	HVT	RVT	LVT
Gate Count	117610	118853	118714
Slack (late)	-3056 ps	-859 ps	-690ps
Insertion Delay	1583 ps	1382 ps	1404 ps
Skew	318 ps	277 ps	167 ps
Latency	1511 ps	1314 ps	1154 ps
Slack (early)	-356 ps	-277 ps	-126 ps
Leakage Power	556.8 uW	680.1 uW	859.8 uW

Table 3 shows the results at CTS (Clock Tree Synthesis) stage. CTS is done with the using only HVT cells, LVT cells and RVT cells. From this Table 3,

- 1) If CTS is done with only HVT cells then delay of that path will be more but leakage power is less than other two cells.so here leakage power is controlled.

- 2) It CTS is done with only RVT cells then delay and leakage both will increase
- 3) If CTS is done with only LVT cells then delay of that path is controlled ,but leakage power increases.

So best way is to use LVT cells to build CLOCK TREE.

III.CONCLUSION

In this paper, we have proposed the methodology to combine placement, gate sizing, and multiple-Vt cell swapping algorithms for leakage and total power optimization. The proposed simplistic power optimization script based on Flow experiments using multiple Vt technique and multivt swapping at synthesis stage achieved not only maximum sub threshold power benefits, but also met circuit speed and area reduction to the design. At Synthesis stage best way is to use the HVT and LVT cells using the multi v swapping flow. At CTS stage best way is to use LVT cells to build clock tree. This methodology can find the best optimal trade-off point between power and delay keeping the performance of the nanometer design.

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