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Survey Paper on Combinational Circuit using Programmable Reversible Gate

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ABSTRACT: Today security in digital computing and communication is of prime importance and therefore, cryptography protocol plays a major role. Reversible logic has emerged as one of the most important approaches and more prominent technology nowadays. Power is the main concern for development and growth of modern VLSI designs. In recent years, the growing market of electronic systems suffers from power dissipation and heat removal problem. If more and more power is dissipated, System becomes overheated which in turn reduces the lifetime of the electronic devices. Reversible logic has also promising application in an online and offline testing of faults. Reversibility circuitry is having its application in following areas: low power consumption, quantum computing, and communication and Nano technology. In this paper the study of different reversible gate and combinational circuit.

KEYWORDS: Reversible Gates, Power Dissipation, Combinational Circuit

I. INTRODUCTION

Most traditional computers lose information in the process of computation. Consider the simple two input Boolean AND gate: Observing an output of 0 does not give enough information to identify the input combination that gave rise to the output. In fact, any one of three different input combinations (00, 01, 10) would force the output of the AND gate to 0. In computing the logical AND of two bits, a traditional AND gate would discard that input information. The only inherently logically reversible traditional primitives include the wire and inverter. The conclusions of Landauer and Bennett show that an energy loss of $kT \ln 2$ joules in the form of heat unavoidably accompanies each bit of information discarded during computation, and that a completely reversible computer is theoretically possible [1, 2]. Only by performing the computation in a logically reversible manner can energy dissipation fall below $kT \ln 2$ joules per bit per cycle.

Power crisis is a vital problem in today's world. In recent years, the growing market of electronic systems suffers from power dissipation and heat removal problem. If more and more power is dissipated, system becomes over heated which reduces the life time of the electronic system. The need of microelectronic circuits with low power dissipation leads to the implementation of reversible logic circuit. Bennett [3] proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and heat dissipation of a circuit. Today security in digital computing and communications is of prime importance and therefore cryptographic protocols play a major role.

There are four major design parameters of reversible circuits. First is the quantum cost which is the number of basic quantum gates like Controlled NOT, Controlled V+ etc. in the reversible circuit. Second is the quantum depth also called quantum delay [4]. Third is the number of ancillary inputs or ancilla inputs which are constant inputs which are used to maintain the reversibility of the device. Fourth is the number of garbage outputs i.e. output signals which are not used as inputs to other gates and are only there to maintain reversibility.

II. REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

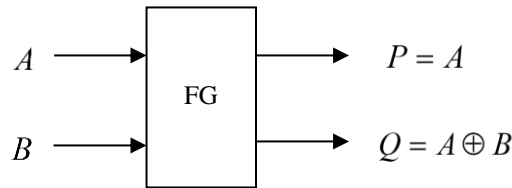


Figure 1: Feynman gate

In figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

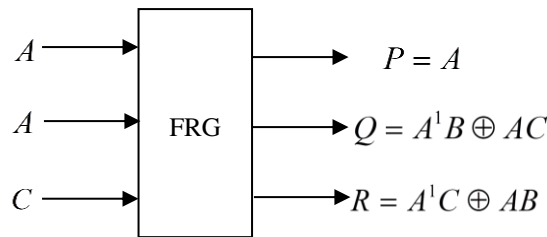


Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

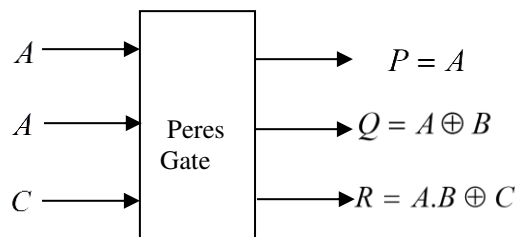


Figure 3: Peres gate

The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \tag{1}$$

$$Q = B \tag{2}$$

$$R = A \oplus B \oplus C \tag{3}$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \tag{4}$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

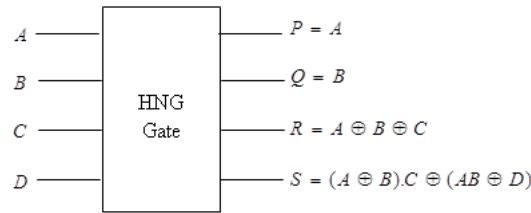


Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A \tag{5}$$

$$Q = A \oplus B \tag{6}$$

$$R = AB \oplus C \tag{7}$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \tag{8}$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for PAOG realization.

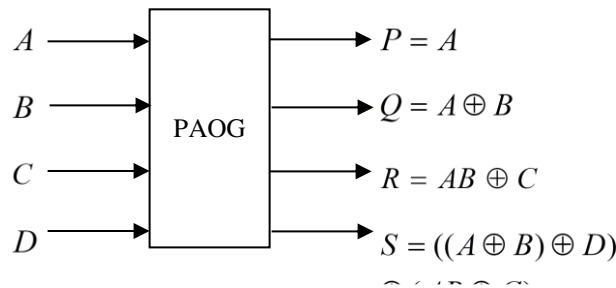


Figure 5: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

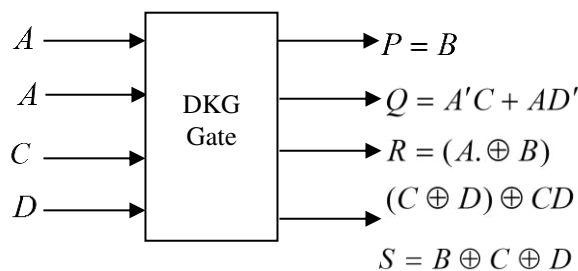


Figure 6: DKG Gate

$$P = B \tag{9}$$

$$Q = A'C + AD' \tag{10}$$

$$R = (A \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

III. LITERATURE REVIEW

Patthi Aruna et al. [1], low power designs are more articulated for various applications that reach out from Web of Things to Quantum figuring. Crude combinational rationale circuits actuate from digit cancellation because of data misfortune during the handling of info data which brings about energy misfortune. The calculations including reversibility drop the deficiency of data by supporting the information bits from yield. In the essential math and rationale units, the combinational circuits assume a huge part in deciding the presentation of the processor. The standards associated with the plan of reversibility are an impending innovation for super low power applications. The reversible rationale circuits outfit a completely better approach to advance in Quantum registering. In this article, we propose an energy lenient low power reversible multiplexer with ideal energy misfortune. The proposed multiplexer additionally diminishes the ancillae, trash results and quantum cost significantly.

S. K. B. C. Naik et al. [2], the reversible Rationale framework will be successful in low power dissemination. For the streamlining of force in VLSI configuration, number of scientists is utilizing reversible rationale consistently. In the VLSI plan, the utilization of reversible rationale enjoys many benefits in light of its rapid, and low power dissemination. This paper gives the plan and near investigation of reversible full viper utilizing Peres door with traditional full snake circuits. During examination it is found that 44% improvement in absolute nuclear energy dispersal over the ordinary snake circuit. These reversible rationale circuits are confirmed and mimicked utilizing Verilog coding, Intel Quartus Prime 20.1.

Sriparna Bhattacharya et al. [3], reversible rationale doors, which are demonstrated to give zero power dispersal under ideal circumstances, are sought after for future registering advances. Utilizing reversible rationale doors, this study gives a superior plan to a minimal expense 4×4 multiplier circuit module. The module can execute 8×8 , 16×16 and up higher request multiplier circuits. As far as entryway counts, trash yields, consistent sources of info, and quantum cost, the recommended multiplier circuit utilizing least number of half adders and full adders succeeds existing plans. Also, this idea can be utilized to carry out various complex frameworks in the area of nanotechnology. The RTL plan of the proposed multiplier circuit is then shown, trailed by a reenactment waveform that outlines how the plan functions. The Xilinx ISE 14.7 programming instrument is likewise used to assess trial results in view of the on-chip power, delay, and other pertinent boundaries.

Alharbi et al. [4], the quantum-spot cell automata (QCA) address arising nanotechnology that is ready to supplant the ongoing corresponding metal-oxide-semiconductor computerized incorporated circuit innovation. QCA comprises an incredibly encouraging semiconductor less worldview that can be downscaled to the sub-atomic level, accordingly working with tera-scale gadget coordination and very low energy scattering. Reversible QCA circuits, which have reversibility supported down from the sensible level to the actual level, can execute figuring tasks dispersing less energy than the Landauer energy limit ($kBT \ln 2$). Time synchronization of rationale doors is a fundamental extra prerequisite, particularly in cases including complex circuits, for guaranteeing exact computational outcomes. This paper reports the plan and reproduction of eight new the two sensibly and actually reversible time-synchronized QCA combinational rationale circuits. The new circuit configuration introduced here mitigates the clock postpone issues, which are brought about by the non-synchronization of rationale door data, by means of the utilization of an innately more symmetric circuit setup. The reproduction results affirm the way of behaving of the proposed reversible time-synchronized QCA combinational rationale circuits which display ultralow energy scattering and all the while give precise computational outcomes.

M. Swathi et al. [5], quantum is an arising innovation in later PCs. Reversibility is the principal benefit of quantum PCs. In regular PCs, the calculation is irreversible for example the info pieces are lost once the rationale block produces the result and info bits can't be reestablished however it very well may be finished in reversible calculation in light of the fact that in reversible calculation the data sources and results have a coordinated correspondence. Hence, a reversible entryway info might really still up in the air from their result which prompts less power utilization. Consequently the intricacy of the computerized circuits can be decreased by utilizing reversible figuring. In quantum PC to perform reversible tasks, we really want to execute the reversible doors utilizing quantum entryways. In this

paper, we talked about different reversible rationale entryways like Feynman, Toffoli, R, Peres and TR doors utilizing fundamental quantum doors like CNOT, Pauli, Trade entryways and their execution utilizing IBM quantum experience.

B. Surya et al. [6], reversible rationale configuration has cleared way for another area of examination and is acquiring a ton of exploration consideration as it is extremely helpful in different regions, for example, low power VLSI plan, quantum registering, and nanotechnology. Combinational rationale disseminates the critical measure of energy because of spot misfortune. Thus, assuming circuits are planned utilizing reversible rationale, where data pieces are not obliterated and decreased the huge measure of force scattering. Reversible circuits are planned utilizing equality saving entryways, which has the property of identifying not in excess of a solitary mistake in the circuit's essential result. In the event that a circuit is both reversible and shortcoming lenient, it can recuperate bit-misfortune at the contribution as well as touch mistake at yield. This paper presents the plan and FPGA union of enhanced information selectors. This paper additionally features the low exchanging power utilization qualities of information selectors, which were ordinarily around 1 to $3\mu\text{W}$ that finds use in low power applications are focusing on ultra-speed.

Pathak et al. [7], quantum innovation has an appealing application these days for its limiting the energy dissemination, which is a conspicuous piece of any framework level plan. In this article, the critical module of a multiplexer, a reached out to $n:1$ is outlined with noticeable application in the control unit of the processor. The proposed multiplexer modules are outlined by the calculation, which is broadened point of view based. Further, quantum cost and entryway count are less to guarantee the productive quantum registering outlined. Likewise, the QCA processing structure is an endeavor to combine the ideal natives in moderate reversible multiplexer in nano-electronic limit application. The created lemmas is outlined to demonstrate the ideal boundaries in the reversible circuit. Contrasted and existing condition of-works of art, the proposed secluded multiplexer, the door count, quantum cost and unit delay are ideal.

M. Rajeshwari et al. [8], power dispersal is becoming serious issue as gadget size is contracting. Ordinary circuits are irreversible in nature and disseminate power for each piece misfortune in circuit. All things considered in the event that we utilize reversible rationale power dispersal can be diminished. The paper is planned to plan and execution of 8-bit shift register utilizing reversible rationale entryways on FPGA board utilizing chipscope. The proposed 8-cycle shift register utilizing reversible rationale is streamlined as far as quantum cost, delay, number of rationale doors utilized. Quantum cost of the proposed plan makes an appearance to 8% improvement and in examination with existing work in study. The coding is finished utilizing verilog module then, at that point, recreated utilizing Xilinx Modelsim and prototyped in Spartan6 load up utilizing constant apparatus chipscope for confirmation of result.

IV. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog. VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (\leftarrow) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (\leftarrow). Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-

Gate Count (GC): The number of gates used to realize reversible circuit

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.

Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.

Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

V. EXPECTED OUTCOMES

The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

1. Design 2×4, 3×8 reversible decoder and 8×3 reversible encoder using different types of reversible gate.
2. Design 2×1, 4×1 and 8×1 reversible multiplexer and 1×2, 1×4 and 1×8 of reversible de-multiplexer using programmable reversible gate.
3. All the modules design to different device family i.e. Spartan-3, Virtex-4 and Virtex-7.

VI. CONCLUSION

Reversible logic has emerged as one of the most important approaches and more prominent technology nowadays. Power is the main concern for development and growth of modern VLSI designs. In recent years, the growing market of electronic systems suffers from power dissipation and heat removal problem. If more and more power is dissipated, System becomes overheated which in turn reduces the lifetime of the electronic devices. The area of reversible logic has received great importance in recent years because of its beneficial feature of reduction in power dissipation. This thesis represents the new methods and approaches to implement the components of the processor and modified design is to utilize advantages of existing techniques and at the same time overcoming drawbacks.

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