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# Fault-Tolerant Network-On-Chip (Noc) For Reliable System-On-Chip (Soc) Operation

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**ABSTRACT:** Networks-on-Chips (NoCs) are crucial components of high-performance multi-processor systems-on-chips, yet their increasing complexity and susceptibility to faults pose significant challenges. This project addresses the need for fault-tolerant NoCs by proposing appropriate fault models and mitigation techniques spanning circuit, architecture, and communication protocols. The project introduces fault-tolerant design methodologies at multiple levels, including the link, routing, and end-to-end communication levels. By incorporating fault-tolerant techniques at these critical junctures, the system enhances resilience against process variations, aging effects, and soft errors inherent in current and future process generations. One key aspect of the proposed method is the isolation technique, which decouples computing cores from faults in the network. By isolating faults, the technique mitigates their impact on network performance and functionality, ensuring reliable system-on-chip (SoC) operation. Ultimately, by integrating various fault-tolerant techniques, this project aims to design robust and reliable NoCs capable of sustaining high performance even in the face of increasing complexity and fault probabilities, thereby ensuring the dependable operation of SoCs in demanding applications.

## I. INTRODUCTION

As technology continues to advance, the challenges associated with chip design and manufacturing, such as process variation, wear-out effects, IR drop, and thermal hot-spots, become increasingly pronounced. In response to these challenges, a paradigm shift is emerging in which the pursuit of a perfect chip is being reevaluated in favor of strategies that tolerate and manage failures. This shift is particularly relevant in the context of Network-on-Chip (NoC) architectures, where fault tolerance is critical for ensuring reliable communication in multi-core systems. Fault tolerance in NoCs typically involves three essential steps: detection, diagnosis, and correction/reconfiguration. At various layers of the communication stack and within different components of the NoC, fault detection and handling mechanisms can be implemented. These mechanisms include link-level error coding, fault-tolerant routing algorithms, and end-to-end retransmission protocols. This work addresses this gap by formulating a comprehensive design flow for providing fault tolerance in NoCs, referred to as Fault-Tolerant NoCs (FT NoCs). By covering detection, diagnosis, and correction aspects, this design flow offers a holistic approach to fault tolerance in NoC architectures. The ultimate goal is to ensure the reliable operation of System-on-Chip (SoC) designs, even in the presence of diverse and challenging fault scenarios. Through the integration of diverse fault-tolerant techniques, this approach aims to enhance the dependability and robustness of SoCs, thereby enabling their effective deployment in critical applications where reliability is paramount.

## II. RELATED WORK

The Bullet Proof router employs N-modular redundancy (NMR), utilizing redundant hardware components throughout its design to ensure fault tolerance. However, this redundancy comes at the cost of increased area and power consumption. In contrast, the RoCo router takes a different approach by dividing the router into two separate row and column modules, each handling one dimension (X or Y). This design isolates faults within each module, allowing the

other module to maintain functionality. Nonetheless, fault tolerance in the RoCo router is achieved with some degradation in performance. The Vicis router leverages input port swapping and an adaptive routing algorithm to handle faults in inter-router links. For addressing faults within a router's data path, such as intra-router links, crossbar (XB), and virtual channel (VC) buffers, it utilizes error correcting codes (ECC) and a crossbar bypass bus. ECC, however, can only tolerate a single fault in the data path. To manage additional faults, the input port swapper and bypass bus employ reconfiguration to avoid or redirect faults to different data paths. The Repair router enhances port swapping by incorporating additional buffers, yet it can only salvage one out of two faulty ports, necessitating costly rerouting. Both Vicis and Repair routers impose a substantial area overhead of around 40–50%, respectively.

Meanwhile, the PVS router achieves fault tolerance in input ports and RC units through resource sharing, wherein buffers are shared among different input channels. However, if the shared resource, such as a demultiplexer, encounters a fault, all associated input ports become inoperable. In contrast, the DRS router adopts decoupled resource sharing to mitigate this issue. It shares multiplexers, demultiplexers, and all VC buffers of 2 or 3 adjacent input ports alongside the decoupled resource-sharing unit of each input port. Consequently, a fault in the DRS unit of one input port does not impact the functionality of adjacent input ports.

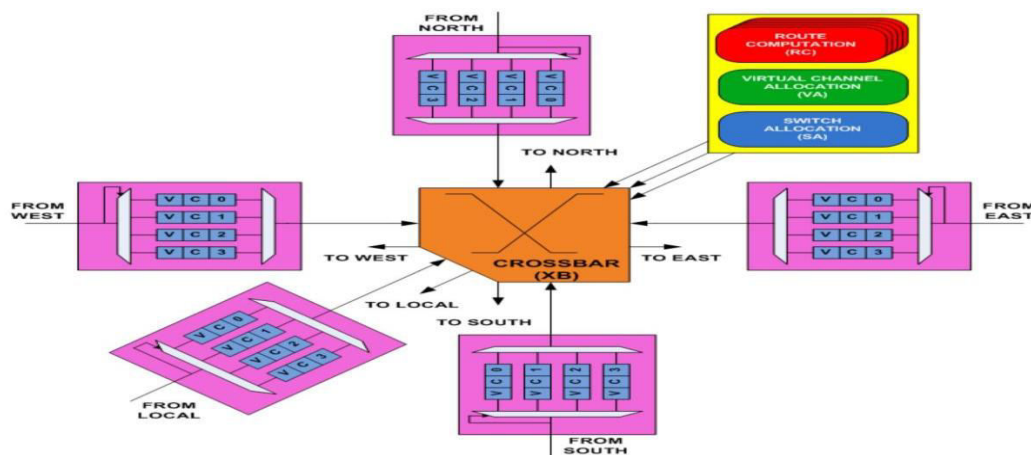


Figure 1. Generic Router.

### III. EXISTING METHOD

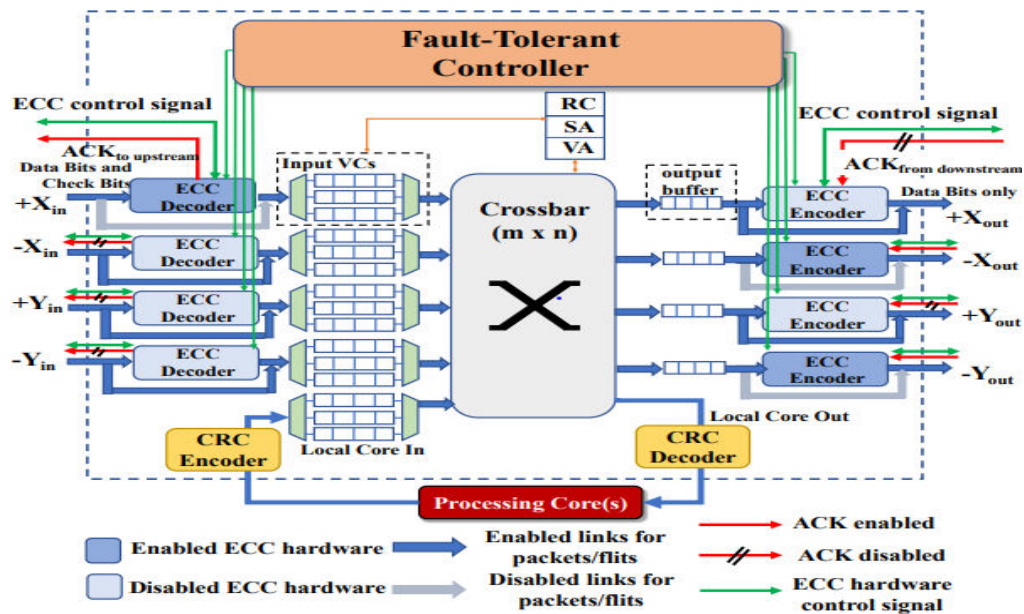
The primary aim of fault-tolerant strategies is to enhance reliability, albeit with trade-offs in terms of increased area, power consumption, and latency. Addressing fault tolerance in Network-on-Chips (NoCs) involves discussions across various layers (physical, data link, and transport) and considering different fault types, such as transient, permanent, and intermittent. While numerous techniques have been proposed in literature to address specific challenges, there remains a scarcity of comprehensive solutions that tackle the overall reliability of the NoC platform.

#### PROPOSED SYSTEM

In this project, we propose an integrated approach to fault tolerance across different layers, aiming to synergistically combat transient, intermittent, and permanent faults in real-time scenarios. We consider the trade-offs in area, power consumption, and delay when selecting these techniques. Our suggested fault-tolerant router dynamically manages the activation and deactivation of ARQ+ECC hardware (Automatic Retransmission Query + Error Correction Codes) to adapt to changing fault conditions. Unlike conventional fault-tolerant router designs, our approach incorporates a per-router fault-tolerant controller and output flit buffers. To facilitate understanding, we introduce simplified concepts using a router diagram, showcasing only ECC units. For clarity, we define each channel between routers and illustrate ECC-Link  $i$  as comprising the ARQ+ECC encoder of router  $i$  and the ARQ+ECC decoder of router  $i+1$ . Enabling/disabling ECC-Link  $i$  involves activating or deactivating both the ECC encoder of router  $i$  and the ECC decoder of router  $i+1$ , controlled by the fault-tolerant controller.

of router i.

**BLOCK DIAGRAM**



**IV. EXPERIMENTAL RESULTS**

As previously discussed, fault injection experiments rely on the quantification of actual faults propagated within the system. With this understanding, the designer of the SI tool has enabled the identification of these faults within the system, allowing for further calculations to be conducted based on this data. Tables 1–4 provide details on the number of propagated faults, replaced faults with new values, concealed faults within the system, failure rates, and the delay in faults propagation for each type of router buffering model, presented both in percentages and absolute quantities, separately for each network configuration.

Input buffer	Total	Real fault injections	Failed experiments	Fault propagation rate	Failure rate	
Cross talk	900	534	188	59	35	
Input buffer	Total	Real fault injections	Failed experiments	Fault propagation rate	Failure rate	
Dead clause	SET	600	237	193	39	81
Micro-operation	500	266	249	53	93	
Stuck then	300	83	46	27	54	

SEU	1800	819	244	45	29
Total	4100	1939	920	47	47

TABLE 1. Injected fault comparison based on failure rate and propagated faults

## V. FUTURE SCOPE

This study introduces a PSO algorithm for spare link placement in ASNoC topology. Adapting the PSO algorithm for applications with a large number of cores poses certain challenges. Hence, there exists an opportunity to explore the potential of alternative meta-heuristic algorithms to address this limitation.

## VI. CONCLUSION

In this project, we introduce a proactive and dynamic fault-tolerant framework that strikes a balance between fault tolerance, performance, and energy efficiency in NoC design. The framework comprises a fault-tolerant router design incorporating dynamic fault-tolerant scheme selection guided by per-router Reinforcement Learning (RL). Each RL agent (router) observes the NoC state, adjusts a control policy to dynamically enable/disable error detection/correction hardware per router, and selects the optimal operation mode among four fault-tolerant strategies. The dual objectives are to minimize overall network power consumption and latency. We present a fault-tolerant ASNoC design based on a PSO-based meta-heuristic algorithm and its FPGA implementation. Experiments are conducted for multimedia applications such as PiP, MPEG-4, MP3Encoder, and VOPD, considering link failures in the generated topology. Results are compared with existing approaches, demonstrating significant performance enhancements in both software and FPGA implementations. Future work includes exploring reconfiguration and scheduling policies for multiple FPGA-implemented applications.






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