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RTL Design and Verification of Synchronous FIFO for AMBA Protocol

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ABSTRACT: The main objective of this project is to create and verify an RTL (Register- Transfer Level) Synchronous First-In- First-Out (FIFO) module specifically for the Advanced Microcontroller Bus Architecture (AMBA) protocol. In a System-on-Chip (SoC) setting, the suggested Synchronous FIFO module acts as an essential bridge, guaranteeing smooth and coordinated data exchange between AMBA-compliant modules. Following the guidelines provided by the AMBA protocol, synchronous logic is implemented in the RTL design of the Synchronous FIFO to control read and write operations of data. This is at the abstraction level of behavior performed under three test cases. Verification of the Synchronous FIFO is a critical step to ensure its correctness and compliance with the AMBA protocol. This involves simulation and formal verification techniques to validate the functionality of the FIFO under various scenarios, including corner cases and boundary conditions.

KEYWORDS: RTL design and verification of synchronous FIFO for AMBA protocol, Synchronous FIFO, Register Transfer Level

I. INTRODUCTION

One essential element of digital systems for transient data storage and transfer across various system components is a synchronous FIFO (First-In-First-Out) system. As per the First-In-First-Out (FIFO) concept, the data that is retrieved and processed first will be the one that initially enters the FIFO. Data is transported between two clock domains—typically with differing clock frequencies or phases—while maintaining synchronisation and accurate timing in a synchronous FIFO. In systems where components are controlled by various clock signals or run at different speeds, this synchronisation is essential. When it comes to digital systems, synchronous FIFOs (First-In-First-Out) design and verification are essential components that guarantee stable and dependable data flow across different components. Designed for a synchronous FIFO module, this testbench aims to verify its features in relation to the AMBA (Advanced Extensible Interface) protocol, which is a commonly used standard for communication in intricate System-on-Chip (SoC) designs. The testbench compares expected and actual findings in a methodical manner to mimic and validate the behaviour of the FIFO. The final result, showing whether the FIFO succeeded or failed each test case, is displayed. Error counters (error_t1, error_t2, error_t3) note any disparities.

II. RELATED WORKS

[1] **Reconfigurable FIFO memory circuit for synchronous and asynchronous communication Abdel-hafeez S, Gordon-Ross A. published in : Int J Circ Theor Appl.; 49:938–952.**

We present a new FIFO (first-in first-out) architecture for both synchronous and asynchronous communication for high-speed and low-power operation. Our FIFO design is reconfigurable and scalable using a separate datapath with an 8T-Cell SRAM and control circuits, which enables specialization for different application

requirements. The datapath uses a two-phase clock system of nonoverlapping signals such that one signal increments the address pointer, while the other signal activates the memory decoder for data reading and writing. This structure halves the critical path delay and simplifies the timing operations between the memory decoder and address pointer while maintaining robustness against process-voltage-temperature (PVT) variations. Our design uses two alternative control circuits to manage separate synchronous and asynchronous operations by generating nonoverlapping control signals that drive the datapath circuit. The empty-full flag circuitry records only the state of the address pointers' rollover independent of the memory size, and, thus, improves scalability and reconfigurability. Compared to prior works, our design is 5X faster with a 2.3X lower power consumption and has a throughput of 1 Giga-Word/s. For a 64-bit word size with a free latency cycle. Additionally, our design functions clocklessly with the synthesizable structure for asynchronous communication that leverages Internet of Things (IoT) and Networks on Chip (NoCs) applications.

[2] Design of RTL Synthesizable 32-Bit FIFO Memory Shilpi Maurya International Journal of Engineering Research & Technology (IJERT) Published in :2016

The paper has presented a fifo memory design for multiple read and writes operations in a single clock domain [2], and generating fifo full and empty conditions. The paper has discussed the relevance of fifo in synchronization between input and output data [1]. we have designed, simulated and synthesized a memory using register file for minimize on-chip area, and reduce cost of memory compare then random access memory.

[3] Design, Simulation and Realization of a Parametrizable, Configurable and Modular Asynchronous FIFO Haytham Ashour Mentor Graphics, Emulation Division Published in: Science and Information Conference 2015 July 28-30, 2015 | London, UK

A new interface circuit that can transfer data efficiently between two unrelated clock domains has been developed. With a relatively low gate count, it allows fully synchronous data communication between the two domains at the mAMBAM rate of 1 datum per cycle of the lower frequency of the two no matter what the frequency ratio between the two domains. The correct operation of this circuit was verified with both gate-level and transistor-level (SPICE) simulations.

[4] Designing of 8-bit Synchronous FIFO Memory using Register File International Journal of Computer Applications (0975 – 8887) , February 2013

A parametrizable and re-configurable asynchronous FIFO design using a modular design approach is presented in this paper. The asynchronous FIFO presented is parametrized in address and data sizes. Early full and empty flag threshold values are re-configured at run-time. The design approach followed is modular in its architecture which means each module in the architecture is implementing an isolated and self-contained set of functions that can be re-used in any other system. This approach resulted in that the asynchronous FIFO itself becomes a modular design offering a modular interface to the other system level components. The re-configurability of the FIFO at run time finds its applications in applications like rate matching, re-configurable hardware and data streaming applications

[5] A New FIFO design Enabling Fully-Synchronous On-Chip Data Communication Network Muhammad E. S. Elrabaa Published in :IEEE, 2011

A synchronous FIFO design is presented in this paper. The novel memory structure presented in the design enhances the performance of the FIFO in terms of area delay and power. This structure enables the design to reduce a power consumption of 4 mw at frequency of 100MHz. The circuit components (LUTs) are utilized in the range of 5% to 66%. This circuit also reduces the delay period of 5.041ns.

[6] A Modular Synchronizing FIFO for NoCs Mark Greenstreet University of British Columbia Published in :IEEE,2009

We have presented a modular synchronization FIFO suitable for use in NoC designs. The design allows independent choices of the sender's protocol (synchronous or asynchronous), the receiver's protocol, the FIFO capacity and the time allocated for metastability resolution. Our design only uses cells that are available in a typical

standardcell library making it well-suited for use in an ASIC design flow. Even without the use of full-custom logic, our FIFOs achieve excellent throughputs of up to 1.95 Gtransfers/sec for an async-to-async implementation and 2.56 GHz operation for the synchronous-to-synchronous version when implemented in the TSMC 90nm process.

[7] A RTL Asynchronous FIFO Design Using Modified Micropipeline Xin Wang, Jari Nurmi Published in: 2006,IEEE

An asynchronous FIFO which applies four- phase handshake protocol to read or write data has been designed in Register-Transfer Level (RTL) using VHDL. The asynchronous FIFO in this paper avoids data movement in a flow-through FIFO by applying token passing scheme in its control pipelines and multiplexer in its data register bank.

Two control pipelines which base on micropipeline structure are proposed and used as the control logic for the asynchronous FIFO. An asynchronous arbiter and C-element RTL structures used in the proposed asynchronous FIFO are also presented.

[8] A Simple, Fast and Scalable Non-Blocking Concurrent FIFO Queue for Shared Memory Multiprocessor Systems Philippas Tsigas, Yi Zhang

In this paper we presented a new bounded non-blocking concurrent FIFO queue algorithm for shared memory multiprocessor systems. The algorithm is simple and introduces two new simple algorithmic mechanisms that can be of general use in the design of efficient non-blocking algorithms. The experiments clearly indicate that our algorithm considerably outperforms the best of the known alternatives in both UMA and ccNUMA machines with respect to both dedicated and multiprogramming workloads. The experimental results also give a better insight into the performance and scalability of non-blocking algorithms in both UMA and ccNUMA large scale multiprocessors with respect to dedicated and multiprogramming workloads, and they confirm that non-blocking algorithms can perform better than blocking on both UMA and ccNUMA large scale multiprocessors.

III. WORKING PRINCIPLE

We'll utilise parameterized FIFO. The FIFO SIZE in the AMBA protocol will adjust dynamically based on the burst size. A standard RTL design will require less synthesizable area in terms of LUT count. There is less processing time. Additionally, a behavioural test bench environment built with Verilog is used to verify the design using a variety of test scenarios. Clock signals are the basis for synchronous FIFO (First-In-First-Out) operations. A read pointer and a write pointer are its two primary parts. When fresh data is added to the FIFO, the write pointer advances, and when data is readout of the FIFO, the read pointer advances. The clock signal is followed synchronously by both pointers. The FIFO is regarded as empty when the read and write pointers are in the same location.

IV. BLOCK DIAGRAM

APB BRIDGE

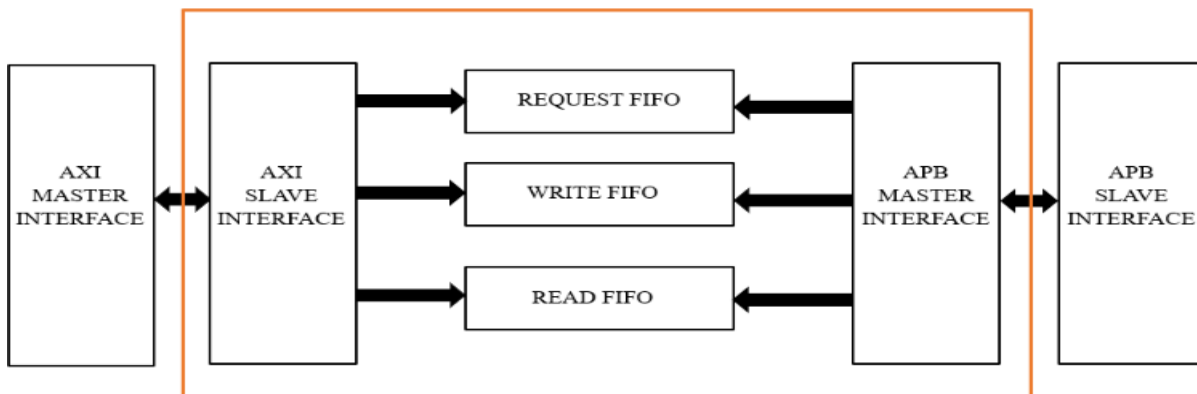


Fig 1. Block diagram for APB Bridge

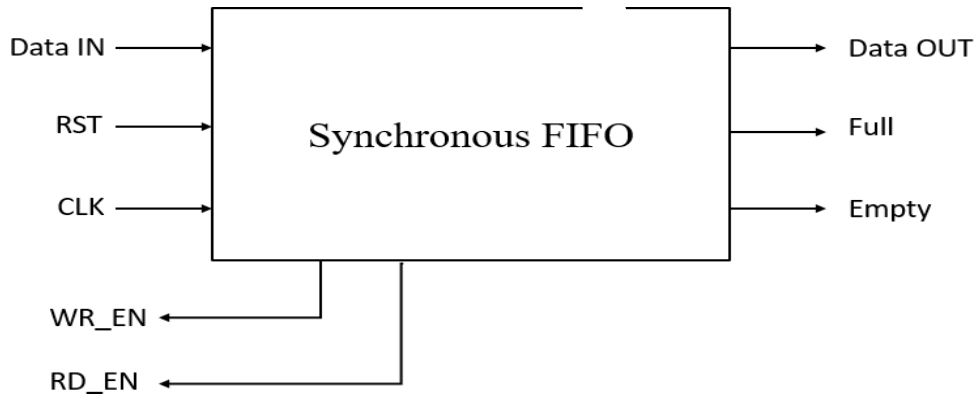


Fig 2. Block diagram of Synchronous FIFO

V. ALGORITHM

1. Initialize the parameters and define the signal.
2. Initialize and toggle the clock.
3. Assert and de assert the reset using task:rst-2_dut().
4. Initialize the memory.
5. Test case 1:task:write_all_read_all_task 1().

Data is written and verified as the data is read and the result is displayed.

6. Test case 2:task:write_5_read_5_task 2().

Data is written into the FIFO and the data is read and verified. The result is displayed.

7. Test case 3:task:write_rand_read_rand_task 3().

Random data is written into the FIFO and random data is read and verified from FIFO and the result is displayed.

8. Test results are checked and display pass/fail and the simulation is finished.

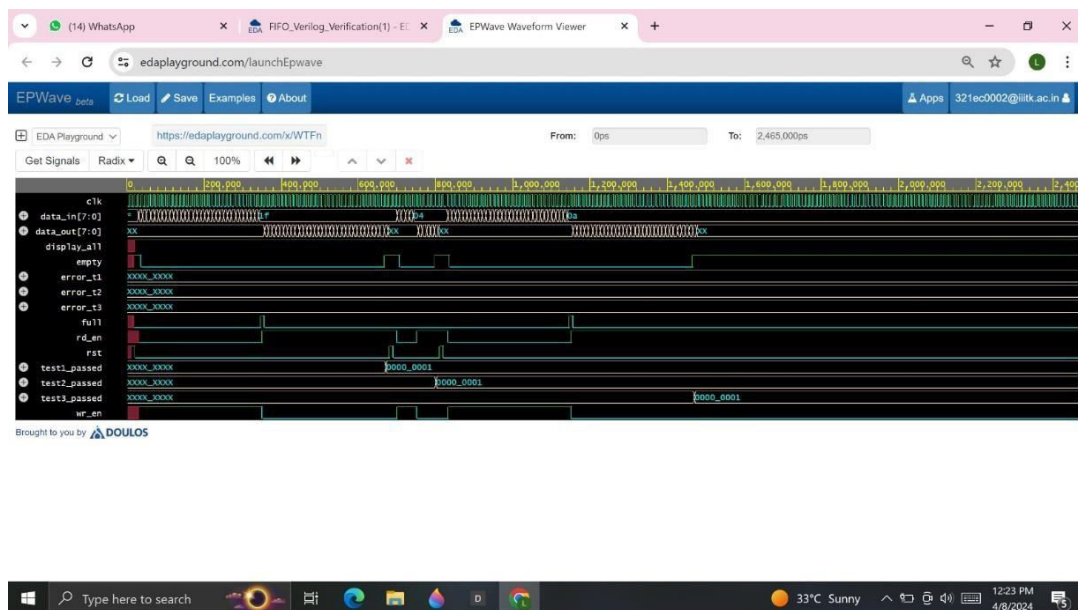
VI. SIGNAL TABULATION

Signal	Direction	Description
For FIFO		
rst	input	Reset the FIFO
clk	input	Clock input to FIFO
data_in	input	bit data input to the FIFO
data_out	output	bit data output from the FIFO
full	output	sets the FIFO when full
empty	output	sets the FIFO when empty

For FIFO memory		
wr_en	input	enable the write function
rd_en	input	enable the write function
wr_ptr	input	memory address of the address bus is stored
rd_ptr	input	memory address of the address bus is stored

VII. EXPERIMENTAL RESULT WAVEFORM

A thorough framework for confirming the accuracy and dependability of a synchronous FIFO module designed for AMBA protocol integration is offered by this testbench project. The project's methodical testing attempts to guarantee that the FIFO operates without a hitch in a variety of situations, enhancing the overall resilience and functionality of digital systems that use the AMBA standard.



VIII. CONCLUSION AND FUTURE ENHANCEMENT

The project intends to increase the overall performance and robustness of digital systems that use the AMBA standard by systematically evaluating the FIFO to make sure it operates as intended under a variety of conditions.

In order to buffer more data between two systems that may operate at various speeds or with bursty data transfer rates, it can be helpful to increase the depth of the FIFO. The throughput and latency characteristics of the FIFO can be enhanced by implementing optimisations such as pipelining, parallelism, or employing faster clock speeds.

In devices that run on batteries or have limited energy, it can be advantageous to design the FIFO to use less power. Clockgating and other techniques

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