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# Design and Simulation of Novel 8t Full Adder in CMOS Logic Style for Low Power Application

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**ABSTRACT:** To implement Complementary Metal Oxide Semiconductor(CMOS)Logic technique many logic styles are employed, One example is full adder which is the circuit one of the most important digital functional blocks used in arithmetic and logic unit. The proposed full adder design has minimum transistor count, which is employed for the generation of XOR function . The goal of this project is to design a full adder using CMOS with low consumption of power and better performance. The proposed Eight transistor full adder circuit is designed using 0.12 $\mu$ m CMOS logic style at 1.2V force voltage. DSCH is used to validate the framework of the specified circuit and Microwind tool is used for designing and simulating circuits at layout position.

**KEYWORDS:** CMOS; Eight full adder; Low transistor count; Layout.

## I. INTRODUCTION

In the fast- growing VLSI assiduity, transistor viscosity is adding with rapid-fire rate day- by- day. According to Moore's law transistor viscosity will get double itself after every eighteen months. As the number of transistors will increase, similarly area, detention and power consumption of the device will also increase. So, a technology is needed by which the area can be reduced and increase the performance of the device. From the once many decades CMOS technology is being used for designing the chips in semiconductor assiduity, but as the number of transistors are adding , area of the device and detention both are adding . So, it requires switching to a technology, which uses lower area and lower detention. Hence, the Domino sense is used for designing the one- bit full adder and compared the colourful performance parameters like area, detention, and power consumption in both technologies.

## II. FULL ADDER

Full adder circuit is one of the most important digital functional blocks used in computation and sense unit. Full adders have been designed using wide range of for enhancement of parameters like power consumption, speed performance and structure size.Full adder is the adder that adds three inputs and produces two labors. The first two inputs are A and B and the third input is an input carry as  $C_{in}$ . Full adder is the introductory block of computation circuit set up in microcontroller and microprocessor inside computation and sense unit( ALU). enhancement of the adder is essential for upgrade the performance of those circuits where adder is employed. Full adders, till now, have been designed using wide range of structures for enhancement of parameters like power consumption, speed performance and structure size. Full adder is a combinational circuit that performs the addition operation of 3 input bits. It principally consists three inputs. The input variables are expressed by A, B and  $C_{in}$ . The two produce variables are expressed by sum( S) and carry(  $C_{out}$ ).

## III. PROPOSED 8T FULL ADDER

In the proposed design a novel full adder in CMOS logic style with small number of transistors for low power application. In a 8T full adder design is being proposed using CMOS technology which is being implemented using DSCH tool. Here technology 1.2V is used for the performance. In the proposed 8T full adder sum is generated using two 3T XOR module and carry is generated using NMOS and PMOS pass transistor sence bias. Large number of transistor are used the noise and area increases, similarly low number of transistors are used the noise and area reduces.Receiving energy is not considered. A novel design of 8T full adder designed on the logic of 3T XOR and one 2T MUX.So in total 8 transistor..The equation for 8T full adder design are

$$\text{SUM} = A \text{ xor } B \text{ xor } C = (A \text{ xor } B) \text{ xor } C$$

$$\text{CARRY} = AB + BC + CA = AB + BC(A + A') + AC(B + B') = AB + (A \text{ xor } B)C = (A'B)B' + (A \text{ xor } B)C$$

Instead of using two NMOS pass transistor devices we have used one NMOS and one PMOS pass transistor device, because of ease of the design and as according to the equation as shown above

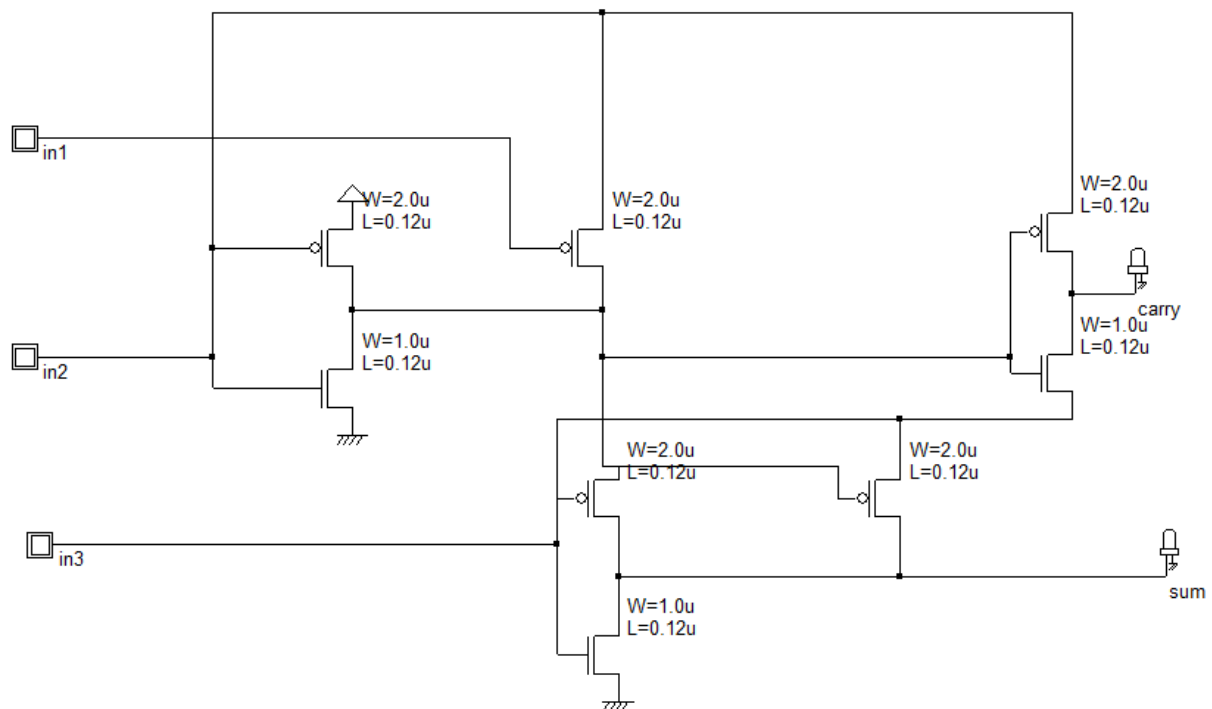


Fig 1 Proposed 8T full adder design

Then we've three inputs in1, in2 and in3 of the full adder and we give the LEDs to indicate the sum and carry of the full adder. When we've only one input is high also the sum led will glow. whenever further than one input is high, also the carry led will glow. When three input 1, input 2 and input 3 are high both the sum led and carry led will glow.

Table 1 Comparison between Full Adder and Proposed 8T Full Adder

Design	Number Of Transistor	Power(mW)	Delay(ns)	PDP
Full Adder	28	5.55	19.67	109.16
8T Full Adder	8	0.67	8	5.36

#### IV. SIMULATION RESULTS

The proposed full adder with minimum of 8 transistor with high speed and low power consumption, which employs a two 3T XOR and 2T MUX. The proposed full adder schematics are drawn using 0.12 $\mu$ m CMOS technology with 1.2 V supply voltage. Simulation results shows the great improvement in terms of power delay product. The critical path delay of the 8T FA measured at 8 ps. The power of the 8T full adder is 0.67 mW. The simulation circuit of 8T full adder using CMOS technology which is designed in DSCH software shown in Fig 2.

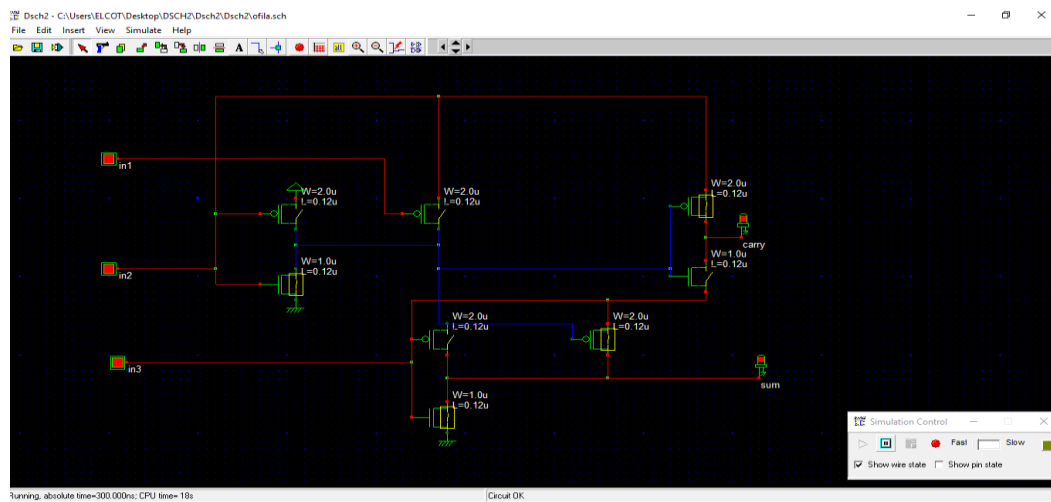


Fig 2 Simulated Circuit of 8T Full Adder

Fig 3 shows Microwind layout of 8T full adder using 0.12 $\mu$ m CMOS technology with 3 input and 2 output.

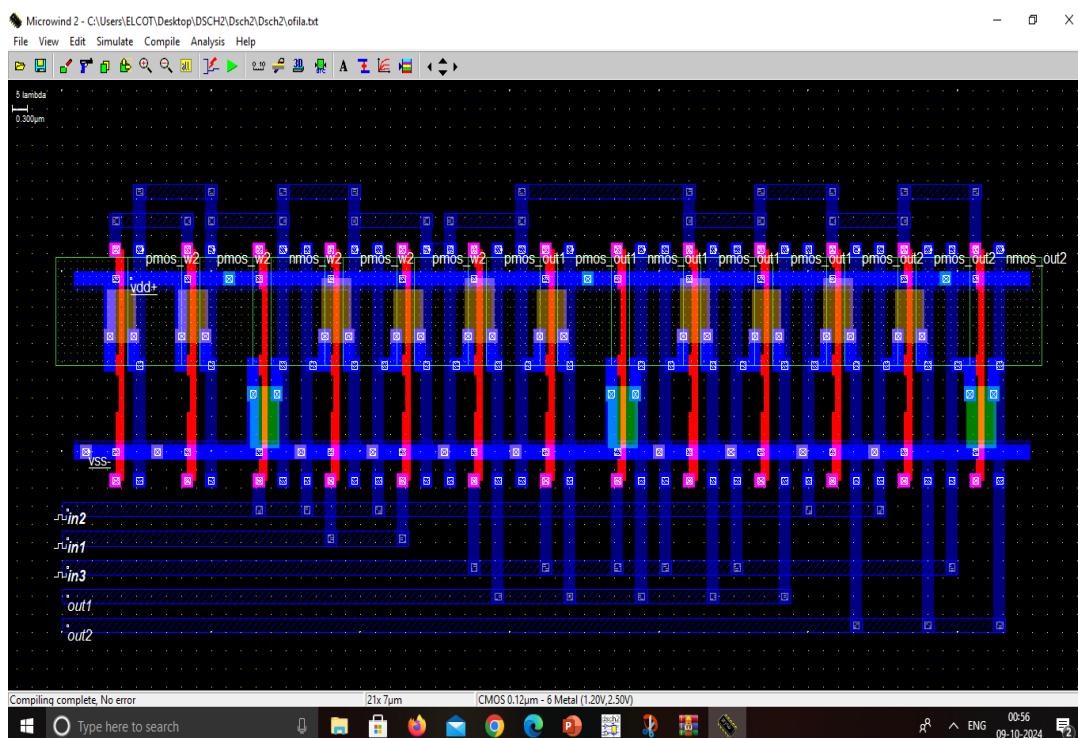


Fig 3 Layout Design of the 8T Full Adder



The power consumption of a proposed full adder is  $0.67 \mu\text{W}$ . Fig 4 shows simulated output waveform of voltage vs time with  $0.67 \mu\text{W}$  power. The Fig 5 shows delay which is obtained from Microwind. delay of the 8T full adder is 8 ns. The power delay product(PDP) of 8T full adder is 5.36 aJ.

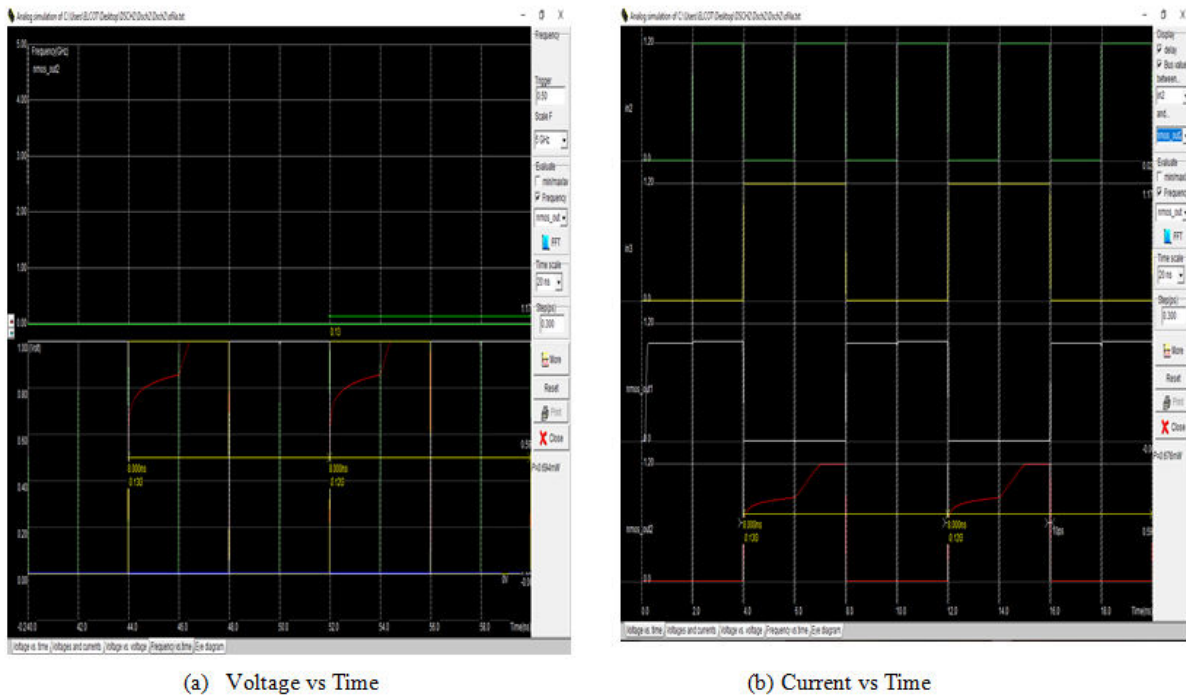


Fig 4 Simulated Output Waveform

Fig 5 shows a Timing diagram of 8T full adder using Verilog code.

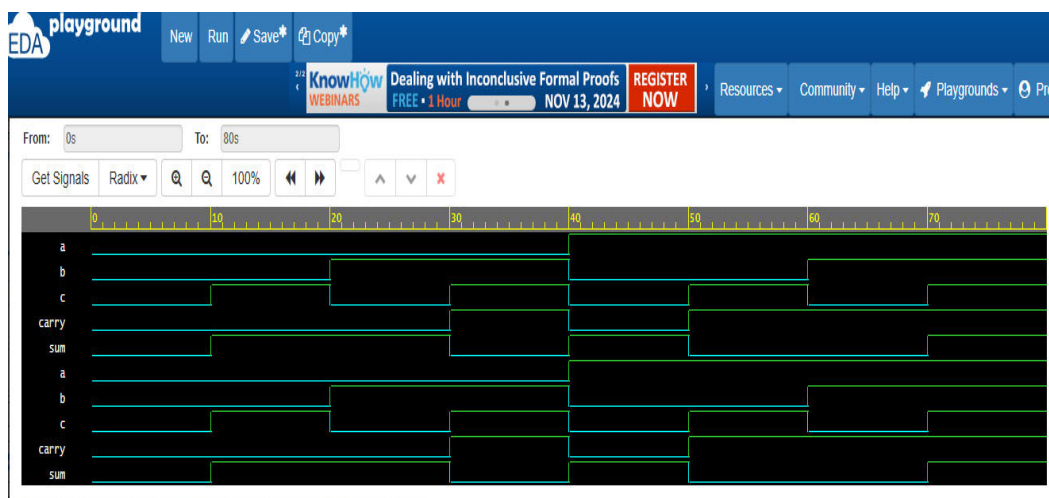


Fig 5 Timing Graph of 8T Full Adder in EDA Playground Tool

**V. CONCLUSION**

A Novel design of 8T full adder, which is implement on the logic of two 3T XOR and one 2T MUX. The Proposed 8T Full Adder is simulated using the DSCHE tool and 3D layout of 8T Full Adder is designed using Microwind tool. A CMOS Full Adder gives better calculation of power delay product by using 0.12 $\mu$ m CMOS technology. The Small number of transistors has higher performance. The power consumption and delay of the proposed 8T full adder is 0.67 mW and 8 ns. which is lower than the conventional full adder. 8T full adder gives better calculation of PSD by using 0.12 $\mu$ m CMOS technology. It is suitable for low energy application and portable devices.

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