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Image Processing Computing and Techniques: Single Exact Single Adders, Single Exact Dual Approximate Adder, Approximate Mirror Adder, and Multiplexer Approximate Adder

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ABSTRACT: Adders are essential components in circuit design, serving as primary modules. They are particularly important for error tolerant applications including digital image processing, machine learning and signal processing. Hence, it is crucial to prioritize the advancement of adders that exhibit minimal power consumption and optimal energy efficiency. Approximate adders demonstrate superior performance compared to exact adders in VLSI devices. The combination of Single Exact and Single Approximation (SESA), Single Exact and Dual Approximation (SEDA), Approximate Mirror Adders (AMA) and Multiplexer Approximate Adder (MAA) approaches has become a promising solution among approximation adders. The above hybrid adders provide energy efficiency and enhanced power compared to alternative accurate and approximation adder designs. The hybrid approximation adders to improve performance and lay the foundation for future hybrid approximate adder circuits. The effectiveness of the proposed approach was confirmed by extensive simulations. Moreover, the actual implementations showcased the adaptability and promise of hybrid adders in realistic situations. The suggested approach guarantees cost-efficiency and enables smooth future updates and expansions. In summary, our research enhances the development of adder designs that are both efficient and low-power, specifically designed to meet the changing needs of current digital systems.

KEYWORDS: Single Exact and Single Approximation (SESA), Single Exact and Dual Approximation (SEDA), Approximate Mirror Adders (AMA) and Multiplexer Approximate Adder (MAA) Image computing

I.INTRODUCTION

The use of approximation computing is crucial in modern electrical systems. It is a computational approach that emphasizes finding accurate solutions to problems rather than exact ones. This technology has gained popularity in numerous industries due to the increasing demand for high-performance computer solutions in the energy sector. While approximation computing offers advantages in terms of resource conservation and efficiency improvement, it is essential to thoroughly evaluate the balance between accuracy and resource preservation. The use of approximation computing depends on the unique requirements of the application and the acceptable level of variance in the results. Approximate circuits, also known as inexact or unreliable circuits, are intentionally designed to produce results that are not exact, but instead include a defined margin of error. These circuits are employed in businesses that prioritize energy conservation and cost reductions over precise accuracy. They are particularly beneficial in image and signal processors for tasks such as picture scaling, filtering, audio and speech processing, as well as audio compression, where a slight decrease in quality is acceptable. These approximation circuits are widely used for hardware accelerators in the domains of machine learning and deep learning.

Graphic Processing Units (GPUs) have utility in diverse domains, including gaming and scientific simulations. Graphics rendering can utilize approximate circuits to enhance real-time performance while maintaining quality within a defined range. The use of approximate circuits is contingent upon the specific needs of the application and the tolerable margin of error. Approximation circuits become an attractive choice when there is a favorable combination of reduced energy consumption, increased speed, and acceptable error margins. Adders are crucial elements in digital electronics and computer systems, primarily used for performing arithmetic operations, including addition. Adders are frequently employed in various applications in the field of computing and electronics. There are two types of adders: precise adders and approximate adders. Accurate adders may consume a larger quantity of power and energy compared to approximate adders, making them less suitable for energy-efficient circuits. Accurate adders are essential for

situations when precision is of utmost importance, while approximation adders offer advantages in terms of speed, resource efficiency, and energy conservation [1]. Approximation adders are a specialized type of digital adder circuit designed to perform addition operations with a certain degree of approximation. The primary objective of approximation adders is to minimize power consumption, reduce hardware complexity, and improve speed. Approximation adders are particularly useful in scenarios where a slight reduction in accuracy is acceptable or imperceptible, such as multimedia processing, real-time signal processing, or low-power devices like IoT sensors. However, it is essential to carefully assess their use based on the specific requirements of the application [2].

II. SESA: SINGLE EXACT SINGLE APPROXIMATE ADDERS

Additionally, the design characteristics of SESA adders are especially addressed in this section. Adders that are part of the SESA family are able to do either a single accurate addition or a single approximation addition. It can be deduced from the fact that SESA adders have a finite maximum error that there is no approximation implemented in the CARRY bits. This article provides an introduction to three different SESA designs, each of which will be discussed in greater detail in the following sections.

A. SESA1 Adder

When we use the SESA1 adder, we make the SUM output equal to the complement of CARRY. This allows us to insert approximation into the SUM result. When the input combinations 000 and 111 are used, the SESA1 adder produces mistakes in the SUM bits.

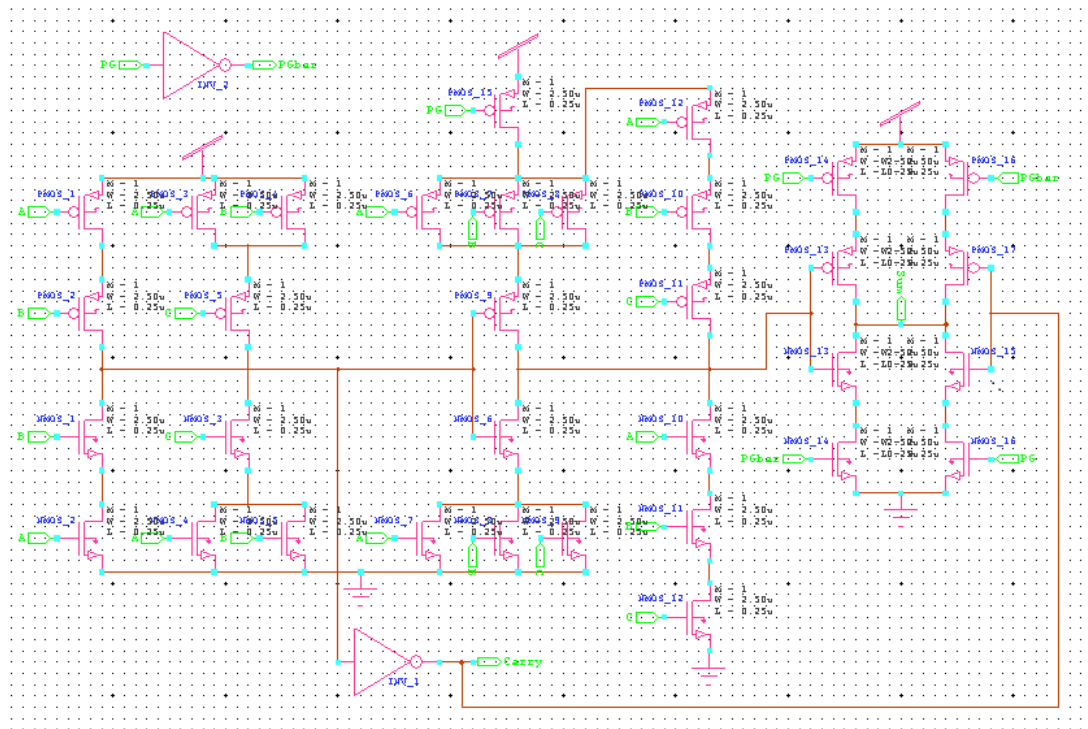


Figure 1: Circuit diagram of SESA1

B. SESA2 Adder

To implement approximation in the SUM output of the SESA2 adder, we make it equal to zero for all of the possible input combinations in order to use the approximate mode. As a consequence of this, the SESA2 adder exhibits faults in the SUM bits for the input combinations including 001, 010, 100, and 111

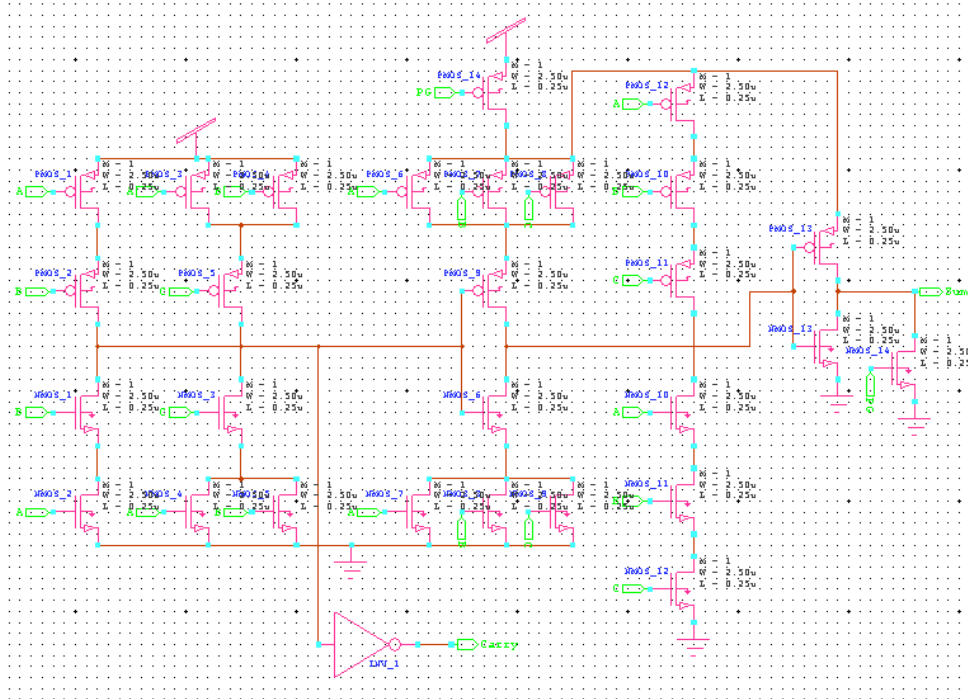


Figure 2: Circuit diagram of SESA2

C. SESA3 Adder

We implement approximation in the SUM output of the SESA3 adder by setting it to 1 for each and every combination of inputs. As a consequence of this, the SESA3 adder exhibits faults in the SUM bits for the input combinations 000, 011, 101, and 110.

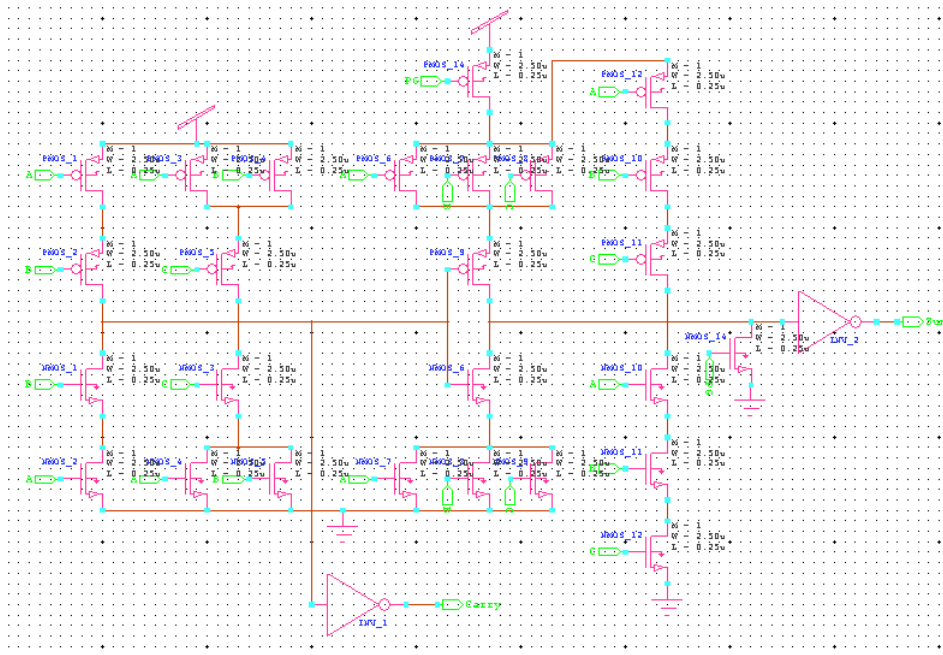


Figure 3: Circuit diagram of SESA3

III. SEDA: SINGLE EXACT DUAL APPROXIMATE ADDERS

The SEDA adders surpasses the SESA adder in terms of advancement. Additionally, it possesses a maximum limit on the potential inaccuracy and offers the possibility to be customized. In contrast to SESA adders, which are limited to performing only one approximate addition, SEDA adders have the capability to do two approximate additions when operating in approximation mode. In the framework of SESA, we implement power gating for the SUM module of the adder, particularly when it is used in approximation mode. This is done in order to ensure safety and efficiency. Additionally, the SUM module is utilized within the SEDA adder in order to generate an extra CARRY.

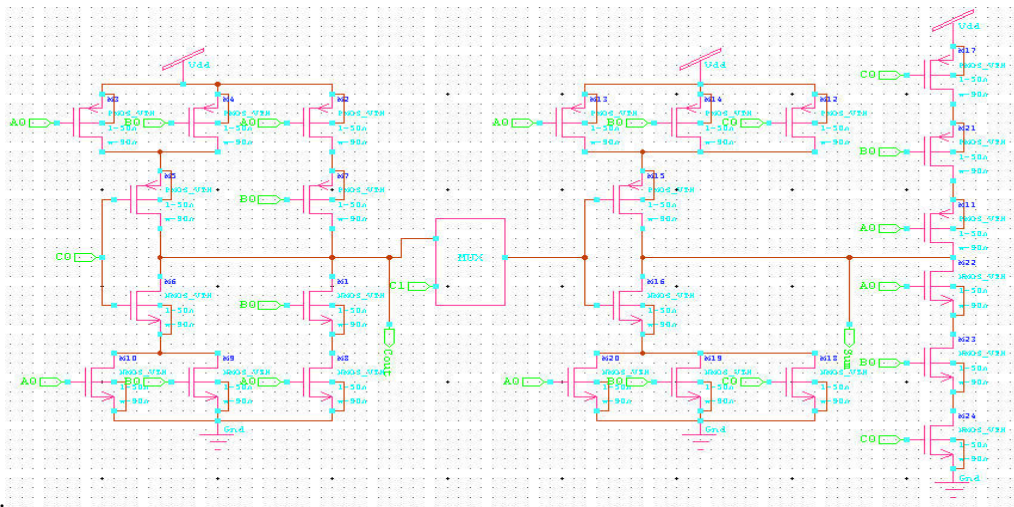


Figure 4. Circuit diagram of SEDA adder

IV. APPROXIMATE ADDERS

This section has explored various approaches for creating approximate adders. With reference to the circuit design, the Tanner software program was utilized in order to carry out the stimulation and analysis of a variety of approximation adders.

A. APPROXIMATE MIRROR ADDER 1

with a reduced number of transistors, in order to obtain an approximation mirror adder. The typical schematic architecture is gradually transformed by the removal of transistors one by one.

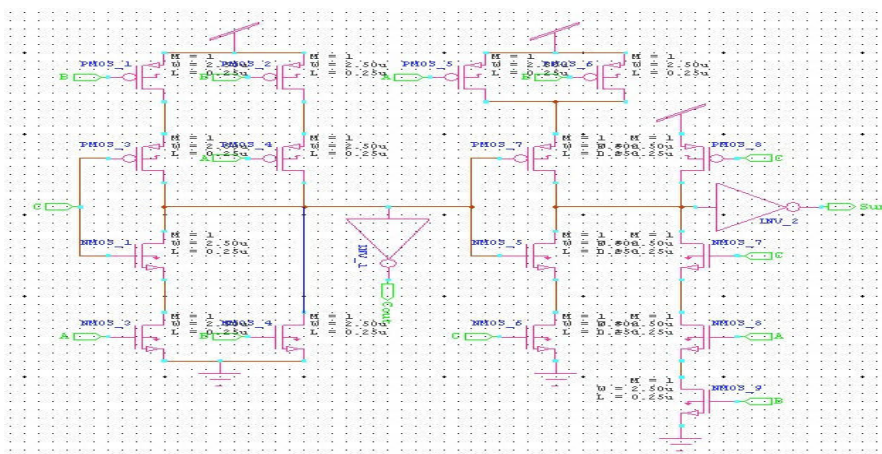


Figure 5. Approximate Mirror Adder 1

B. APPROXIMATE MIRROR ADDER 2

Except for the input combination A=1, B=1, Cin=1, and A=0, B=0, Cin=0, the truth table of Full Adder demonstrates that Sum is equal to the complement of cout1 in six out of eight situations. The exception to this rule is the combinations A=1, B=1, Cin=1. Within the context of combination mirror adders, the computation of the complement of Cout often takes place at the initial stage. The approach of sum equals to complement of Cout is a straightforward method for obtaining a straightforward schematic output.

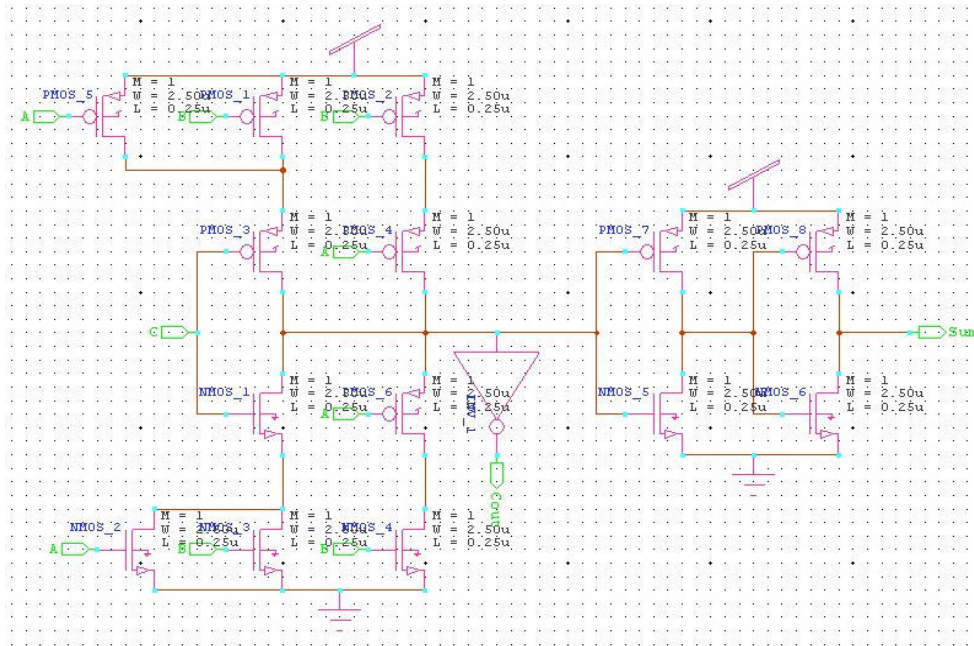


Figure 6. Approximate Mirror Adder 2

C. APPROXIMATE MIRROR ADDER 3

Further simplification can be achieved by combining approximation 1 and approximation 2, respectively. It has been observed that this revised schematic contains three errors in total, in addition to one fault in the Cout algorithm.

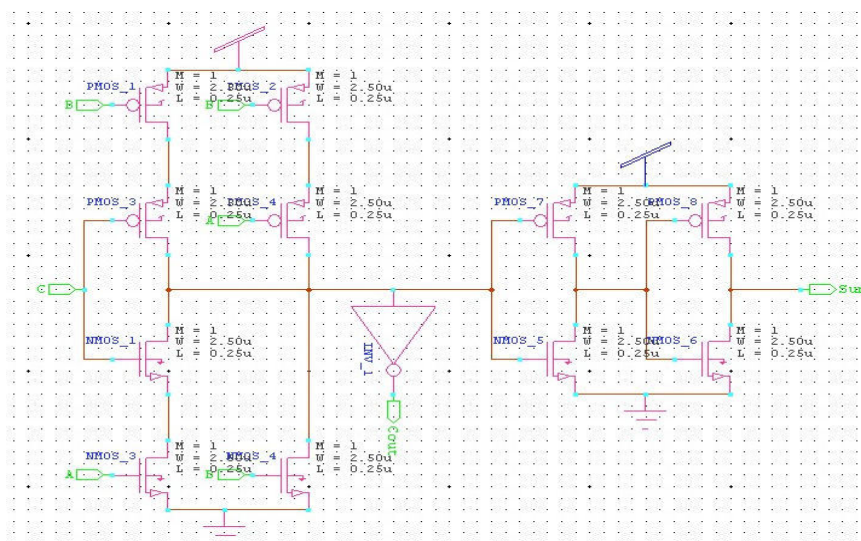


Figure 7. Approximate Mirror Adder 3

V. PROPOSED MULTIPLEXER APPROXIMATE ADDER

For the purpose of this endeavor, multiplexers will be used only in order to achieve an approximation. A transistor gate-based adder is used in the construction of the multiplexer. This adder is composed of three components: (1) an XOR gate, (2) a multiplexer, and (3) an OR gate. Through the utilization of the multiplexer, the XOR gate and the OR gate can be identified. A design that is based on invertors is utilized in its construction.

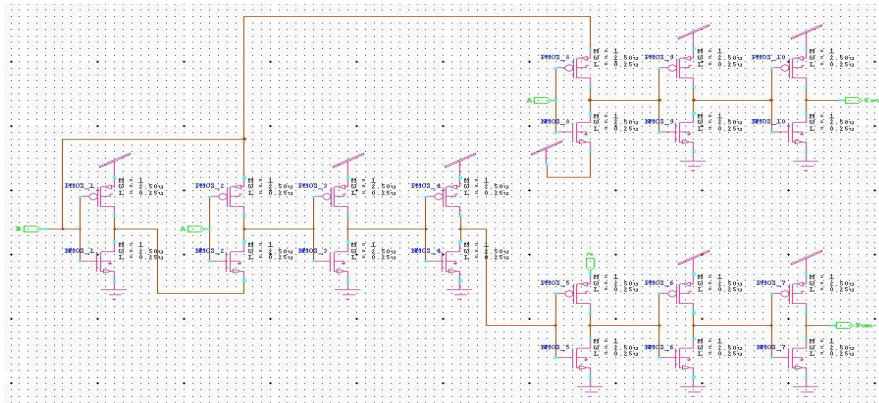


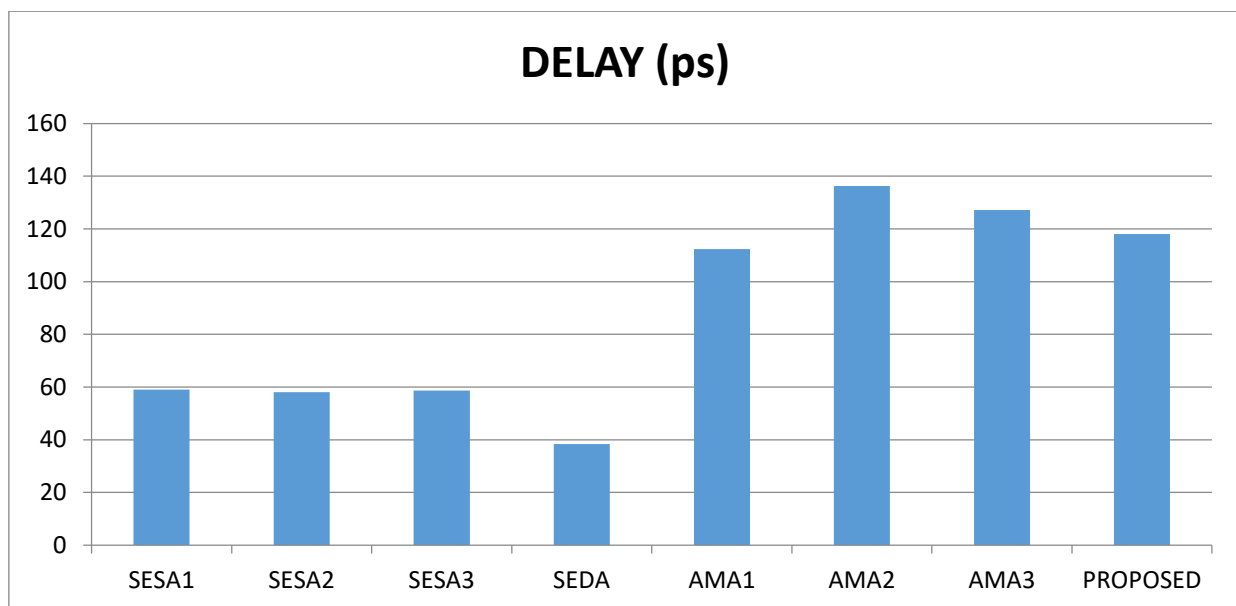
Figure 8. Proposed Multiplexer Approximate Adder

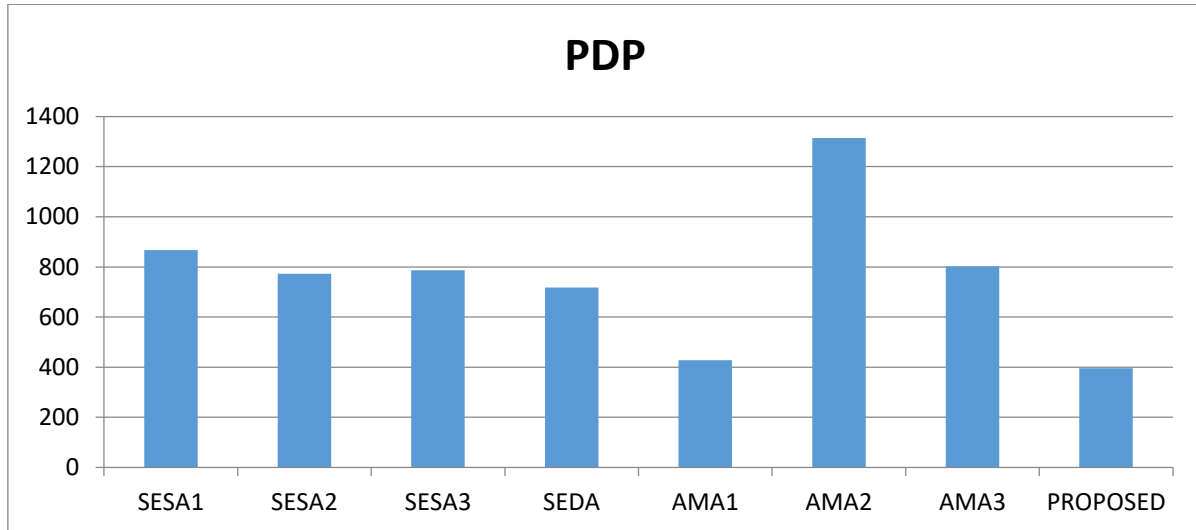
VI. RESULTS

A. Comparison of Different Approximate Adders

SESA1, SESA2, SESA3, SEDA and At a process technology of 90 nanometers, simulations were performed on three approximate mirror adders as well as the proposed multiplexer approximate adder. Specifically, the ratio of W_n to L_n was 2:1, while the ratio of W_p to L_p was 3:1. Through the use of the Tanner EDA tool, a power supply of 1V was supplied and simulated over a period of 500 nanoseconds. This was accomplished by applying the same input patterns to the complete adders. A comparison of the power and the propagation delay was made in Table 1, which was tabulated after being measured.

Design	Power (μ W)	Delay (ps)	PDP ($Ws*10^{-18}$)	No. of Transistors
SESA 1	14.7	59.0	867.3	33
SESA 2	13.3	58.1	772.73	28
SESA 3	13.4	58.7	786.58	26
SEDA	18.7	38.4	718.08	28
AMA1	4.22	112.4	427.64	18
AMA2	9.84	136.3	1341.19	16
AMA3	6.30	127.2	801.36	13
Proposed	3.35	118.1	395.64	20





B. Evaluation for Image Processing Applications

Image smoothing is a technique employed to reduce the undesired noise in an image by calculating the average of the pixel values in the neighboring area of each pixel. Image sharpening is a method used to enhance the clarity and details of an image, resulting in a more distinct and clear look. This is achieved by amplifying the high frequency components of the image. The input image is initially resized to a dimension of 256x256 and then transformed into a grayscale image. This is done in order to facilitate the development of real-time image processing applications. In this section, the proposed single approximation technique, known as picture smoothening and image sharpening, is implemented in MATLAB and its performance metrics are evaluated.



Original Image

SESA1 Based Image

SESA2 Based Image



SESA3 Based Image



SEDA Based Image



AMA1 Based Image



AMA2 Based Image



AMA3 Based Image



Proposed MAA Based Image

VII. CONCLUSION

This study effectively showcased the capabilities of SESA and SEDA along with Three AMA adders. Additionally, a novel MAA adder was developed to enhance the quality of medical images by employing smoothing and sharpening approaches. The assessment of these adders demonstrates their capacity for extensive utilization in diverse technological fields, such as microprocessor engineering. An in-depth research reveals that the SESA, SEDA, and AMA adders have a lower power consumption compared to their contemporaries, but slightly higher. On the other hand, the recently introduced proposed MAA based adder exhibits exceptional efficiency, characterized by significantly lower power consumption and reduced delay, surpassing existing approximation adders in the same domain. The study conclusively demonstrates that the Proposed MAA surpasses other methods in terms of application performance metrics. In the field of medical imaging, the implementation of the Proposed MAA is expected to greatly improve the sharpness of images, leading to more accurate diagnoses of chronic conditions. The objective of this research is to design a MAC circuit in order to explore its practical applications in greater detail.

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