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System Design & SI Simulations for Driver Monitoring System

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ABSTRACT: To study all the SI-related hardware challenges through design and simulations and learn a typical embedded system design workflow, a driver monitoring system is attempted to design and illustrated as an example. The driver monitoring system is chosen given its complex electrical architecture, the need for high-speed interconnects (Camera, Storage, etc.) on PCB, and a wide range of use cases in the field (Driver safety, evidence for insurance, etc.).

KEYWORDS: Schematic Design, SI (Signal Integrity), High-Speed, PCB Design, Camera, Storage

I. INTRODUCTION

Over the last few years, the design of printed circuit boards (PCBs) has become more complicated as the margin of error in electrical designs has shrunk dramatically, and the chances of system failure are extremely high if due attention is not given during design. Simulation-driven design is the best approach that is being adopted across the industry to combat it. Signal integrity is one of modern electronic systems' most important design requirements. Through rigorous SI simulation, SI issues such as “delays,” “ringing,” “crosstalk,” and “EMI” can be identified. Once possible issues have been figured out, layout constraints could be implemented to increase performance. A high-performance product with improved reliability and lower cost can be generated by addressing SI problems early in the engineering builds. The primary objective of this paper is to illustrate guidelines for designing a PCB and build confidence through SI simulations.

The paper is organized as follows: Section II describes the block-level architecture and how the system helps serve the purpose. Section III describes schematic and Design guidelines. Section IV presents simulation results showing the signal integrity performance. Finally, Section V presents the conclusion.

II. LITERATURE SURVEY

Using a camera, the system tracks the driver's actions and stores the data on a micro card. Additionally, the vehicle's movements are monitored using a 9-axis sensor, contributing to a comprehensive driver activity tracking solution. This PCB is designed for use in a car-mounted solution, making it suitable for a wide range of commercial vehicles. The finished product can be easily installed on a car's windshield, providing a reliable means to record the driver's actions during operation.

Some insurance companies may require evidence to determine the driver's liability in the event of an accident. This PCB can provide crucial video evidence, helping to establish the sequence of events and potentially reducing the driver's liability costs. As a result, the device helps to cut down on an individual's liability costs by giving them recorded videos as proof. This lets the car owner monitor the driver's behavior, driving skills, etc. Here is the top-level diagram of the system we intend to build.

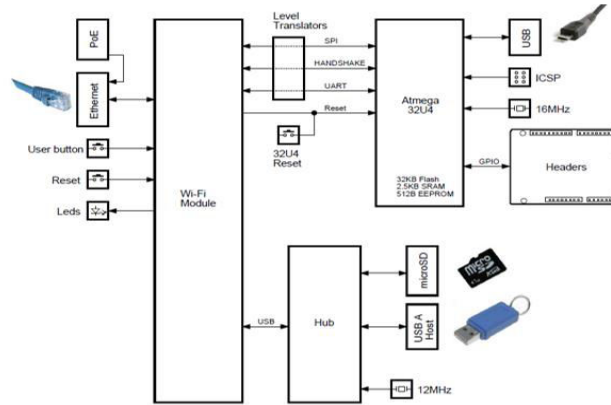


Fig. 1. Architecture Diagram

III. METHODOLOGY

The first step is determining the system's power consumption and number of components, followed by schematic design, layout design, simulations, and design improvements through simulation feedback. OrCAD Capture and Cadence Allegro are used to make schematics and layouts, respectively. Ansys HFSS is used for SI simulations.

Schematic Considerations:

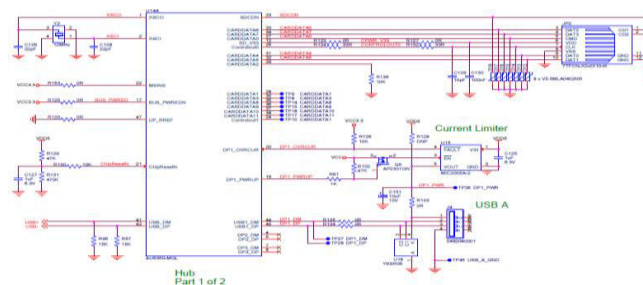
1. Choose discrete components based on the needs of the power supply and be careful using bulk capacitors at the IC's input and output; critical to consider a low ESR capacitor to reduce the ripple
2. Keep an LC filter to adjust the power supply for noise or ripples
3. Check termination and AC capacitance requirements for High-Speed
4. If EMI is a concern, CMC could be an option to reject common mode noise
5. If the Eye-margin is limited, consider using Re-driver/Re-timer

Layout Considerations:

1. The power components should be placed so as to make the high current flow paths as short as to reduce the AC impedance and conduction losses
2. Putting the decoupling capacitors near the processor pins and connecting them directly to the pins is the best way to reduce connection impedance without using vias
3. Maintaining characteristic impedance all along the path is key for reducing return loss
4. Consider lower length of traces, less number of vias, and stripline routing to better insertion loss
5. To eliminate timing errors, inter-pair, and intra-pair skew matching is a must depending on RX requirements

IV. RESULTS

Schematic Design



(a)

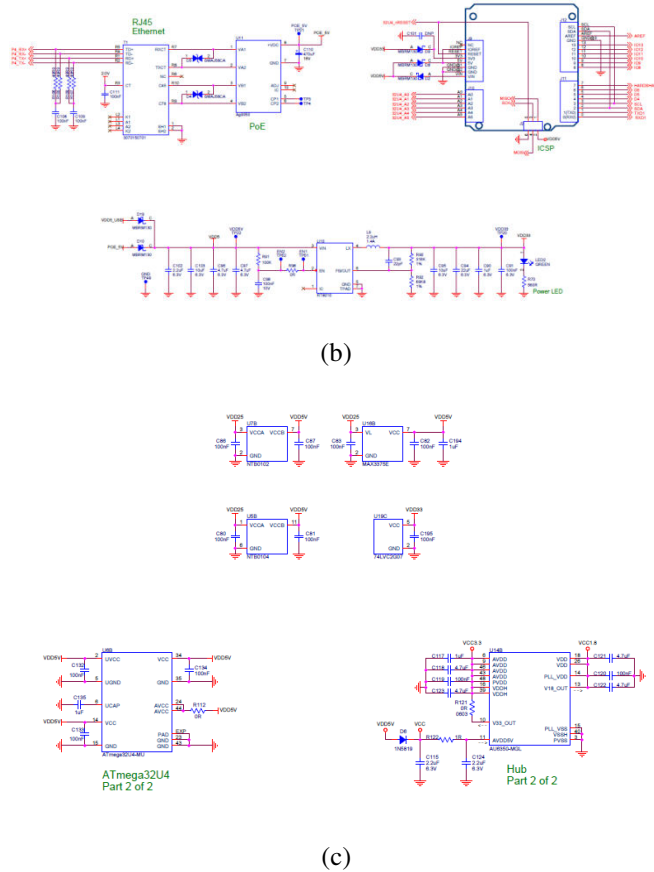
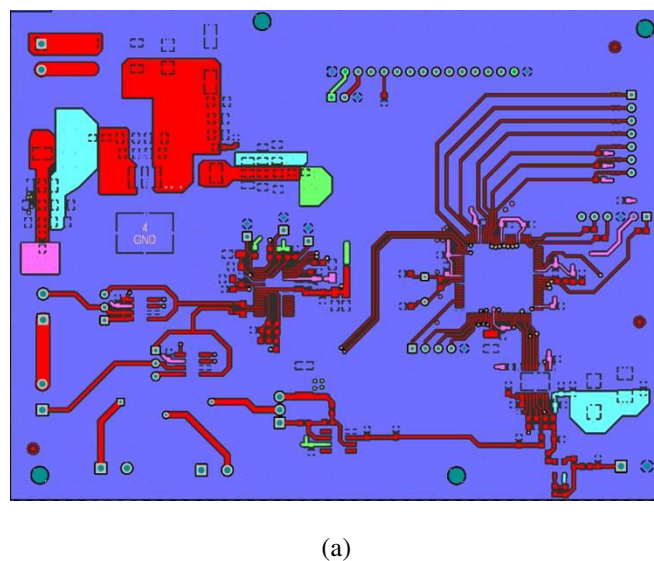
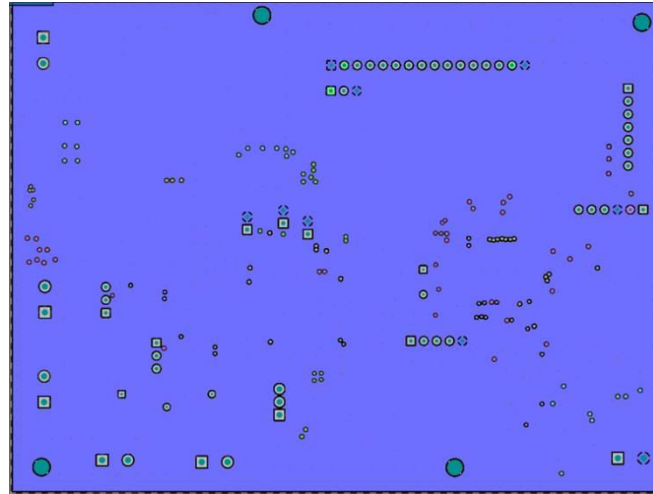


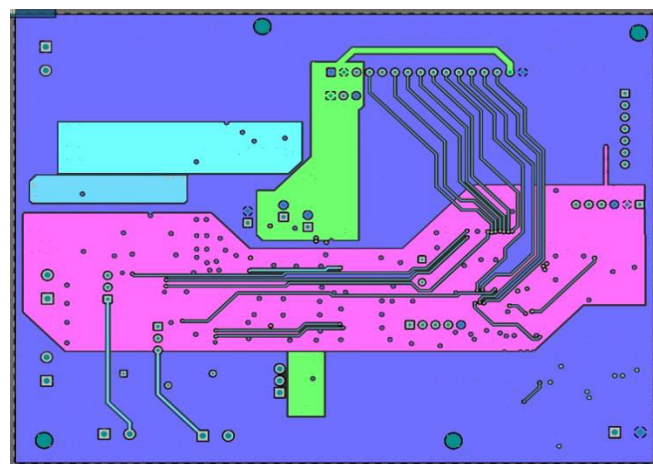
Fig. 2. Schematic Design Sections (a) High-Speed (b) Power Supply (c) Controller

Layout Design

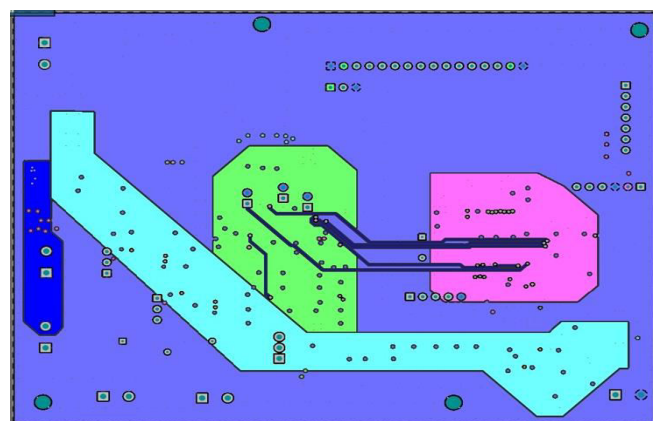




(b)



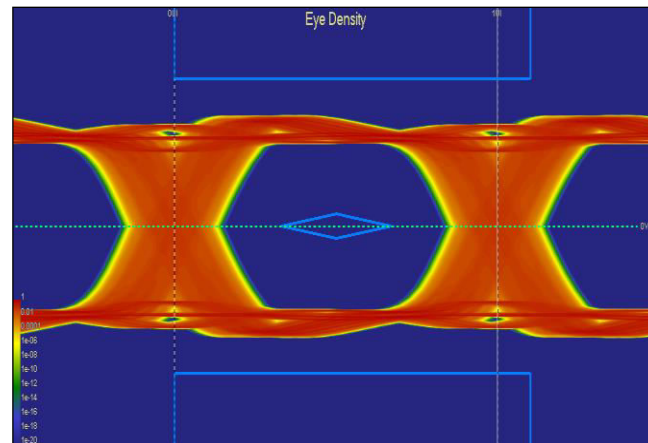
(c)



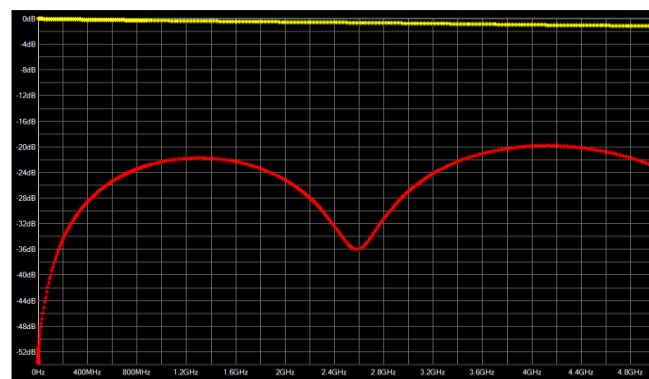
(d)

Fig. 3. PCB Routing Layers (a) Top (b) ISL-2 (c) ISL-3 (d) Bottom

Signal Integrity Simulation



(a)



(b)

Fig. 4 SI Simulations (a) Eye Diagram (b) S21 (Insertion Loss), S11 (Return Loss)

V. CONCLUSION

In summary, the evolution of printed circuit board (PCB) design towards greater complexity underscores the challenges posed by increasing circuit integration in smaller consumer devices. The shrinking margin of error in electrical designs necessitates meticulous attention during the design phase to prevent system functional failures. Simulation-driven design decisions emerge as crucial tools in mitigating these risks. Signal integrity (SI) and power integrity are pivotal requirements in modern electronics, particularly for high-speed PCBs and integrated circuits, where issues like delays, ringing, crosstalk, and electromagnetic interference (EMI) can significantly impact performance. Implementing layout constraints and termination procedures effectively addresses SI concerns, enhancing reliability and cost-effectiveness. Though this paper only covers Signal Integrity (SI) simulations, this work could be extended to Power Integrity (PI) simulations - like DCIR, AC Transient, PSRR, etc.

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