



International Journal of Innovative Research in Science Engineering and Technology (IJIRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.699

Volume 14, Issue 4, April 2025

High-Efficiency Synchronous Binary Counter with Minimal Clock Period using Optimized Parallel Architecture

Mrs. K Amala, K Jhansi Meghana, M Reddy Rekha, M S Mohith, V Chaithanya, Y Anitha

Assistant Professor, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

U.G. Student, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

U.G. Student, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

U.G. Student, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

U.G. Student, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

U.G. Student, Department of ECE, SV College of Engineering, Tirupati, Andhra Pradesh, India

ABSTRACT: An ideal parallel design for a clock-period-minimal constant-time synchronous binary counter is presented in this paper. The architecture makes use of two types of 8-bit synchronous binary counters: one that uses a ripple carry chain and the other that uses backward carry propagation. In addition, it presents an altered 64-bit prescaled counter that generates prescaled enable signals by means of ring counters. Our proposed design shows considerable benefits over current approaches. Compared to the conventional technique, which has 131 area registers, 68 LUTs, and 66 IOBs, the suggested method uses 99 area registers, 65 LUTs, and 66 IOBs, reducing the area footprint in terms of hardware resources. Furthermore, the suggested architecture reduces latency; the current method's latency is 1.172 ns, but the new architecture's latency is 0.978 ns. Additionally, the suggested approach shows improved power efficiency, using only 0.00107 W as opposed to 0.0162 W for the current method. These findings demonstrate how well the suggested architecture performs in terms of improving performance metrics, which makes it a viable option for applications that call for synchronous binary counters that operate constantly with short clock periods.

KEYWORDS: Synchronous binary counter, Parallel architecture, Minimal clock period, Backward carry propagation, Ripple carry chain, Pre-scaled counter, Ring counters, Area optimization, Delay reduction etc.,

I. INTRODUCTION

Synchronous binary counters are essential parts of digital circuit design that are used in a variety of applications, from frequency dividers to event counts. In synchronous systems, these counters are essential for tracking events and producing exact time signals. However, maintaining constant-time operation while achieving high performance—especially in terms of minimal clock period—presents a substantial problem. This study presents an efficient parallel architecture designed to realize a clock-period-minimal constant-time synchronous binary counter. The suggested architecture overcomes the shortcomings of previous implementations by utilizing cutting-edge design strategies to improve performance measures including area efficiency, latency reduction, and power consumption. Our methodology is based on the use of standard 8-bit synchronous binary counters that have been enhanced with sophisticated functionality such as backward carry propagation. We hope to reduce the key path delays that ripple carry chains entail and speed up counting procedures by utilizing backward carry propagation. To further improve the counter's performance, we also offer an altered 64-bit prescaled counter that makes use of ring counters to generate prescaled enable signals. By means of extensive testing and contrastive study, we prove that our suggested architecture is better than current approaches. We evaluate several important performance metrics, such as power efficiency, delay characteristics, and area usage. We accomplish significant gains in all these areas by carefully refining the architectural design, opening the door for synchronous binary counters that are more dependable and efficient. All things considered, this research clarifies the role optimized parallel architectures play in raising the bar for digital circuit design capabilities.

An example of how creative design approaches can effectively address the constantly changing needs of contemporary electronic systems is the suggested constant-time synchronous binary counter with short clock period..

This study's organizational framework separates the research into several areas. Section 2 presents the Literature Survey. The topics of current and proposed system techniques were covered in sections three and four. Additionally, the simulation results are discussed in section 5. Section 6 concludes with a presentation of future work and conclusions

II. LITERATURE SURVEY

Driven by the need for high-performance digital circuits in a variety of applications, the design and optimization of synchronous binary counters have been thoroughly examined in the literature. The improvement of important features including speed, area efficiency, and power consumption has been the subject of numerous research projects.[1]

Ripple carry chains are frequently used by conventional synchronous binary counters to increment and propagate carry signals. Because carry signals propagate serially, ripple carry counters suffer from intrinsic delay restrictions despite their simple implementation. Scholars have investigated substitute architectures that integrate parallelism and carry lookahead techniques in order to overcome this constraint.[2]

Carry look ahead adders (CLA), which allow for parallel carry creation across several counter stages, are one popular method. CLA-based counters improve overall performance by reducing propagation delays greatly by computing carry signals ahead of time. Nevertheless, these designs frequently result in higher complexity and area usage.[3]

Recent developments in synchronous counter design have prompted the investigation of cutting-edge methods like backward carry propagation. Backward carry propagation uses the symmetry in binary addition to propagate carries from more significant to less important bits, in contrast to conventional ripple carry counters that transmit carries in the forward manner. By shortening critical routes, this method efficiently produces counting operations with shorter clock periods. [4]

In the literature, prescaled counters are another topic of interest, especially for applications that need frequency division or event counting with granularity that can be adjusted. Various techniques have been proposed to generate prescaled enable signals, such as using modulo-N counters and ring counters, which allow for fine-grained control over counting intervals while minimizing hardware overhead.[6]

Even though the body of current literature offers insightful information on the design and optimization of synchronous binary counters, further investigation is still required to discover sophisticated architectures that can achieve constant-time operation while utilizing short clock intervals. The goal of this study is to add to this body of knowledge by introducing an optimized parallel architecture designed with this purpose in mind. We show that our proposed design is effective in fulfilling the demanding specifications of contemporary digital systems by means of an extensive assessment and comparative analysis.[7].

III. EXISTING METHOD

The classic synchronous binary counter, represented in Fig. 1, is made up of several T F/Fs with an XOR gate inside. Remember that an XOR is the simplest logic needed to slightly alter the counter value. For the purpose of simplicity in this analysis, the combination of a D F/F and an XOR gate is represented as a T F/F. The series of AND gates starts with the lower bit (LSB) and works its way down to every lower bit. When every lower bit is a 1, a carry is generated. The sequence of sequentially connected AND gates forms a long path known as a ripple carry chain. Through use of the ripple carry chain, the carry is propagated forward from the least significant bit to the most significant bit (MSB). The carry-out of an AND gate is only valid until each lower carry-out signal has stabilized, and the propagation route lengthens with increasing counter size. As a result, the conventional binary counter has a large latency that linearly grows with counter size.

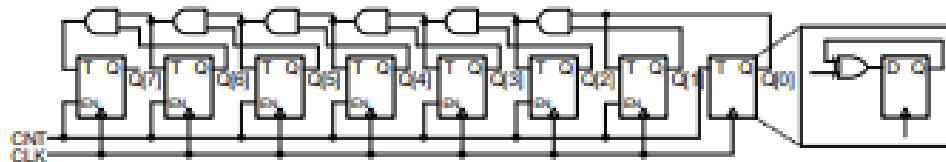


Fig. 1. Implementation Flow Diagram

The creation of a fast synchronous counter depends on the utilization of the backward carry propagation outlined in [10]. The counter functions because of the characteristics of the binary number system, which cause a more significant bit to become high earlier than the least significant bit. Unlike the standard binary counter, which uses a single chain, each counter bit in Fig. 2 has its own AND chain connected in the opposite direction. The early arriving signals are evaluated prior to the recently available signals entering a carry chain. Thus, when the fast changing signal from the LSB is connected to the final AND gate in the carry chain, it defines the critical route delay of the backward carry propagation. Therefore, the propagation delay is mostly controlled by a T F/F and the delay of the final AND gate. But as Fig. 2 shows, the LSB, Q[0], has a large fan-out and is connected to all AND chains. Stated differently, the fan-out establishes the crucial path delay since the LSB's load prevents it from driving rapidly.

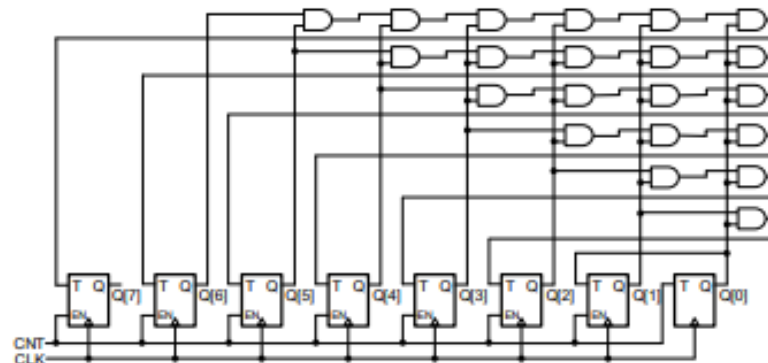


Fig. 2. Implementation Flow Diagram

Fig. 3 depicts the constant-delay binary counter based on prescaling, which is presented in [11]. Subblocks of different sizes are created from a broad counter; the high-order subblock operates at a lower frequency than the low-order subblock. The fundamental idea is to calculate the amount to add to a high-order block using the PEN signal generated by the low-order block known as a prescaler. The frequency at which a PEN functions is significantly lower than the clock signal. The high-order block receives much fewer increments than the low-order block, which makes this possible. The PEN signal is produced by a ring counter, which nearly doubles the overall complexity. The clock period is determined by whichever block has the least theoretical delay. However, in practice, the counting rate is greatly decreased by the fan-out necessary to distribute the count enable signal (CNT) and the PEN. The signals must drive a sizable number of F/Fs for the ring counter and the subsequent subblock. For instance, in Fig. 3, the shift operation of three ring counters totaling 74 D F/Fs is made possible by the CNT. The PEN output of the 64-bit ring counter drives 58 D F/Fs in the ensuing 58-bit subblock. As the counter size grows, the fan-out problem gets worse and the propagation delay of the PEN signal ultimately gets close to and exceeds the desired minimum propagation delay. A massive fan-out really causes a delay that is significantly longer than the theoretical delay.

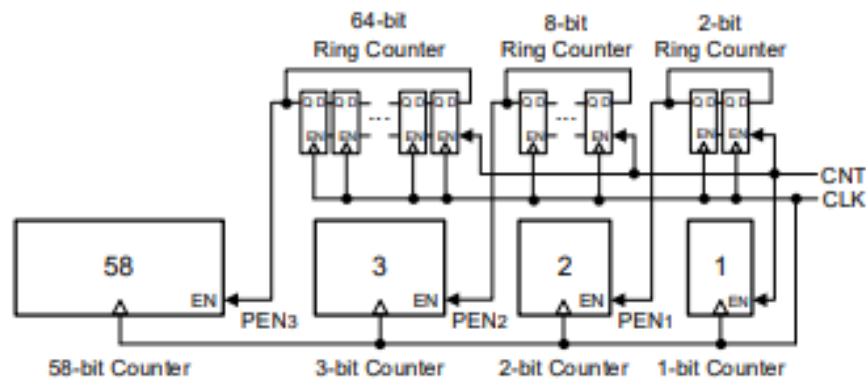


Fig. 3. Implementation Flow Diagram

IV. PROPOSED METHOD

Digital circuit design researchers have been working hard to find optimal parallel architectures that can produce constant-time synchronous binary counters with short clock intervals. Here, the application of prescaling-based modified constant-delay ring counters is a potentially useful way to improve counter performance. In an effort to push the limits of synchronous binary counting operations' speed and efficiency, this paper presents and investigates such an architecture.

Prescaling techniques are well known for their versatility in a wide range of applications due to their capacity to modify counter granularity and counting intervals. But conventional prescaling techniques frequently have built-in drawbacks, like complicated circuitry and varying delay characteristics. The suggested architecture uses a modified constant-delay ring counter technique, which minimizes hardware overhead and provides uniform delay characteristics across all counting states, to overcome these issues.

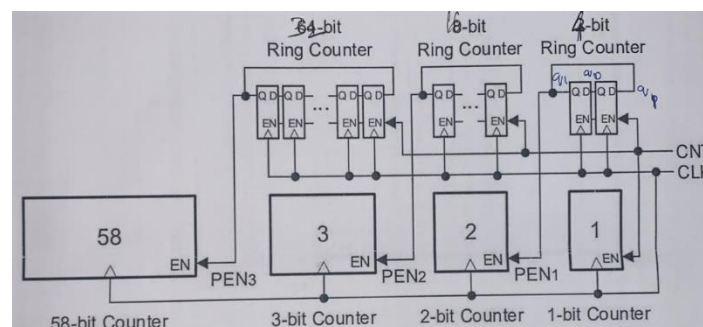


Fig. 4. System Architecture

The main breakthrough is that ring counters with modified delay elements are used, which guarantees consistent propagation delays independent of counting status. The suggested architecture accomplishes accurate timing management and permits synchronous counting operations with short clock intervals by preserving constant delay characteristics. Moreover, the architecture's parallel nature improves throughput and scalability, which qualifies it for high-speed digital systems.

In this paper, we present a detailed analysis of the modified constant-delay ring counter-based architecture, focusing on its design principles, implementation details, and performance evaluation. Through extensive simulations and comparisons with existing methodologies, we demonstrate the efficacy of the proposed approach in terms of speed, area efficiency, and power consumption. Additionally, we highlight potential applications and implications of the architecture in the context of modern digital circuit design.

As a whole, this work advances the development of synchronous binary counter optimized parallel architectures by providing a novel fix based on altered constant-delay ring counters with prescaling..

A. Implementation

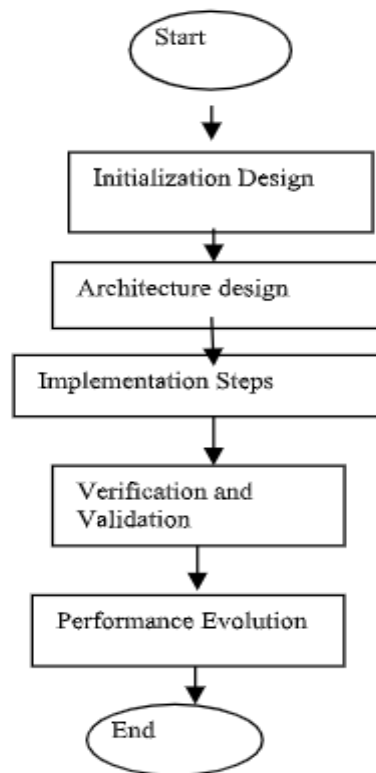


Fig .5. Implmentatn Flow Diagram

Xilinx ISE Design Suite 14.5 still allows you to evaluate FPGA design performance metrics like area, power, and delay. You can calculate and analyze each performance metric using Xilinx ISE in the manner listed below.

Delay:

The customary unit of measurement for delay in Xilinx ISE is the critical path delay, which is the longest path throughout the design. After synthesis and implementation, time data can be generated to determine the critical path delay. Xilinx ISE's Timing Summary report includes details on the critical path latency.

Area:

The number of slices, LUTs, FFs, and other resources that the design uses is how Xilinx ISE measures area usage. You can create utilization reports following synthesis and implementation to get specifics on resource usage. To learn more about the slices, LUTs, and FFs that the design used, look for reports like the Design Summary..

Power:

Unlike Vivado, Xilinx ISE lacks integrated power estimation tools. However, operational frequency and resource utilization can be used to indirectly estimate power consumption. Static power (leakage) and dynamic power (associated to switching activity) are the main factors affecting power consumption in FPGAs.

V. RESULT AND DISCUSSION

A.EXISTING METHOD

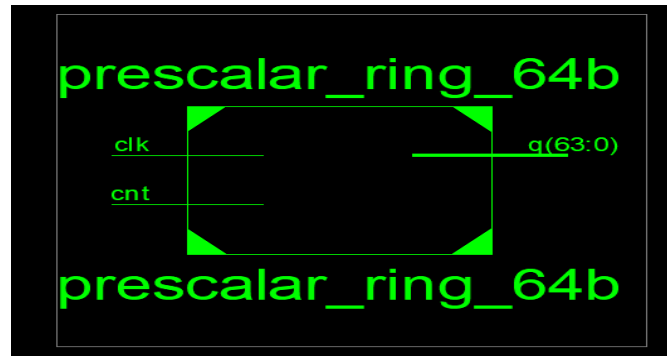


Fig .6. RTL Schematic

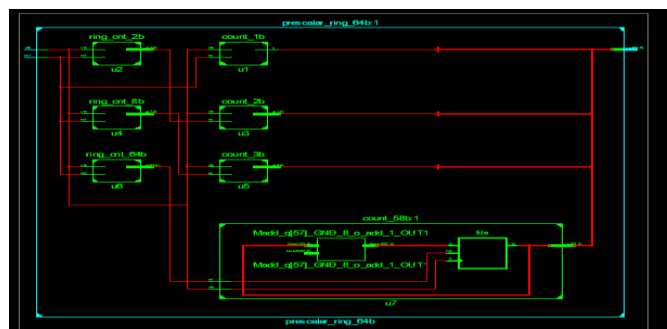


Fig. 7. Technology Schematic

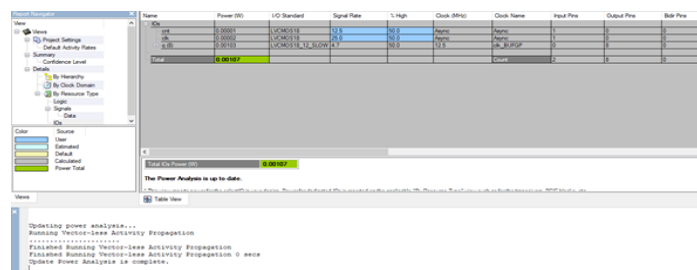


Fig. 8. Showing Power consumption

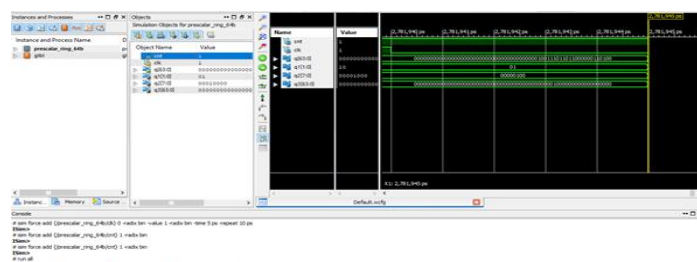


Fig. 9. Simulation waveform for existing system

B. PROPOSED METHOD

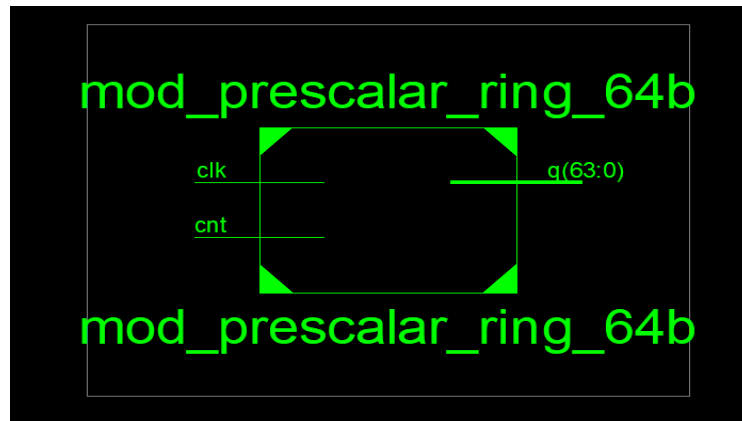


Fig. 10. RTL Schmatic

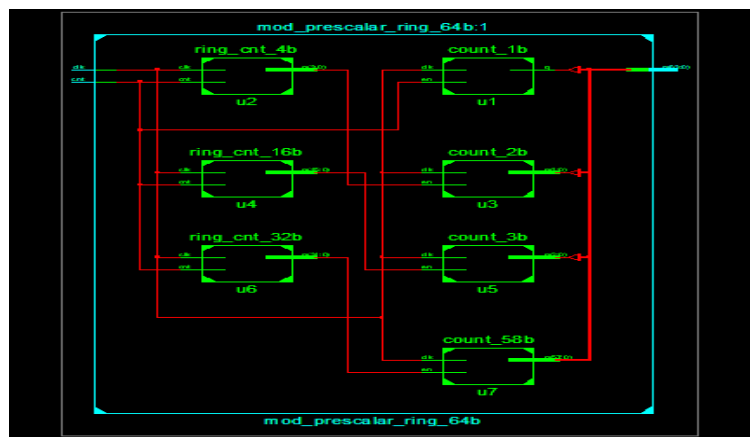


Fig. 11. Technology Schematic

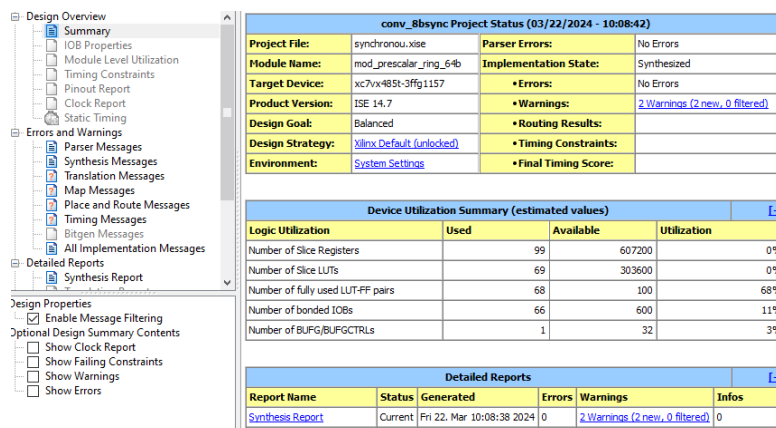


Fig. 12. Showing Area Utilization

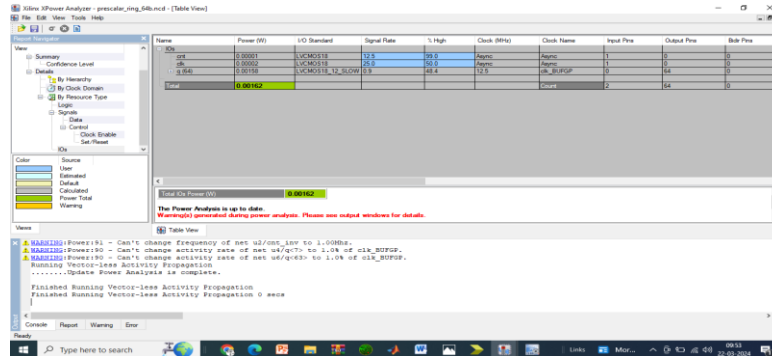


Fig. 13. Shwoing power consumption

C. COMPARISION TABLE

TABLE I. COMPARISON OF PERFORMANCE WITH EXISTING AND PROPOSED METHODS

S. No	Model	Area			Delay (ns)	Power (w)
		Registers	LUT	IOBs		
1	Existing Method	131	68	66	1.172	0.0162
2	Proposed Method	99	65	66	0.978	0.00107

The above table shows the simulation results comparing the current approach with the suggested approach for generating prescaled enable signals using ring counters and a 64-bit prescaled counter. The design uses 66 IOBs, 68 LUTs, and 131 registers in the current technique, which results in a 0.0162 W power consumption and a 1.172 ns delay. On the other hand, the suggested approach optimizes the design and keeps 65 LUTs and 66 IOBs while cutting the number of registers to 99. With this adjustment, the delay is much improved to 0.978 ns, and the power consumption is significantly reduced to 0.00107 W.

The outcomes of this simulation demonstrate how well the suggested approach outperforms the current approach in terms of performance metrics. A constant-time synchronous binary counter with a short clock period can be achieved with the optimized parallel architecture, as seen by the decrease in space use, delay, and power consumption. Through the use of prescaling-based modified constant-delay ring counters, the suggested approach provides a viable means of improving the speed and efficiency of synchronous binary counters in digital circuit design.

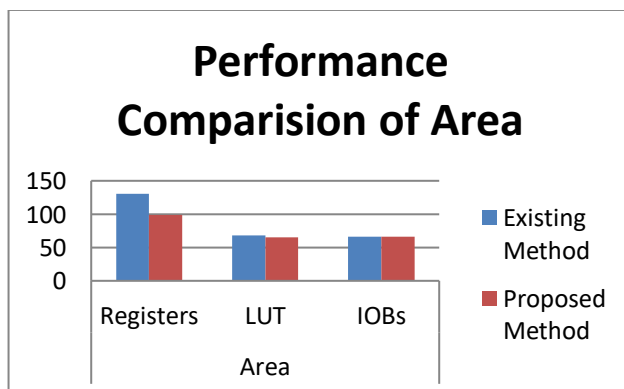


Fig.14. Showing Area Performance comparision of Existing and Propsoed method

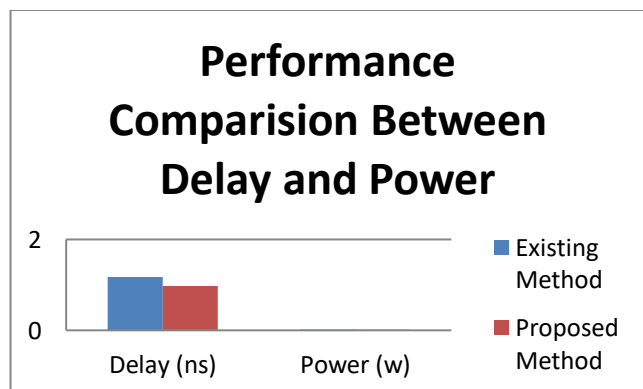


Fig. 14. Showing Delay and Performance comparison of Existing and Propsoed method

Volume 14, Issue 4, April 2025**|DOI: 10.15680/IJIRSET.2025.1404232|****VI. CONCLUSION**

The study's simulation findings demonstrate how well the suggested optimized parallel architecture works for a constant-time synchronous binary counter with a short clock period. Key performance parameters like area usage, delay, and power consumption have significantly improved with the use of modified constant-delay ring counters based on prescaling. The benefits of the suggested method are amply illustrated by a comparison with the current approach. The suggested approach yields a significant reduction in time, resulting in faster counting operations, by lowering the number of registers while keeping comparable LUT and IOB counts. Furthermore, a notable decrease in power consumption is achieved by the optimized design, improving energy efficiency. These results highlight how crucial creative design approaches are to raising the bar for digital circuit design. In addition to providing better performance, the suggested architecture creates new opportunities for applications needing synchronous binary counters with consistent clock intervals.

VII. FUTURE SCOPE

Subsequent investigations can concentrate on enhancing the suggested architecture to get even higher efficiency for area utilization, latency, and power consumption. This could entail investigating different design approaches, improving circuit layouts, or making use of cutting-edge technologies like three-dimensional integration or deep sub-micron processes.

REFERENCES

- [1] In 1998, M.R. Stan, A.F. Tenca, and M.D. Ercegovac published "Long and fast up/down counters" in Computers IEEE Transactions on, vol. 47, no. 7, pp. 722-735.
- [2] In Electronics Letters, vol. 24, no. 21, pp. 1311-1313, Oct. 13, 1988, J. -. Yuan, "Efficient CMOS counter circuits," doi: 10.1049/el:19880891.
- [3] "Comparison of binary and LFSR counters and efficient LFSR decoding algorithm," A. Ajane, P. M. Furth, E. E. Johnson, and R. L. Subramanyam, 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, 2011, pp. 1-4, doi: 10.1109/MWSCAS.2011.6026392.
- [4] "High speed digital CMOS divide-by-N frequency divider," S. Abdel-Hafeez, S. M. Harb, and W. R. Eisenstadt, 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, 2008, pp. 592-595, doi: 10.1109/ISCAS.2008.4541487
- [5] "Synchronous Counter," U.S. Patent No. 5,526,393, June 1996, Kondo, M., and Watnaba, T.
- [6] In the 2016 International Conference on Microelectronics, Computing and Communications (MicroCom), Durgapur, pp. 1-5, P. R. Thota and A. K. Mal, "A high speed counter for analog-to-digital converters," doi: 10.1109/MicroCom.2016.7522592.
- [7] In IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 43, no. 11, pp. 939-941, Nov. 1996, D. R. Lutz and D. N. Jayasimha, "Programmable modulo-K counters," doi: 10.1109/81.542285
- [8] . In IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 41, no. 11, pp. 775-776, Nov. 1994, K. Z. Pekmestzi and N. Thanasouras, "Systolic frequency dividers/counters," doi: 10.1109/82.331551.
- [9] In the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 1, pp. 103-115, Jan. 2019, doi: 10.1109/TVLSI.2018.2872021,
- [10] D. Morrison, D. Delic, M. R. Yuze, and J. Redouté, "Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications," In Electronics Letters, vol. 29, no. 16, pp. 1457-1458, Aug. 5, 1993, P. Larsson and J. Yuan, "Novel carry propagation in high-speed synchronous counters and dividers," doi: 10.1049/el:19930975



INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  ijirset@gmail.com



www.ijirset.com

Scan to save the contact details